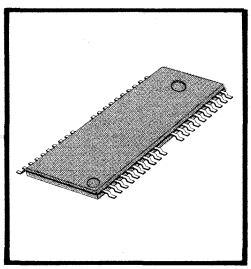
SAMSUNG

1120-4101

MOS Memory

1995



- SRAM
- FIFO

PRINTED IN KOREA

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Certified ISO 9001

Certificate No FM 24651

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Pseudo SRAMs

5V CMOS Fast SRAM

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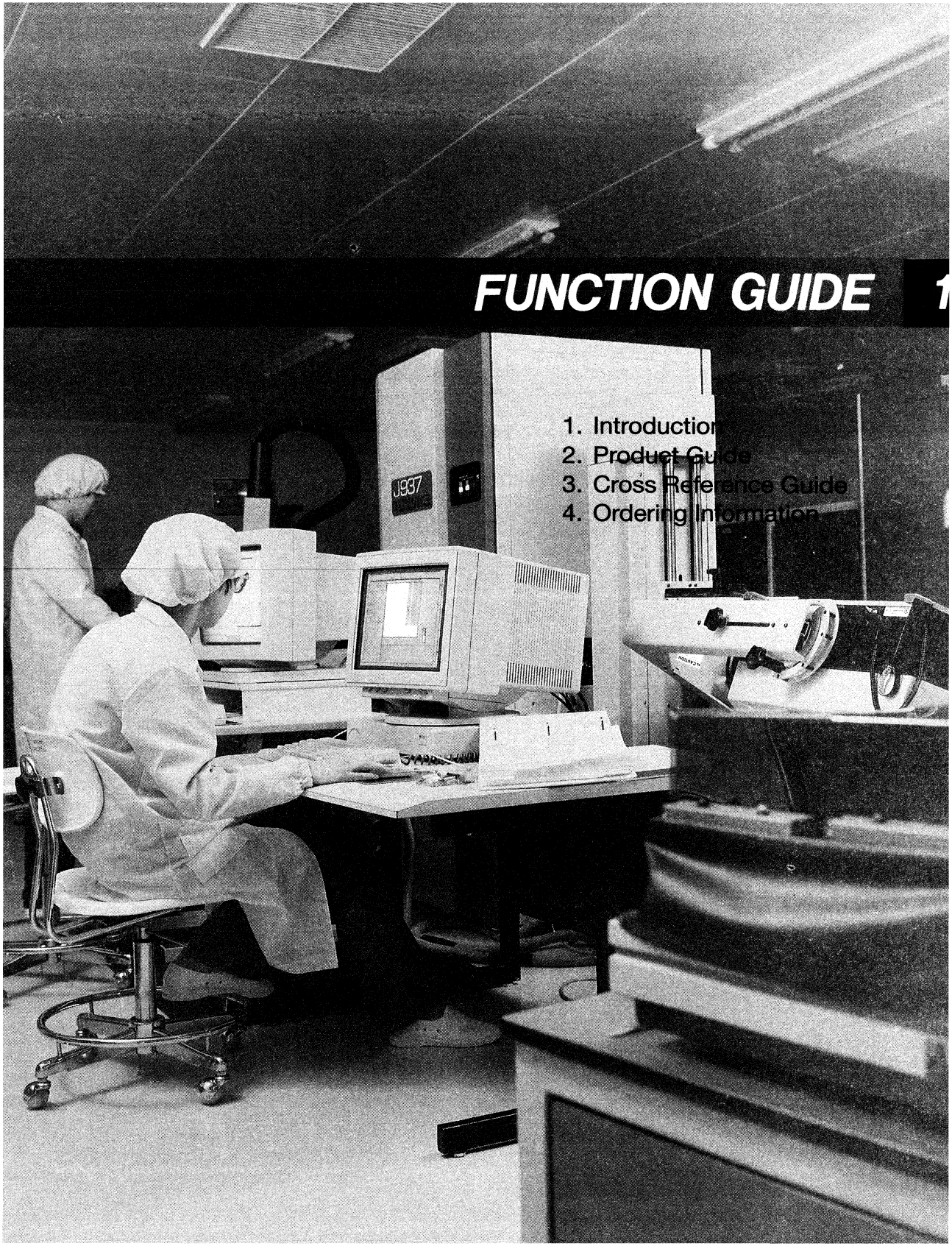
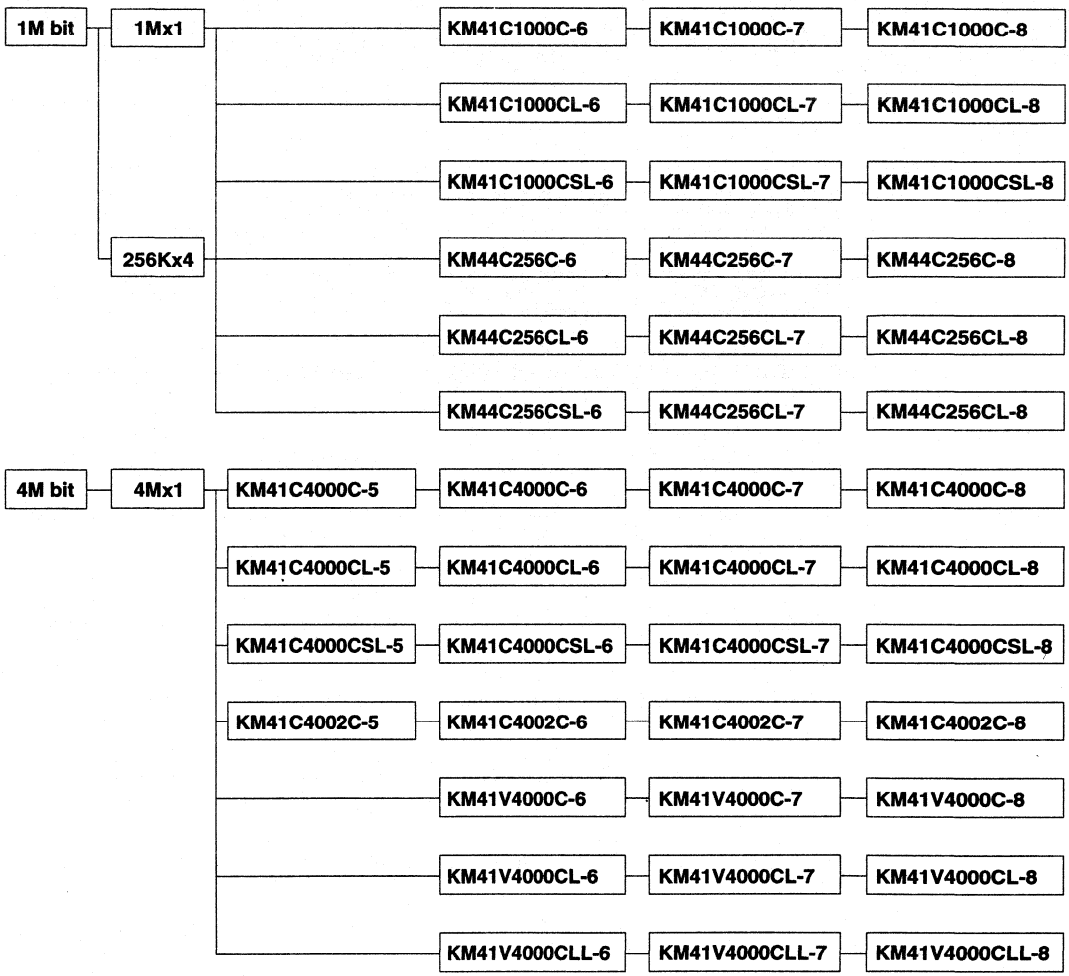


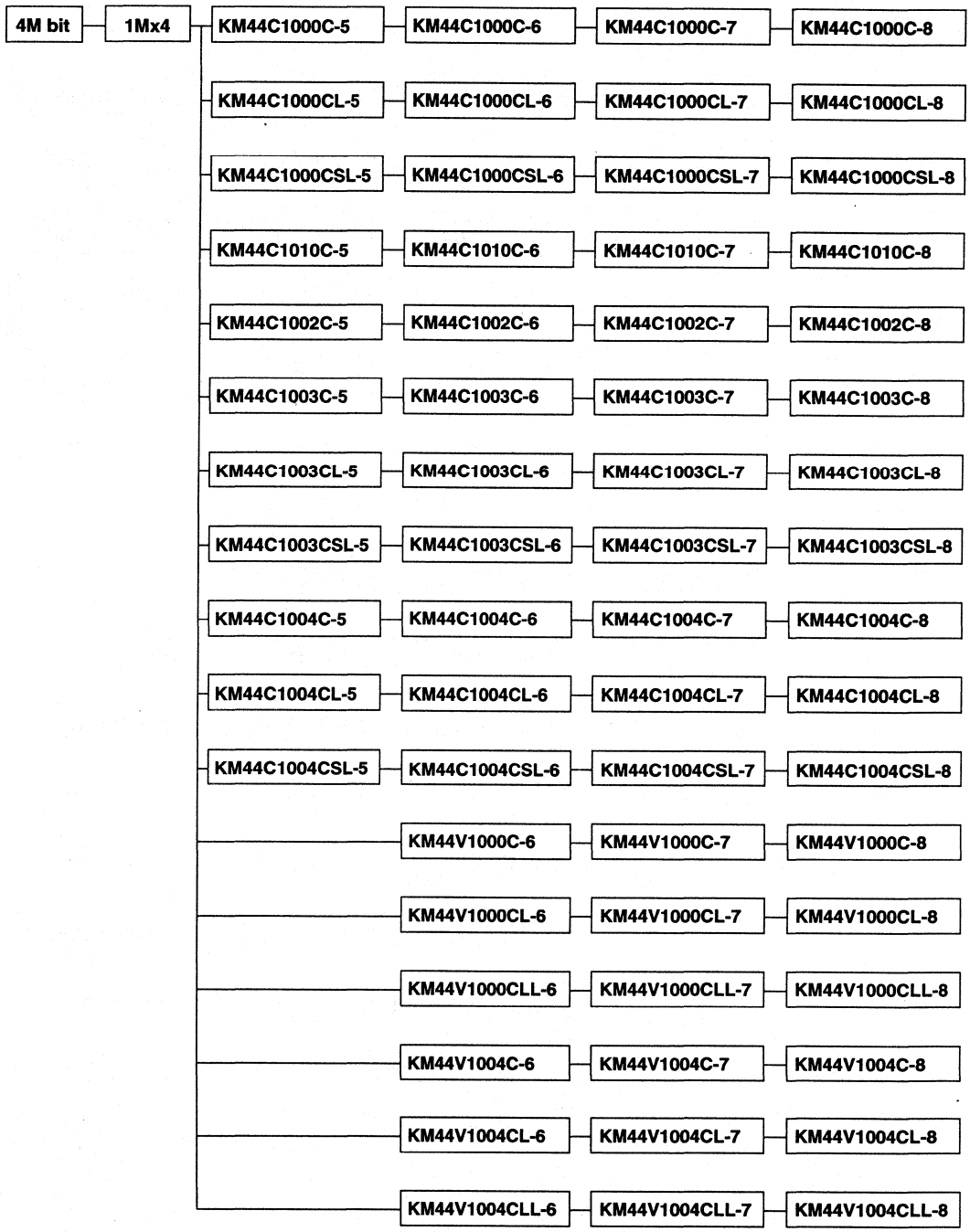
FUNCTION GUIDE 1

1. Introduction
2. Product Guide
3. Cross Reference Guide
4. Ordering Information

1. INTRODUCTION

1.1 Dynamic RAM

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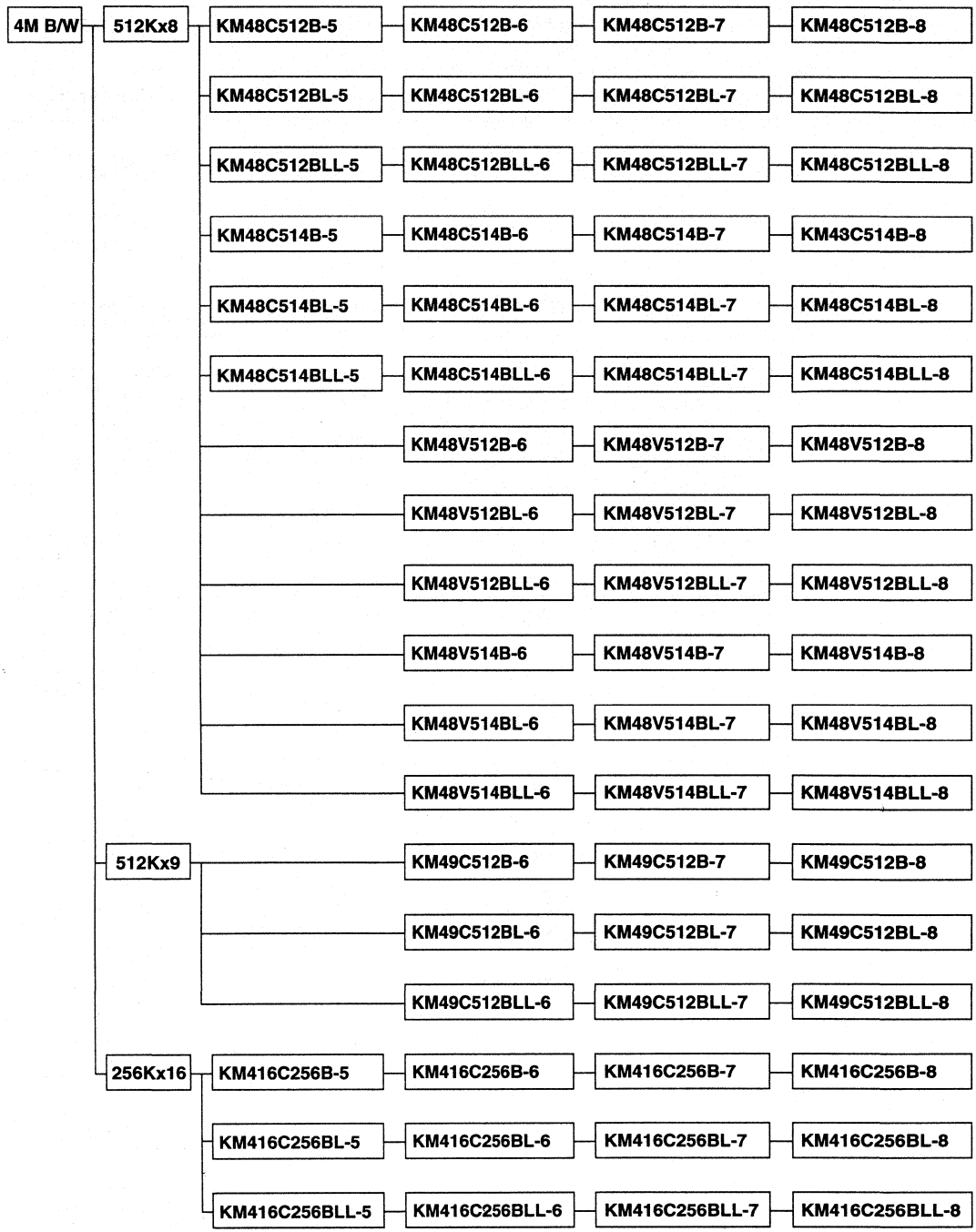
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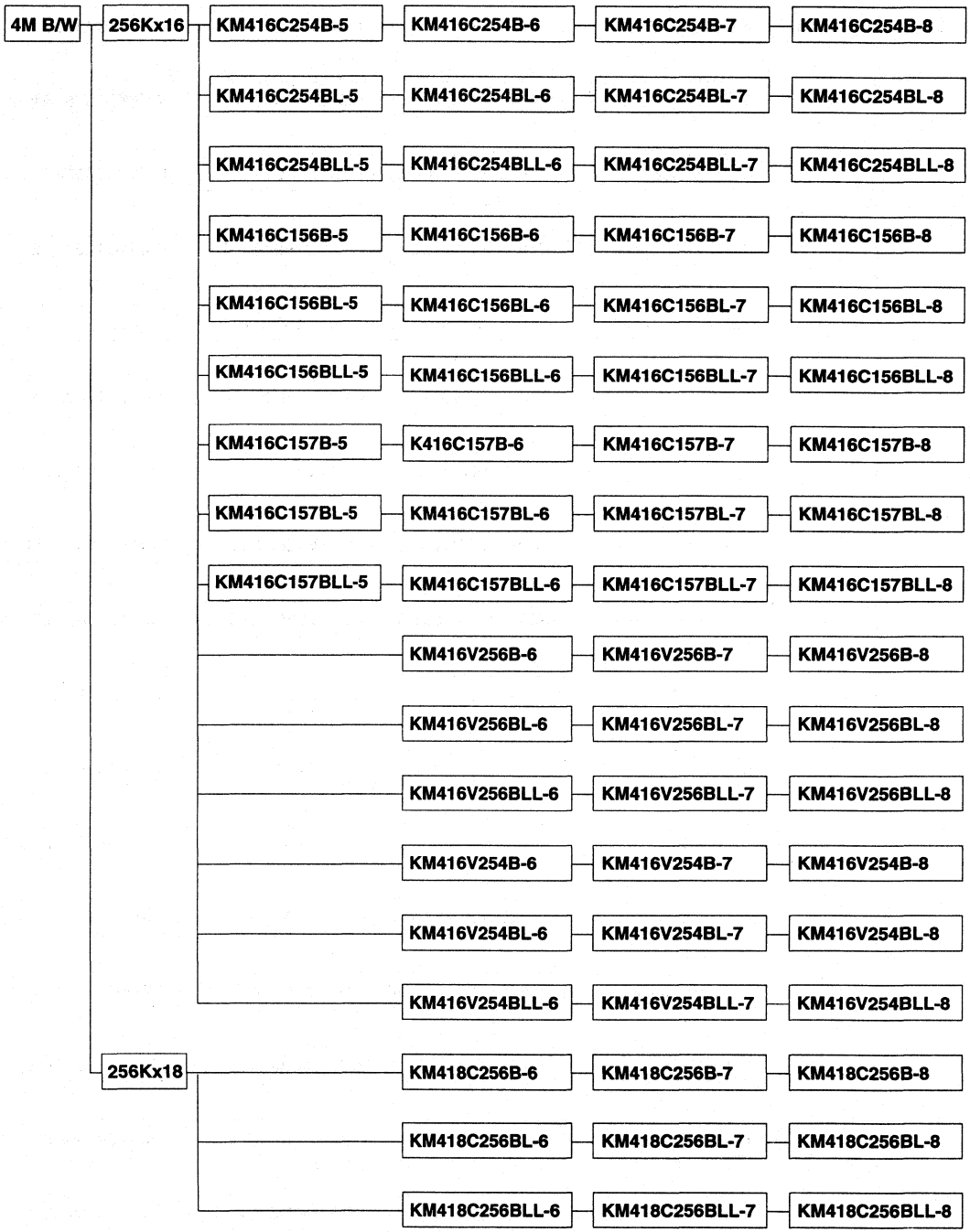
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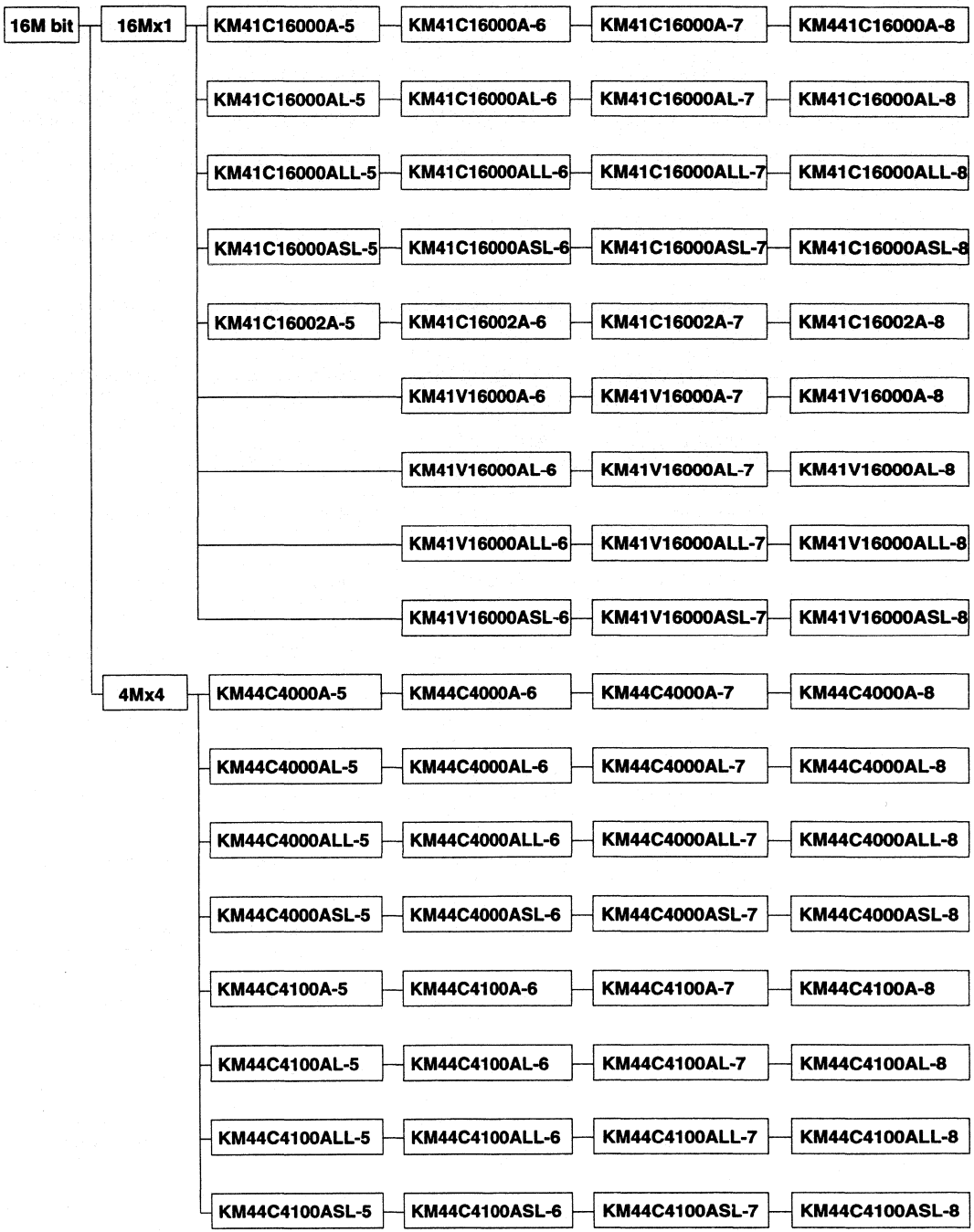
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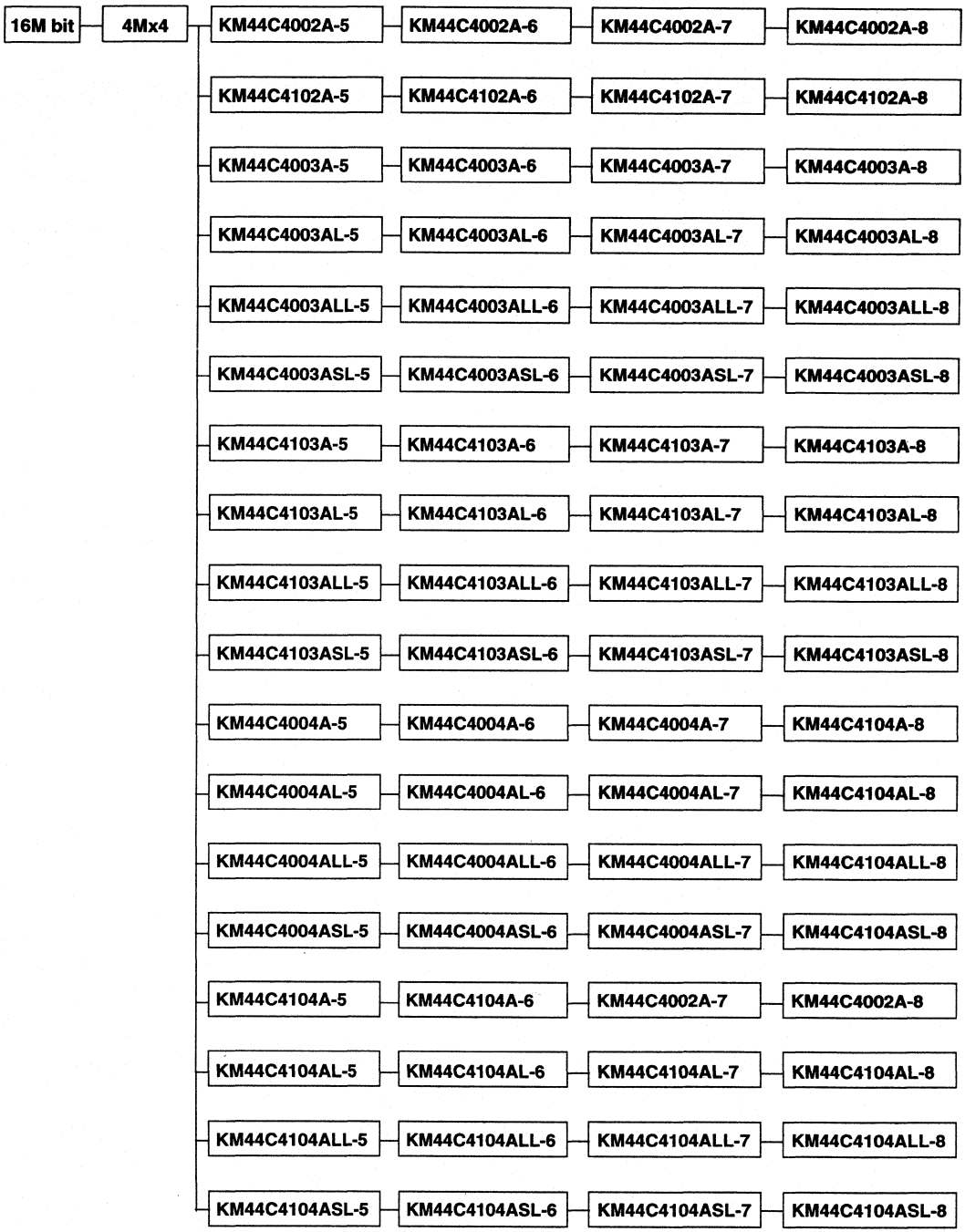
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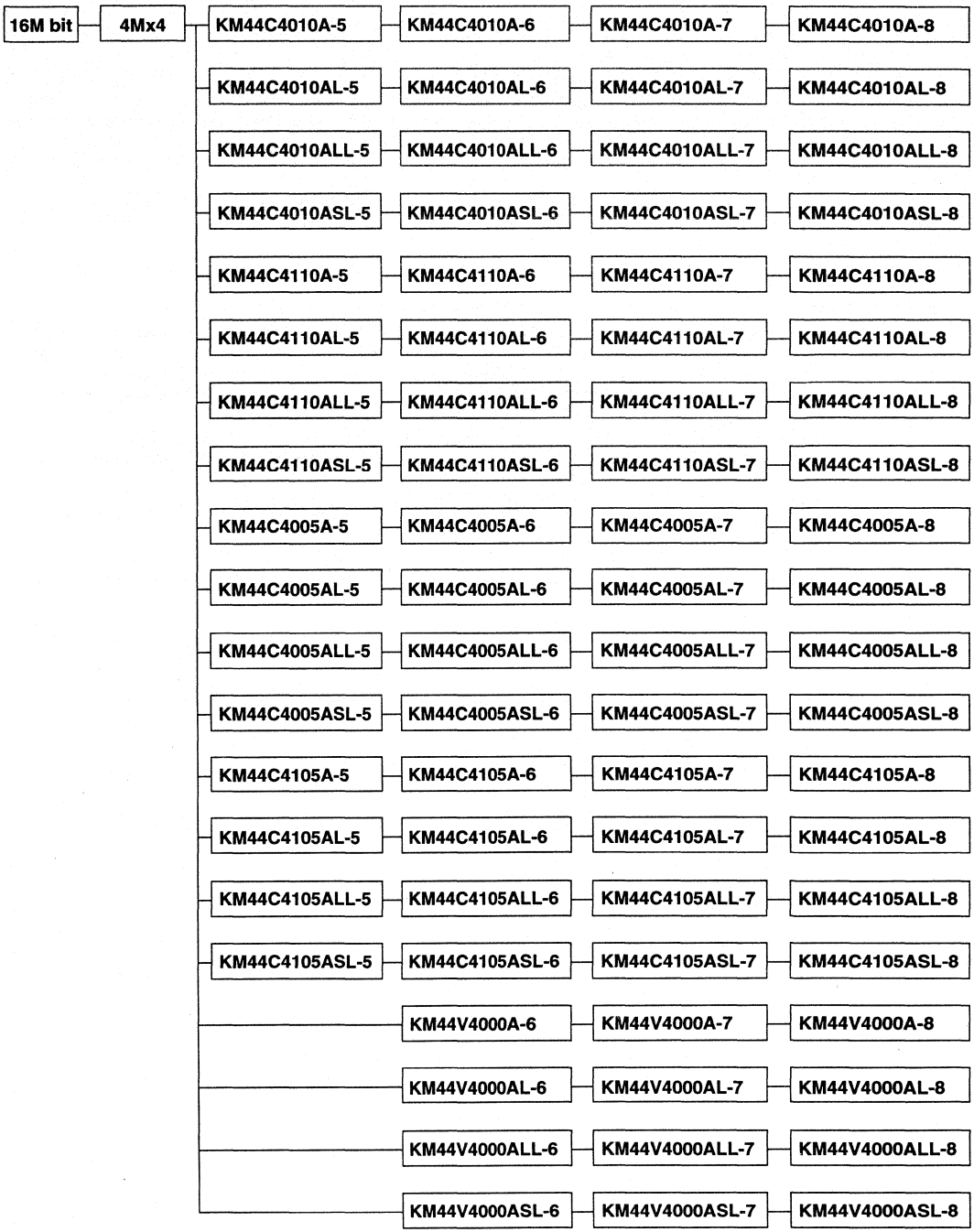
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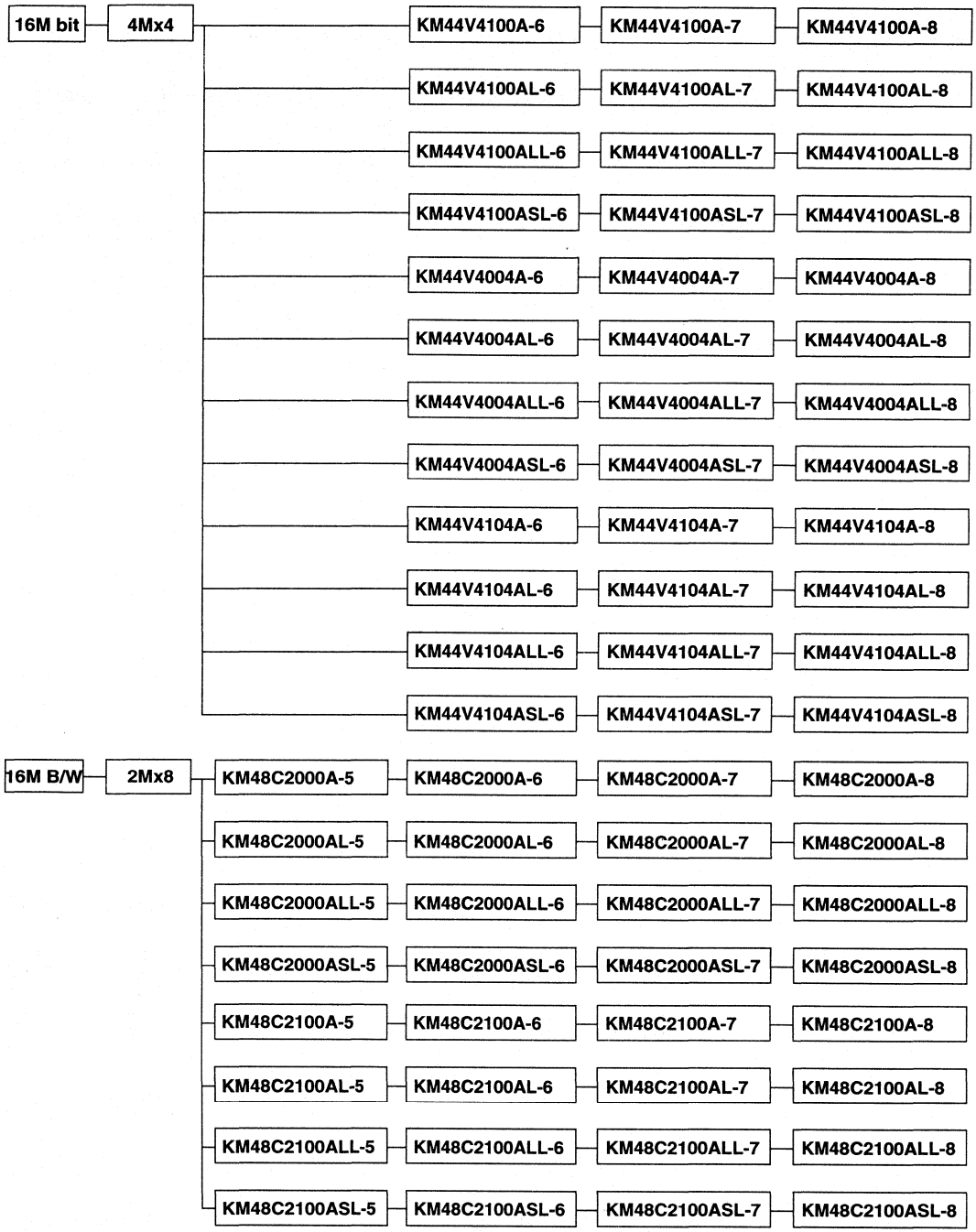
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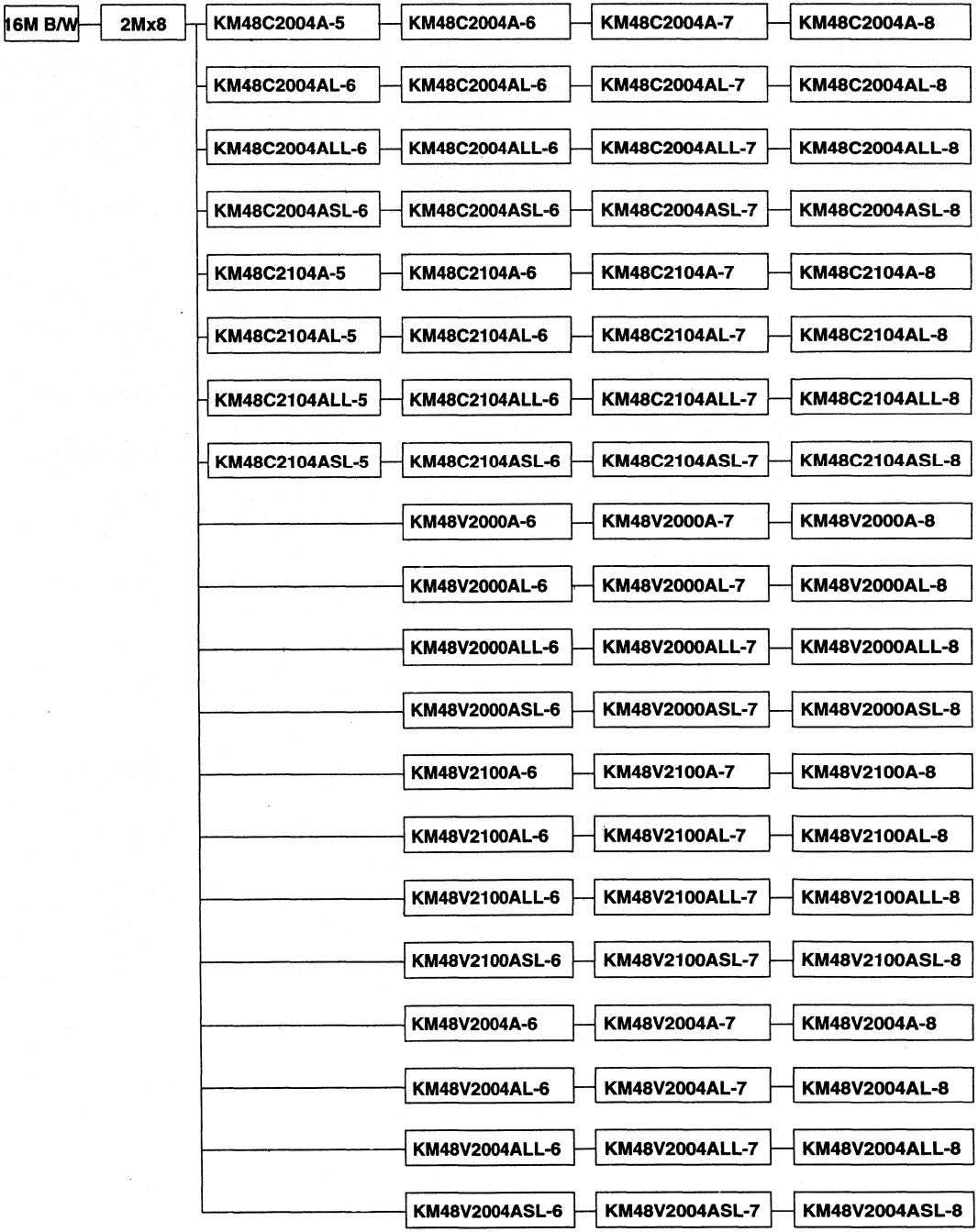
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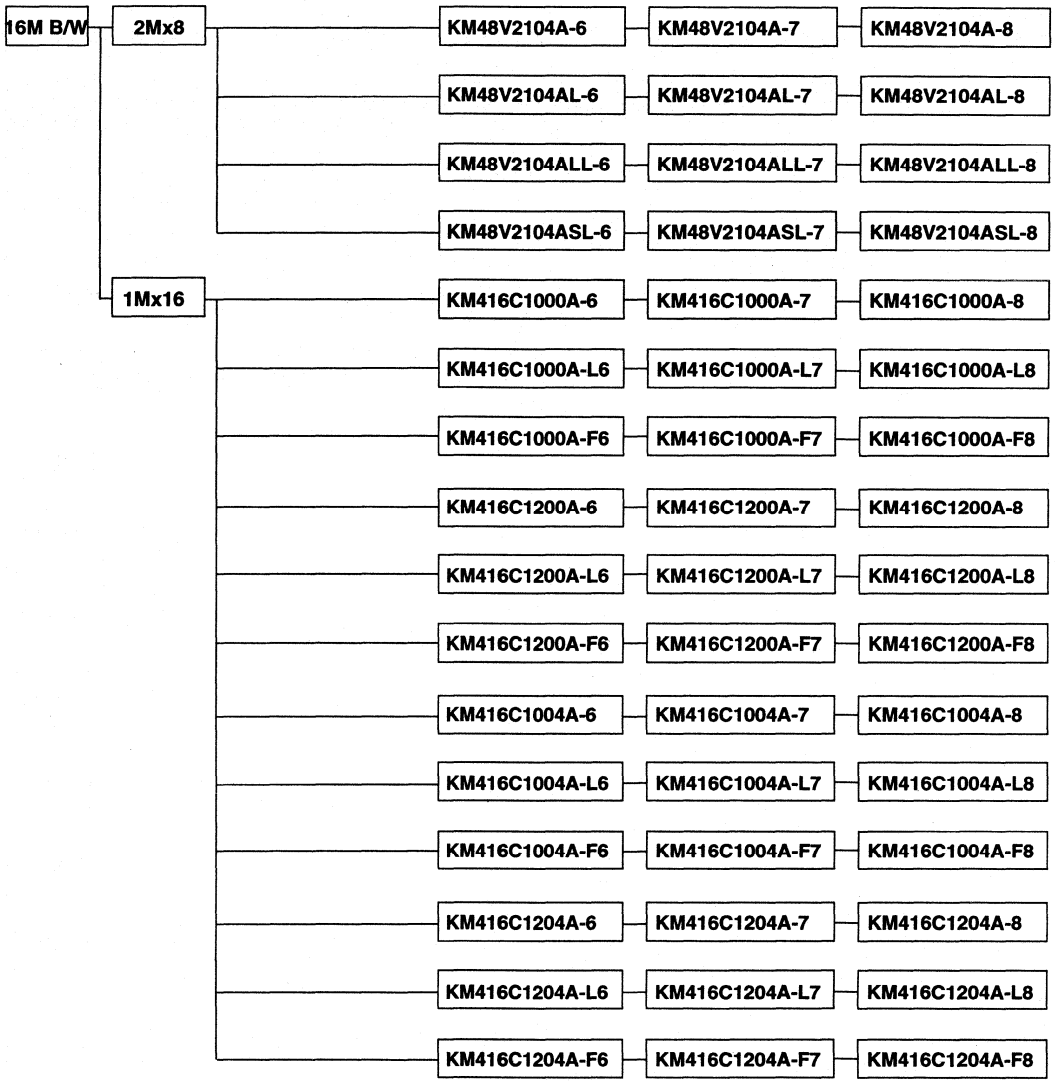
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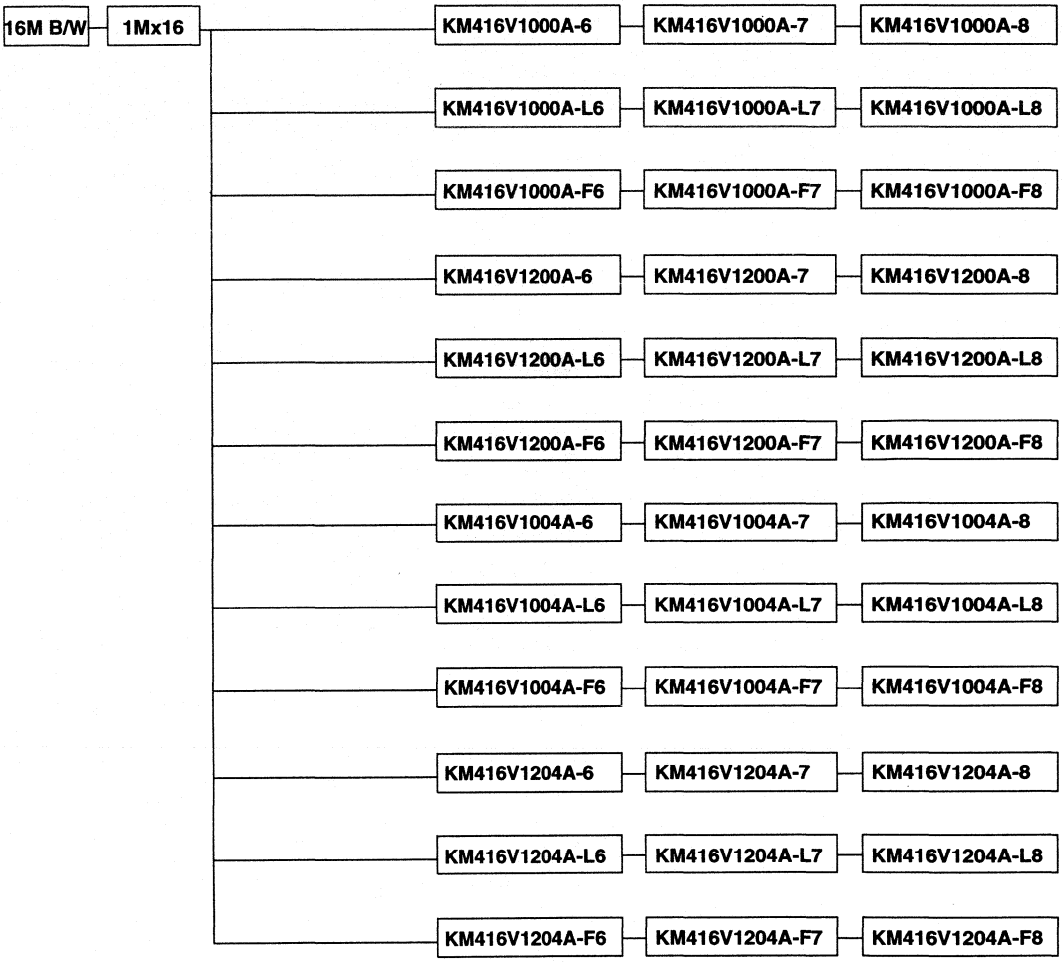
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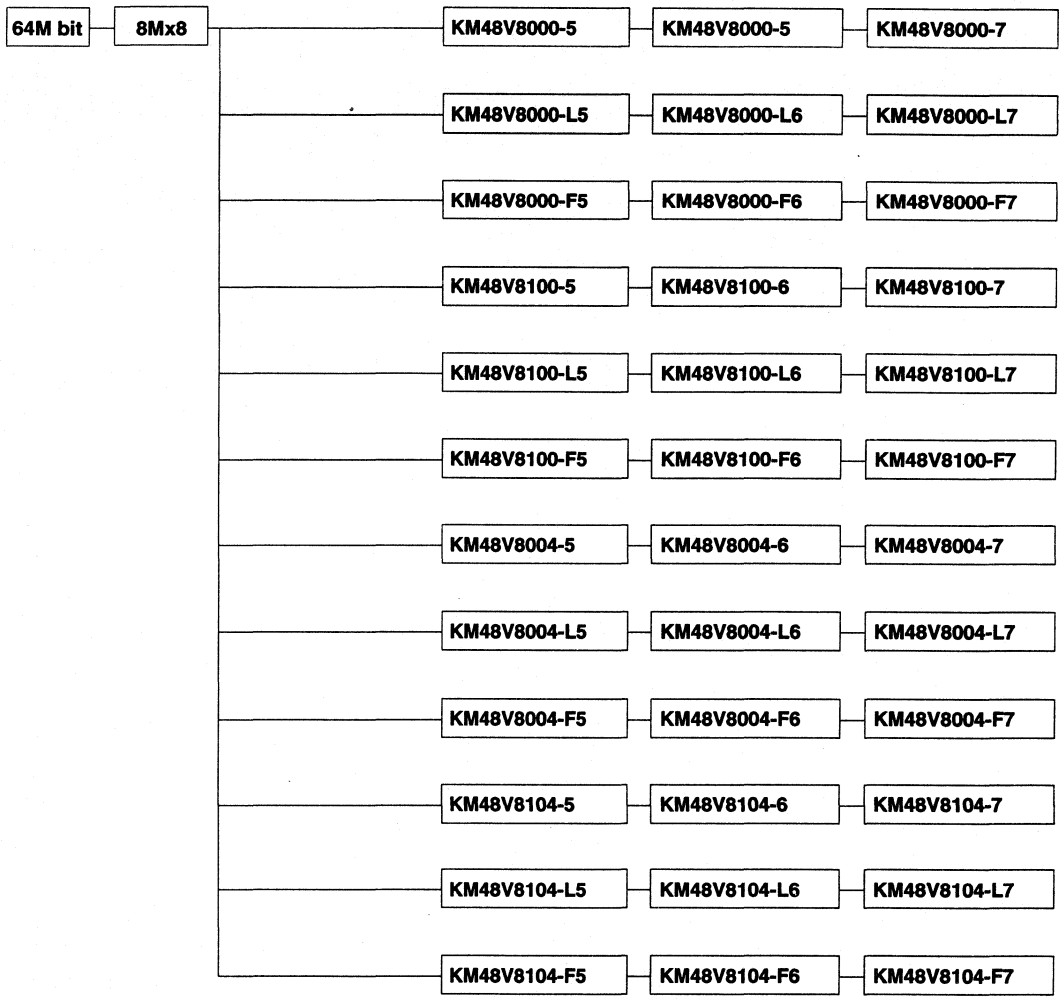
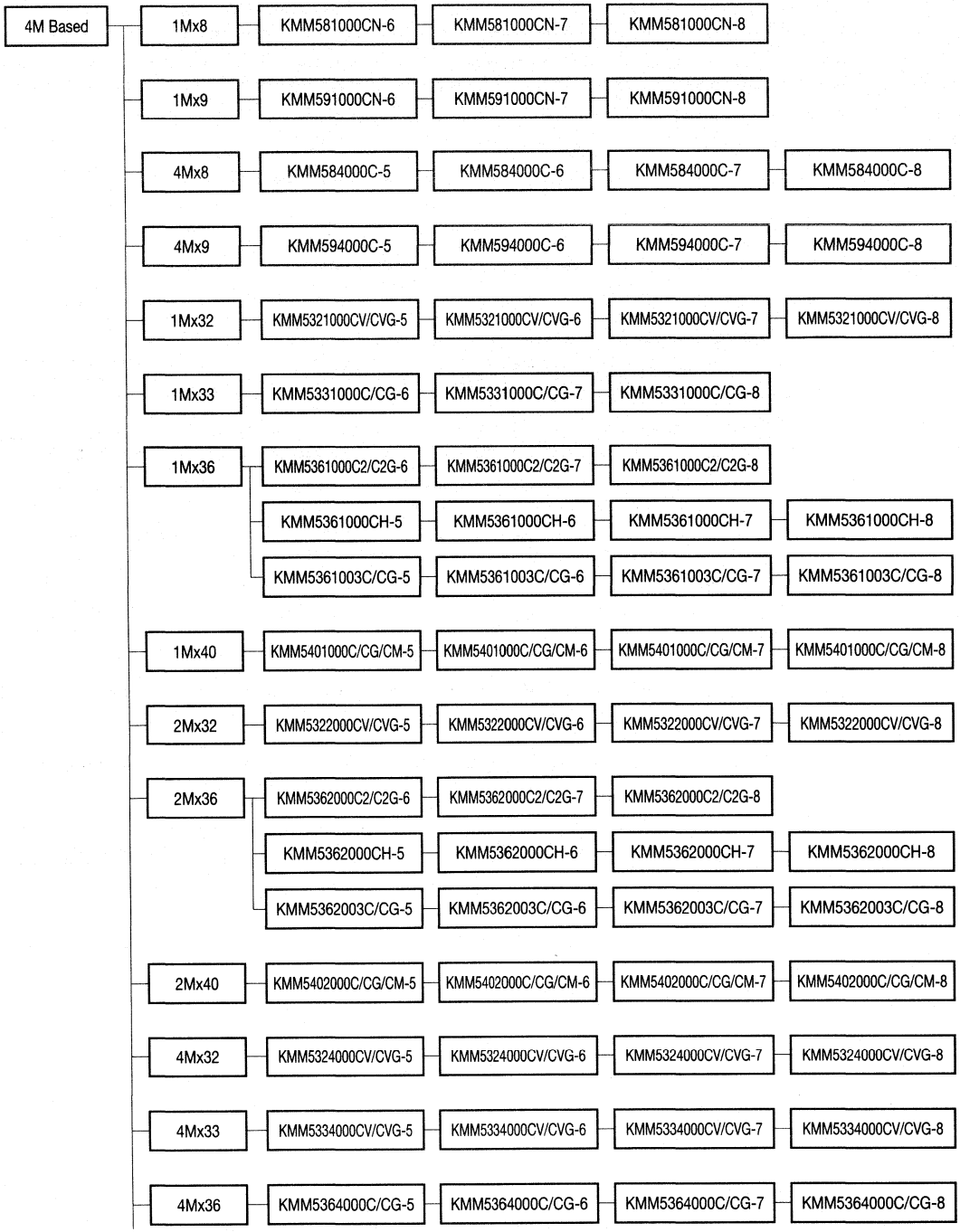
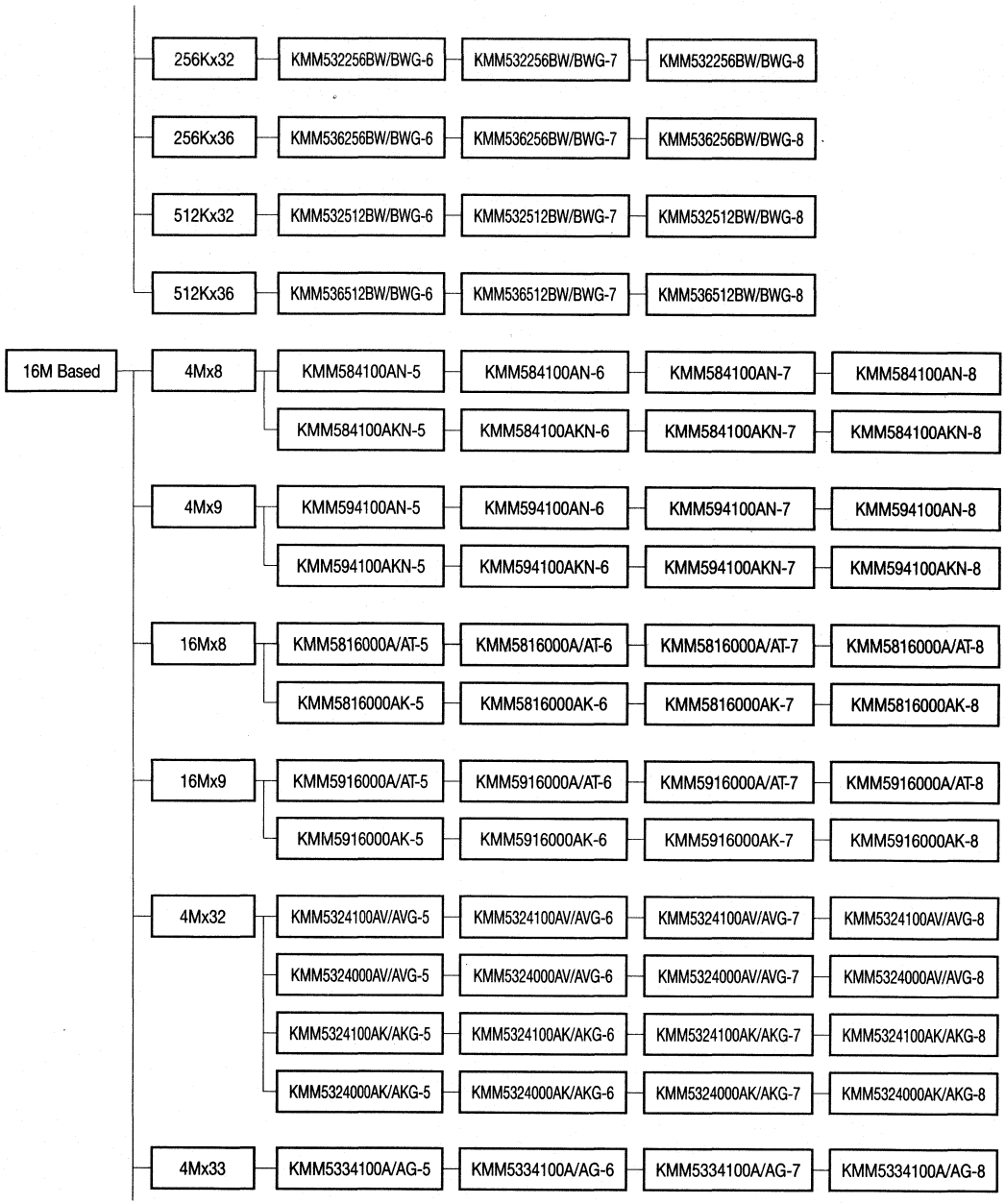
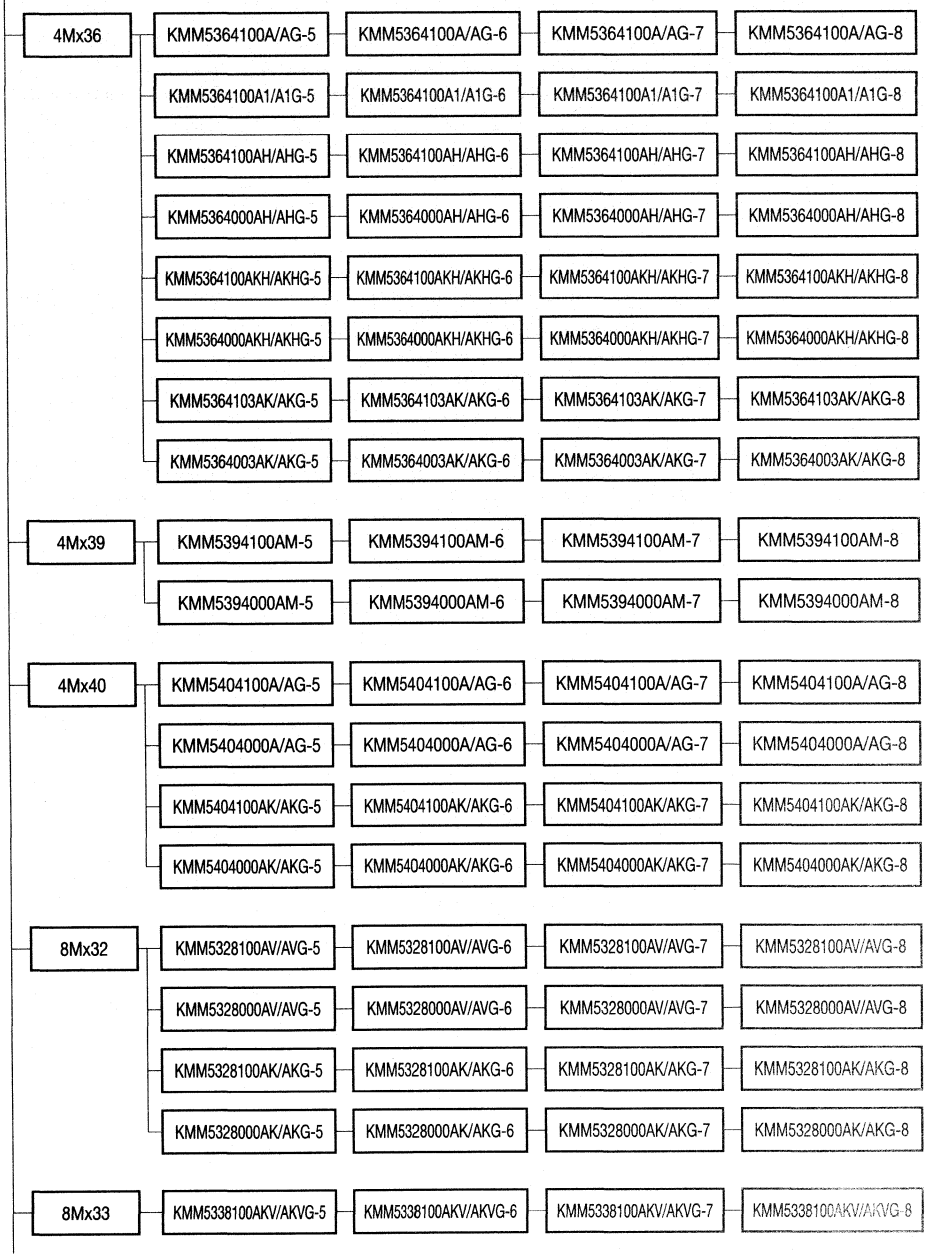
KM416V1000A-L6
KM416V1000A-L7
KM416V1000A-L8
KM416V1000A-F6
KM416V1000A-F7
KM416V1000A-F8
KM416V1200A-6
KM416V1200A-7
KM416V1200A-8
KM416V1200A-L6
KM416V1200A-L7
KM416V1200A-L8
KM416V1200A-F6
KM416V1200A-F7
KM416V1200A-F8
KM416V1004A-6
KM416V1004A-7
KM416V1004A-8
KM416V1004A-L6
KM416V1004A-L7
KM416V1004A-L8
KM416V1004A-F6
KM416V1004A-F7
KM416V1004A-F8
KM416V1204A-6
KM416V1204A-7
KM416V1204A-8
KM416V1204A-L6
KM416V1204A-L7
KM416V1204A-L8
KM416V1204A-F6
KM416V1204A-F7
KM416V1204A-F8

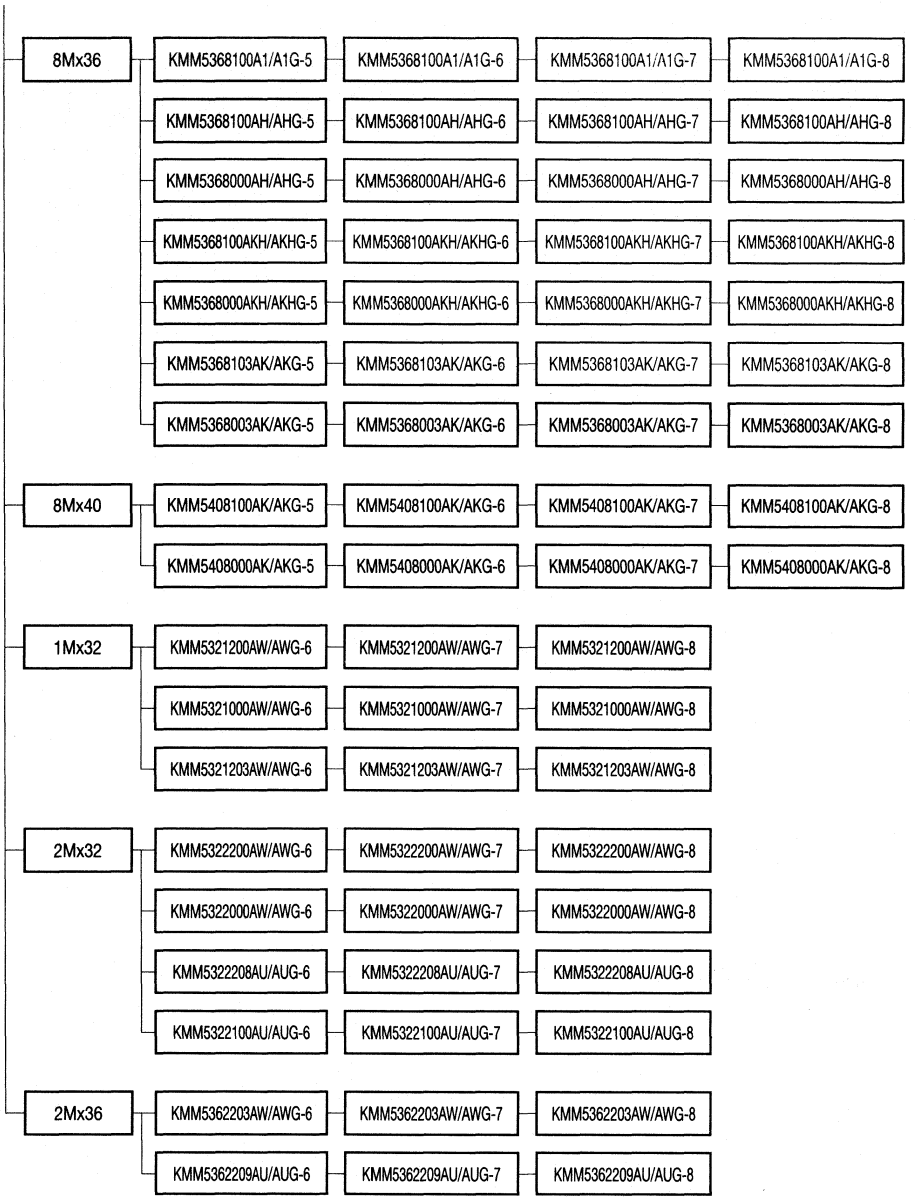

64M bit
8Mx8
KM48V8000-5
KM48V8000-5
KM48V8000-7
KM48V8000-L5
KM48V8000-L6
KM48V8000-L7
KM48V8000-F5
KM48V8000-F6
KM48V8000-F7
KM48V8100-5
KM48V8100-6
KM48V8100-7
KM48V8100-L5
KM48V8100-L6
KM48V8100-L7
KM48V8100-F5
KM48V8100-F6
KM48V8100-F7
KM48V8004-5
KM48V8004-6
KM48V8004-7
KM48V8004-L5
KM48V8004-L6
KM48V8004-L7
KM48V8004-F5
KM48V8004-F6
KM48V8004-F7
KM48V8104-5
KM48V8104-6
KM48V8104-7
KM48V8104-L5
KM48V8104-L6
KM48V8104-L7
KM48V8104-F5
KM48V8104-F6
KM48V8104-F7

1.2 Dynamic RAM Module

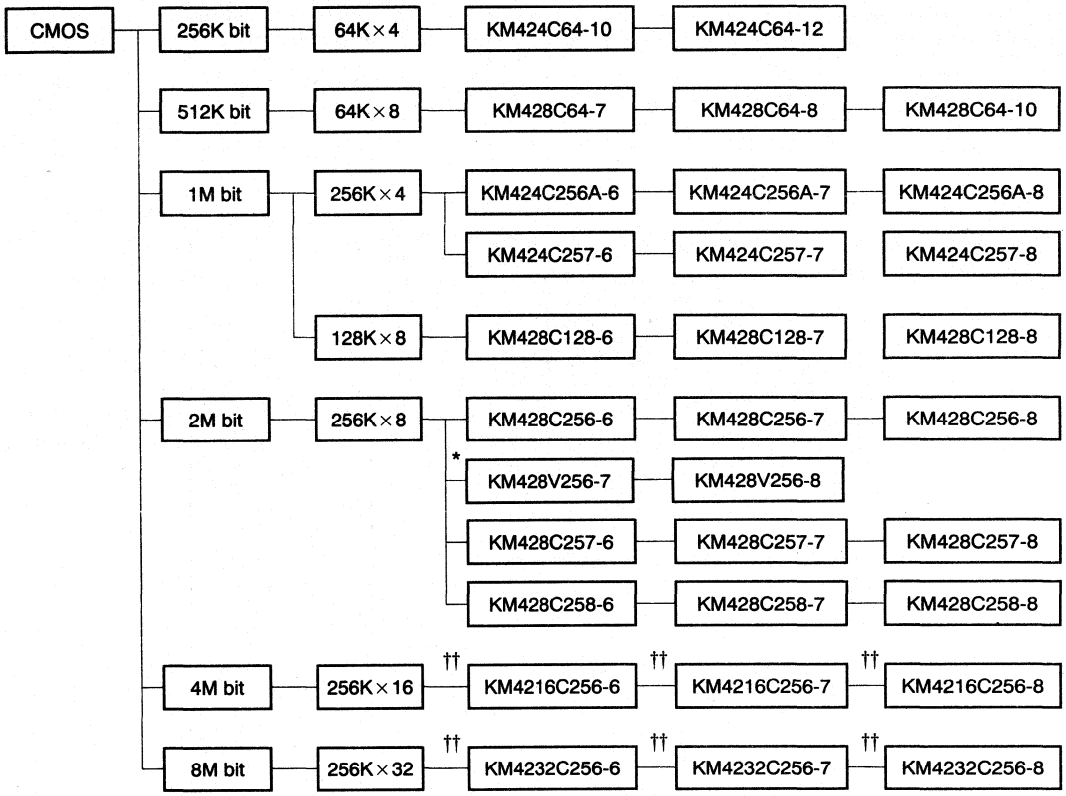



256Kx32
KMM532256BW/BWG-6
KMM532256BW/BWG-7
KMM532256BW/BWG-8
256Kx36
KMM536256BW/BWG-6
KMM536256BW/BWG-7
KMM536256BW/BWG-8
512Kx32
KMM532512BW/BWG-6
KMM532512BW/BWG-7
KMM532512BW/BWG-8
512Kx36
KMM536512BW/BWG-6
KMM536512BW/BWG-7
KMM536512BW/BWG-8
16M Based
4Mx8
KMM584100AN-5
KMM584100AN-6
KMM584100AN-7
KMM584100AN-8
KMM584100AKN-5
KMM584100AKN-6
KMM584100AKN-7
KMM584100AKN-8
4Mx9
KMM594100AN-5
KMM594100AN-6
KMM594100AN-7
KMM594100AN-8
KMM594100AKN-5
KMM594100AKN-6
KMM594100AKN-7
KMM594100AKN-8
16Mx8
KMM5816000A/AT-5
KMM5816000A/AT-6
KMM5816000A/AT-7
KMM5816000A/AT-8
KMM5816000AK-5
KMM5816000AK-6
KMM5816000AK-7
KMM5816000AK-8
16Mx9
KMM5916000A/AT-5
KMM5916000A/AT-6
KMM5916000A/AT-7
KMM5916000A/AT-8
KMM5916000AK-5
KMM5916000AK-6
KMM5916000AK-7
KMM5916000AK-8
4Mx32
KMM5324100AV/AVG-5
KMM5324100AV/AVG-6
KMM5324100AV/AVG-7
KMM5324100AV/AVG-8
KMM5324000AV/AVG-5
KMM5324000AV/AVG-6
KMM5324000AV/AVG-7
KMM5324000AV/AVG-8
KMM5324100AK/AKG-5
KMM5324100AK/AKG-6
KMM5324100AK/AKG-7
KMM5324100AK/AKG-8
KMM5324000AK/AKG-5
KMM5324000AK/AKG-6
KMM5324000AK/AKG-7
KMM5324000AK/AKG-8
4Mx33
KMM5334100A/AG-5
KMM5334100A/AG-6
KMM5334100A/AG-7
KMM5334100A/AG-8


4Mx36
KMM5364100A/AG-5
KMM5364100A/AG-6
KMM5364100A/AG-7
KMM5364100A/AG-8
KMM5364100A1/A1G-5
KMM5364100A1/A1G-6
KMM5364100A1/A1G-7
KMM5364100A1/A1G-8
KMM5364100AH/AHG-5
KMM5364100AH/AHG-6
KMM5364100AH/AHG-7
KMM5364100AH/AHG-8
KMM5364000AH/AHG-5
KMM5364000AH/AHG-6
KMM5364000AH/AHG-7
KMM5364000AH/AHG-8
KMM5364100AKH/AKHG-5
KMM5364100AKH/AKHG-6
KMM5364100AKH/AKHG-7
KMM5364100AKH/AKHG-8
KMM5364000AKH/AKHG-5
KMM5364000AKH/AKHG-6
KMM5364000AKH/AKHG-7
KMM5364000AKH/AKHG-8
KMM5364103AK/AKG-5
KMM5364103AK/AKG-6
KMM5364103AK/AKG-7
KMM5364103AK/AKG-8
KMM5364003AK/AKG-5
KMM5364003AK/AKG-6
KMM5364003AK/AKG-7
KMM5364003AK/AKG-8
4Mx39
KMM5394100AM-5
KMM5394100AM-6
KMM5394100AM-7
KMM5394100AM-8
KMM5394000AM-5
KMM5394000AM-6
KMM5394000AM-7
KMM5394000AM-8
4Mx40
KMM5404100A/AG-5
KMM5404100A/AG-6
KMM5404100A/AG-7
KMM5404100A/AG-8
KMM5404000A/AG-5
KMM5404000A/AG-6
KMM5404000A/AG-7
KMM5404000A/AG-8
KMM5404100AK/AKG-5
KMM5404100AK/AKG-6
KMM5404100AK/AKG-7
KMM5404100AK/AKG-8
KMM5404000AK/AKG-5
KMM5404000AK/AKG-6
KMM5404000AK/AKG-7
KMM5404000AK/AKG-8
8Mx32
KMM5328100AV/AVG-5
KMM5328100AV/AVG-6
KMM5328100AV/AVG-7
KMM5328100AV/AVG-8
KMM5328000AV/AVG-5
KMM5328000AV/AVG-6
KMM5328000AV/AVG-7
KMM5328000AV/AVG-8
KMM5328100AK/AKG-5
KMM5328100AK/AKG-6
KMM5328100AK/AKG-7
KMM5328100AK/AKG-8
KMM5328000AK/AKG-5
KMM5328000AK/AKG-6
KMM5328000AK/AKG-7
KMM5328000AK/AKG-8
8Mx33
KMM5338100AKV/AKVG-5
KMM5338100AKV/AKVG-6
KMM5338100AKV/AKVG-7
KMM5338100AKV/AKVG-8


8Mx36
KMM5368100A1/A1G-5
KMM5368100A1/A1G-6
KMM5368100A1/A1G-7
KMM5368100A1/A1G-8
KMM5368100AH/AHG-5
KMM5368100AH/AHG-6
KMM5368100AH/AHG-7
KMM5368100AH/AHG-8
KMM5368000AH/AHG-5
KMM5368000AH/AHG-6
KMM5368000AH/AHG-7
KMM5368000AH/AHG-8
KMM5368100AKH/AKHG-5
KMM5368100AKH/AKHG-6
KMM5368100AKH/AKHG-7
KMM5368100AKH/AKHG-8
KMM5368000AKH/AKHG-5
KMM5368000AKH/AKHG-6
KMM5368000AKH/AKHG-7
KMM5368000AKH/AKHG-8
KMM5368103AK/AKG-5
KMM5368103AK/AKG-6
KMM5368103AK/AKG-7
KMM5368103AK/AKG-8
KMM5368003AK/AKG-5
KMM5368003AK/AKG-6
KMM5368003AK/AKG-7
KMM5368003AK/AKG-8
8Mx40
KMM5408100AK/AKG-5
KMM5408100AK/AKG-6
KMM5408100AK/AKG-7
KMM5408100AK/AKG-8
KMM5408000AK/AKG-5
KMM5408000AK/AKG-6
KMM5408000AK/AKG-7
KMM5408000AK/AKG-8
1Mx32
KMM5321200AW/AWG-6
KMM5321200AW/AWG-7
KMM5321200AW/AWG-8
KMM5321000AW/AWG-6
KMM5321000AW/AWG-7
KMM5321000AW/AWG-8
KMM5321203AW/AWG-6
KMM5321203AW/AWG-7
KMM5321203AW/AWG-8
2Mx32
KMM5322200AW/AWG-6
KMM5322200AW/AWG-7
KMM5322200AW/AWG-8
KMM5322000AW/AWG-6
KMM5322000AW/AWG-7
KMM5322000AW/AWG-8
KMM5322208AU/AUG-6
KMM5322208AU/AUG-7
KMM5322208AU/AUG-8
KMM5322100AU/AUG-6
KMM5322100AU/AUG-7
KMM5322100AU/AUG-8
2Mx36
KMM5362203AW/AWG-6
KMM5362203AW/AWG-7
KMM5362203AW/AWG-8
KMM5362209AU/AUG-6
KMM5362209AU/AUG-7
KMM5362209AU/AUG-8

1.3 Video RAM

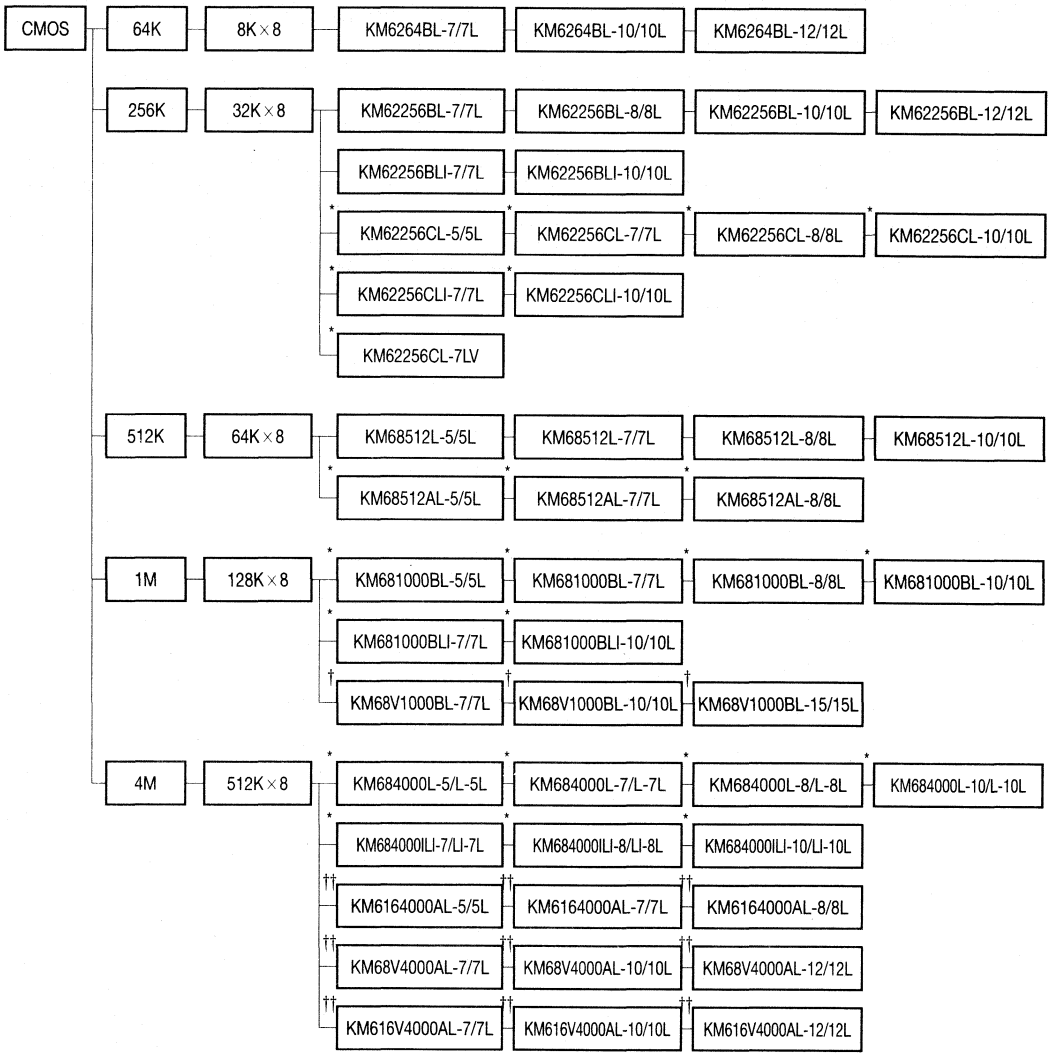


†† Under Development

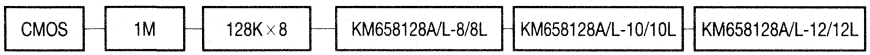
SAMSUNG ELECTRONICS

1.4 Static RAM

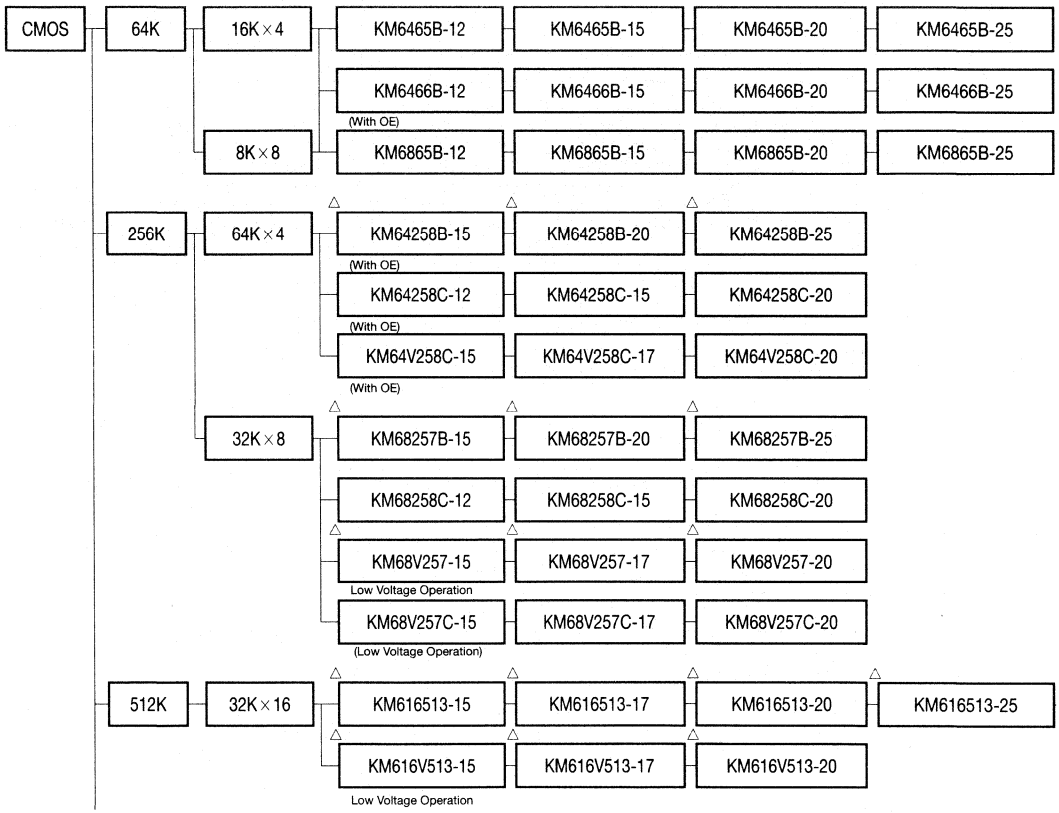
Standard SRAM

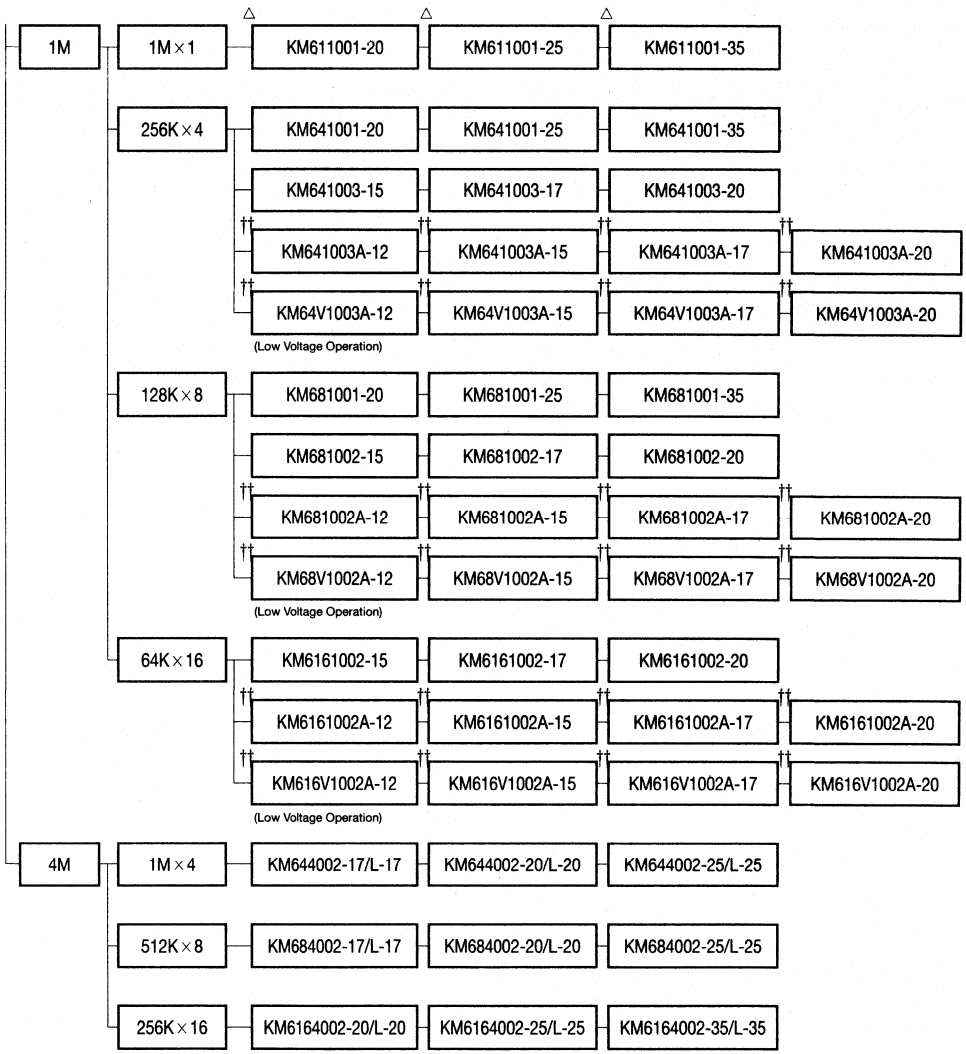


Pseudo SRAM

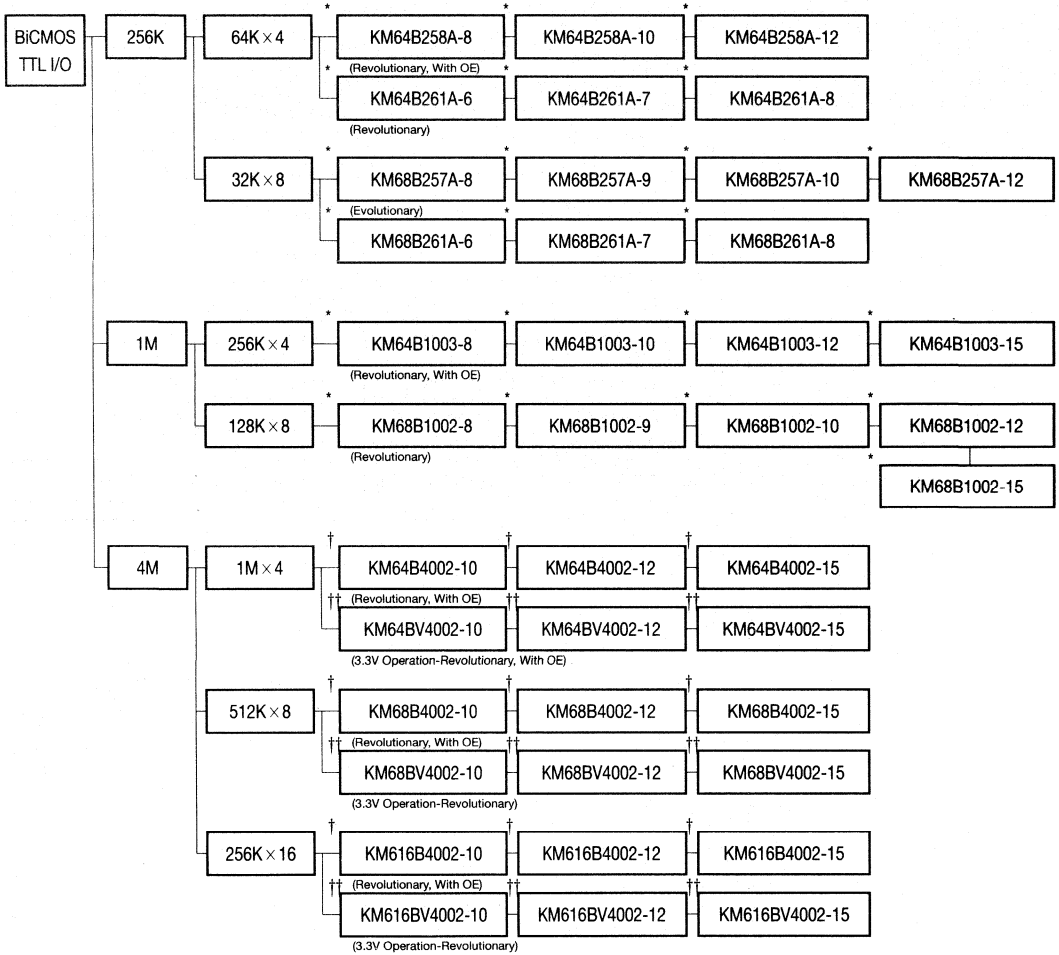


High Speed SRAM

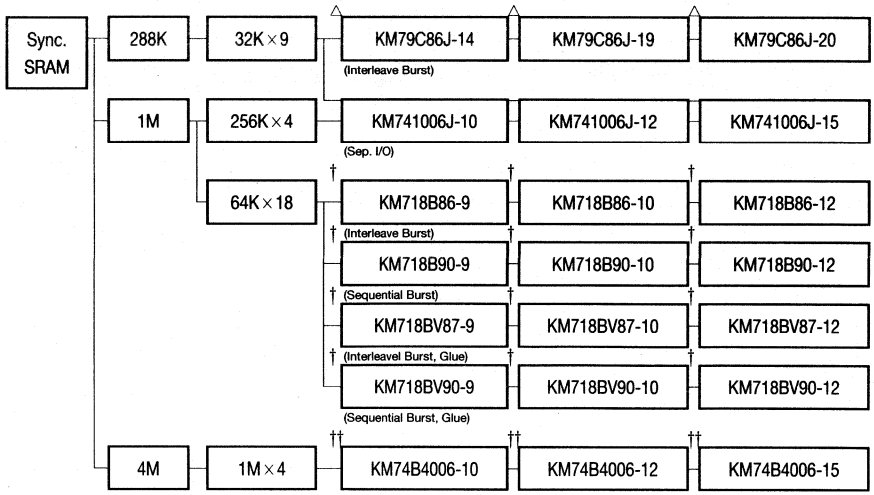



△
△
△
1M
1M×1
KM611001-20
KM611001-25
KM611001-35
256K×4
KM641001-20
KM641001-25
KM641001-35
KM641003-15
KM641003-17
KM641003-20
††
KM641003A-12
KM641003A-15
KM641003A-17
KM641003A-20
KM64V1003A-12
KM64V1003A-15
KM64V1003A-17
KM64V1003A-20
(Low Voltage Operation)
128K×8
KM681001-20
KM681001-25
KM681001-35
KM681002-15
KM681002-17
KM681002-20
KM681002A-12
KM681002A-15
KM681002A-17
KM681002A-20
KM68V1002A-12
KM68V1002A-15
KM68V1002A-17
KM68V1002A-20
(Low Voltage Operation)
64K×16
KM6161002-15
KM6161002-17
KM6161002-20
KM6161002A-12
KM6161002A-15
KM6161002A-17
KM6161002A-20
KM616V1002A-12
KM616V1002A-15
KM616V1002A-17
KM616V1002A-20
(Low Voltage Operation)
4M
1M×4
KM644002-17/L-17
KM644002-20/L-20
KM644002-25/L-25
512K×8
KM684002-17/L-17
KM684002-20/L-20
KM684002-25/L-25
256K×16
KM6164002-20/L-20
KM6164002-25/L-25
KM6164002-35/L-35

BiCMOS SRAM


BiCMOS TTL I/O
256K
64K×4
KM64B258A-8
KM64B258A-10
KM64B258A-12
(Revolutionary, With OE)
KM64B261A-6
KM64B261A-7
KM64B261A-8
(Revolutionary)
32K×8
KM68B257A-8
KM68B257A-9
KM68B257A-10
KM68B257A-12
(Evolutionary)
KM68B261A-6
KM68B261A-7
KM68B261A-8
1M
256K×4
KM64B1003-8
KM64B1003-10
KM64B1003-12
KM64B1003-15
(Revolutionary, With OE)
128K×8
KM68B1002-8
KM68B1002-9
KM68B1002-10
KM68B1002-12
(Revolutionary)
KM68B1002-15
4M
1M×4
KM64B4002-10
KM64B4002-12
KM64B4002-15
(Revolutionary, With OE)
KM64BV4002-10
KM64BV4002-12
KM64BV4002-15
(3.3V Operation-Revolutionary, With OE)
512K×8
KM68B4002-10
KM68B4002-12
KM68B4002-15
(Revolutionary, With OE)
KM68BV4002-10
KM68BV4002-12
KM68BV4002-15
(3.3V Operation-Revolutionary)
256K×16
KM616B4002-10
KM616B4002-12
KM616B4002-15
(Revolutionary, With OE)
KM616BV4002-10
KM616BV4002-12
KM616BV4002-15
(3.3V Operation-Revolutionary)

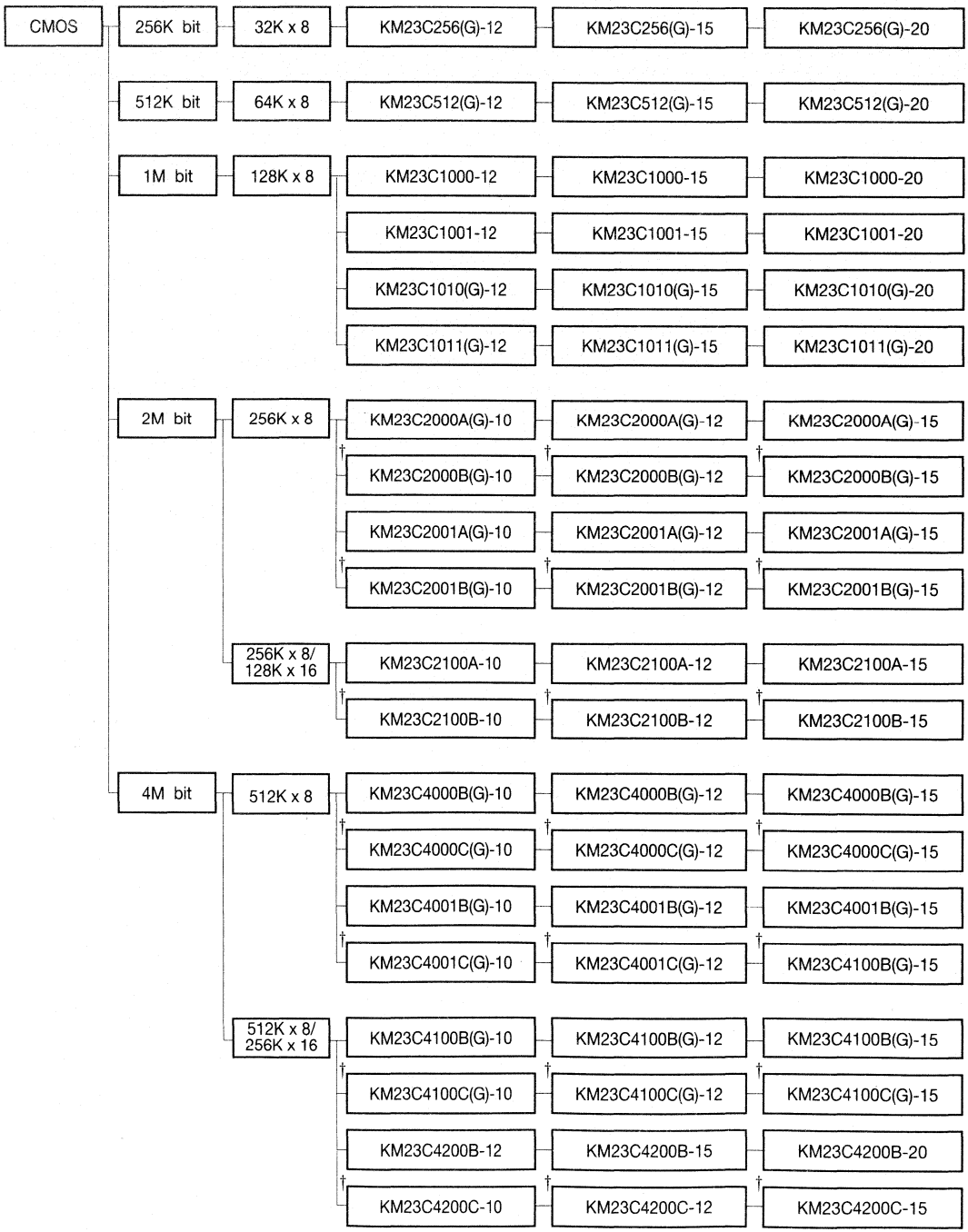
Specialty SRAM

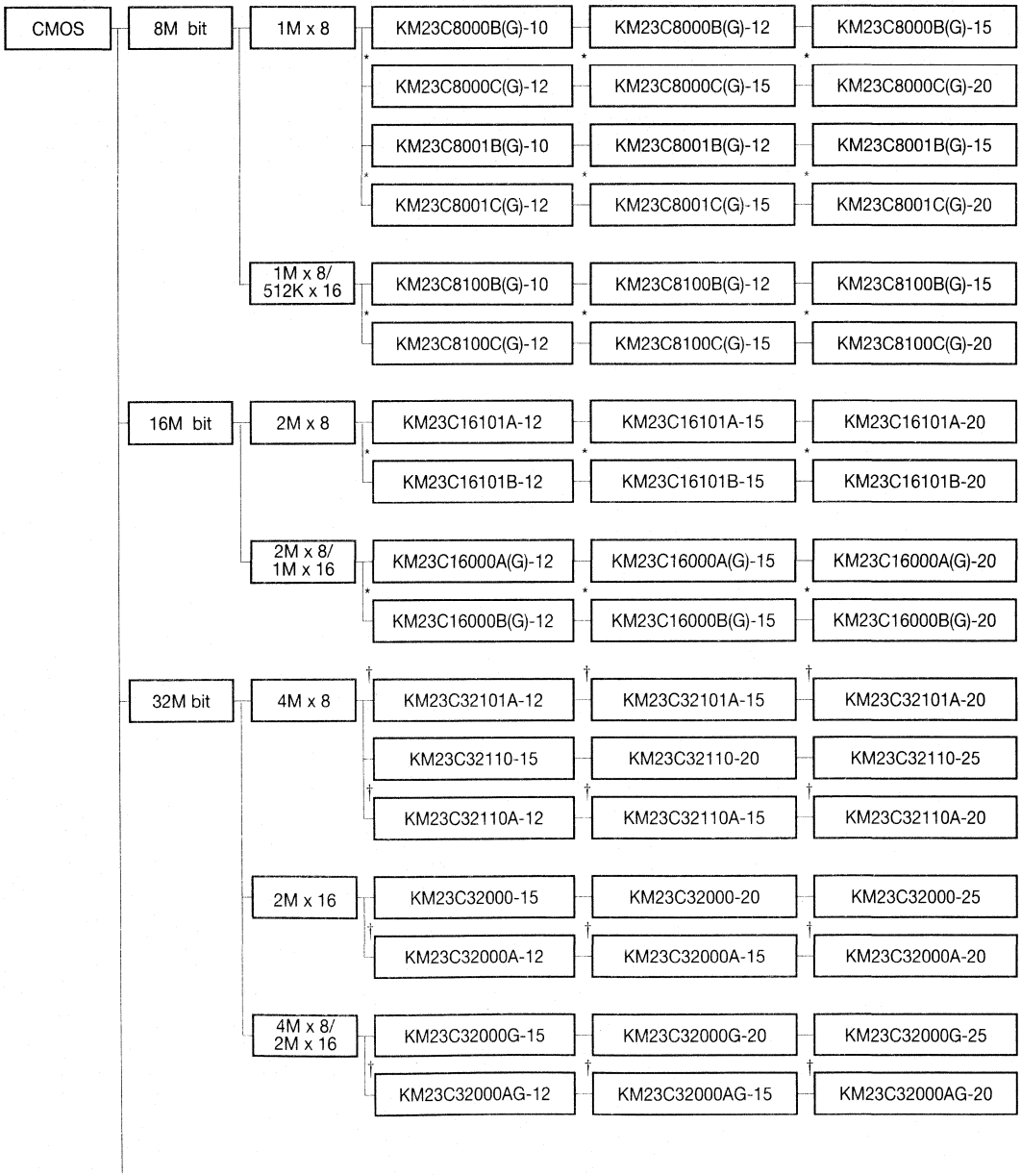


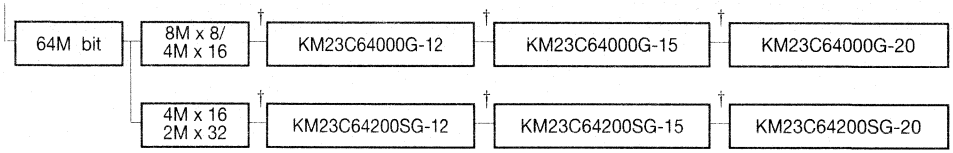
* : New Product † : Preliminary Product †† : Advanced Information △ : Last Time by Product

1.5 MASK ROM

Standard Product

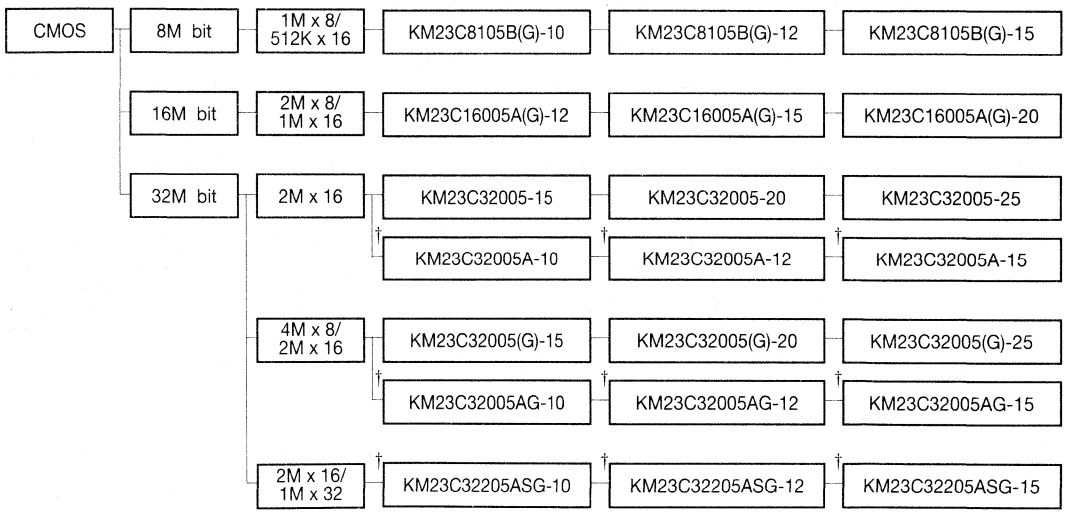



CMOS
8M bit
1M x 8
KM23C8000B(G)-10
KM23C8000B(G)-12
KM23C8000B(G)-15
KM23C8000C(G)-12
KM23C8000C(G)-15
KM23C8000C(G)-20
KM23C8001B(G)-10
KM23C8001B(G)-12
KM23C8001B(G)-15
KM23C8001C(G)-12
KM23C8001C(G)-15
KM23C8001C(G)-20
1M x 8/ 512K x 16
KM23C8100B(G)-10
KM23C8100B(G)-12
KM23C8100B(G)-15
KM23C8100C(G)-12
KM23C8100C(G)-15
KM23C8100C(G)-20
16M bit
2M x 8
KM23C16101A-12
KM23C16101A-15
KM23C16101A-20
KM23C16101B-12
KM23C16101B-15
KM23C16101B-20
2M x 8/ 1M x 16
KM23C16000A(G)-12
KM23C16000A(G)-15
KM23C16000A(G)-20
KM23C16000B(G)-12
KM23C16000B(G)-15
KM23C16000B(G)-20
32M bit
4M x 8
KM23C32101A-12
KM23C32101A-15
KM23C32101A-20
KM23C32110-15
KM23C32110-20
KM23C32110-25
KM23C32110A-12
KM23C32110A-15
KM23C32110A-20
2M x 16
KM23C32000-15
KM23C32000-20
KM23C32000-25
KM23C32000A-12
KM23C32000A-15
KM23C32000A-20
4M x 8/ 2M x 16
KM23C32000G-15
KM23C32000G-20
KM23C32000G-25
KM23C32000AG-12
KM23C32000AG-15
KM23C32000AG-20

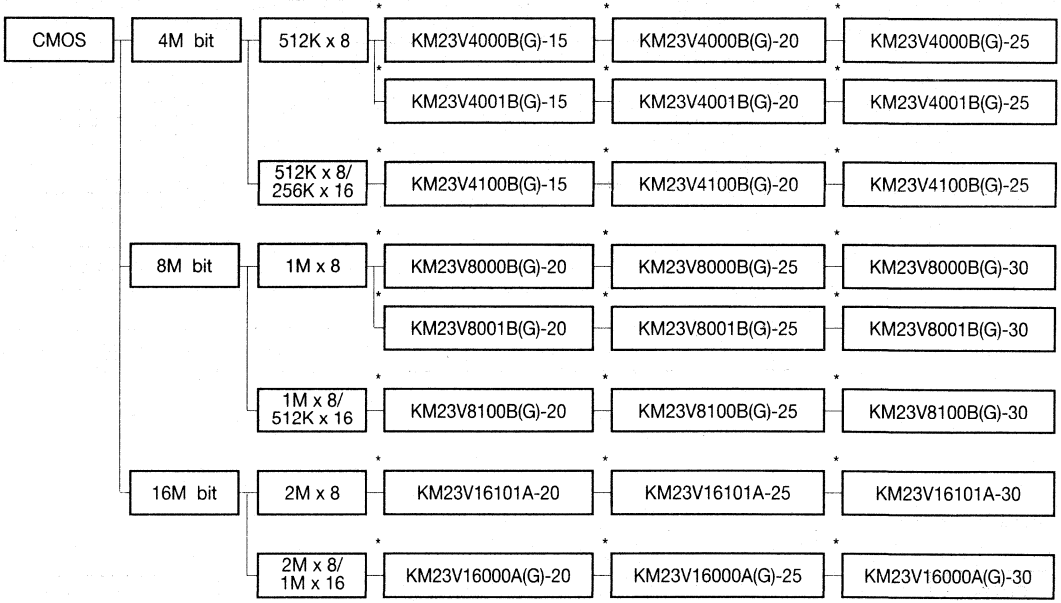


* : New Product
† : Under Development

Page Mode Product



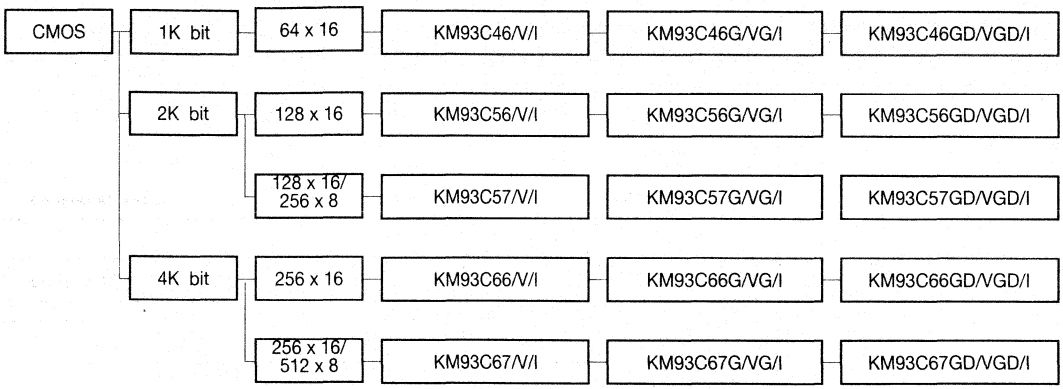
Low Voltage Product



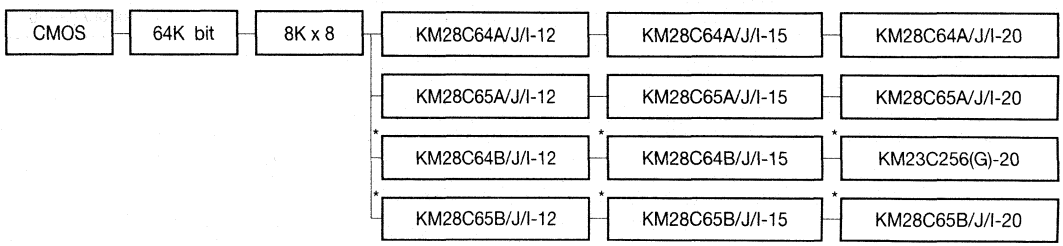
* : New Product
† : Under Development

1.6 EEPROM

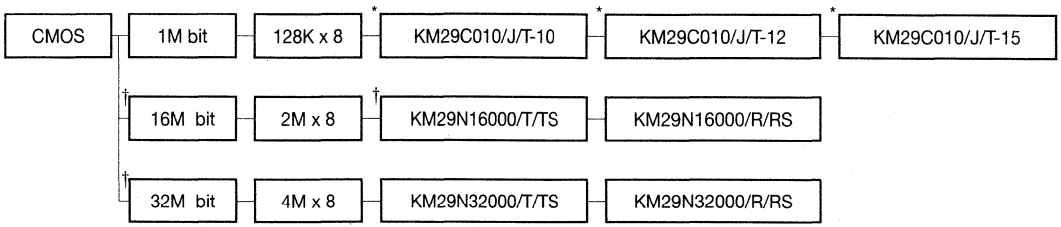
***Serial EEPROM**



***Parallel EEPROM**



1.7 Flash



* : New Product
† : Preliminary Product

2. PRODUCT GUIDE

2.1 Dynamic RAM

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
1M bit	1Mx1	5V±10%	KM41C1000C# KM41C1000CL# KM41C1000CSL#	60/70/80	Fast Page	P:18 Pin DIP J:20 Pin SOJ Z:20 Pin ZIP V:20 Pin TSOP-I (Forward) VR:20 Pin TSOP-I (Reverse) T:20 Pin TSOP-II (Forward) TR:20 Pin TSOP-II (Reverse
	256Kx4	5V±10%	KM44C256C# KM44C256CL# KM44C256CSL#	60/70/80	Fast Page	
4M bit	4Mx1	5V±10%	KM41C4000C# KM41C4000CL# KM41C4000CSL#	50/60/70/80	Fast Page	P:20 Pin DIP J:20 Pin SOJ Z:20 Pin ZIP V:20 Pin TSOP-I (Forward) VR:20 Pin TSOP-I (Reverse) T:20 Pin TSOP-II (Forward) TR:20 Pin TSOP-II (Reverse
			KM41C4002C#		Static Column	
		3.3V±10%	KM41V4000C# KM41V4000CL# KM41V4000CLL#	60/70/80	Fast Page	
	1Mx4	5V±10%	KM44C1000C# KM44C1000CL# KM44C1000CSL#	50/60/70/80	Fast Page	
			KM44C1010C#		Fast Page with WPB	
			KM44C1002C#		Static Column	
			KM44C1003C#		Quad CAS	
			KM44C1003CL# KM44C1003CSL#			
			KM44C1004C#		EDO	
			KM44C1004CL# KM44C1004CSL#			
		3.3V±10%	KM44V1000C# KM44V1000CL# KM44V1000CLL#	60/70/80	Fast Page	
			KM44V1004C#		EDO	
			KM44V1004CL# KM44V1004CLL#			
4M B/W	512Kx8	5V±10%	KM48C512B# KM48C512BL#	50/60/70/80	Fast Page	

Dynamic RAM

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
4M B/W	512Kx8	5V±10%	KM48C512BLL#	50/60/70/80	Fast Page	J:28 Pin SOJ Z:28 Pin ZIP T:28 Pin TSOP-II (Forward) TR:28 Pin TSOP-II (Reverse)
			KM48C514B#		EDO	
			KM48C514BL#			
			KM48C514BLL#			
		3.3V±10%	KM48V512B#	60/70/80	Fast Page	
			KM48V512BL#			
			KM48V512BLL#			
			KM48V514B#		EDO	
			KM48V514BL#			
			KM48V514BLL#			
	512Kx9	5V±10%	KM49C512B#	60/70/80	Fast Page	
			KM49C512BL#			
			KM49C512BLL#			
	256Kx16	5V±10%	KM416C256B#	50/60/70/80	Fast Page	
			KM416C256BL#			
			KM416C256BLL#			
			KM416C254B#		EDO	
			KM416C254BL#			
			KM416C254BLL#			
			KM416C156B#		Fast Page with 2WE	
			KM416C156BL#			
			KM416C156BLL#			
			KM416C157B#			
			KM416C157BL#			
			KM416C157BLL#			
		3.3V±10%	KM416V256B#	60/70/80	Fast Page	
			KM416V256BL#			
			KM416V256BLL#			
			KM416V254B#		EDO	
			KM416V254BL#			
			KM416V254BLL#			
	256Kx18	5V±10%	KM418C256B#	60/70/80	Fast Page	
			KM418C256BL#			
			KM418C256BLL#			
16M bit	16Mx1	5V±10%	KM41C16000A#	50/60/70/80	Fast Page(4K)	J:24 Pin SOJ (400mil) T:24 Pin TSOP-II (Forward) (400mil)
			KM41C16000AL#			
			KM41C16000ALL#			
			KM41C16000ASL#			

Dynamic RAM

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
16M bit	16Mx1	5V±10%	KM41C16002A#	50/60/70/80	Static Column(4K)	TR:24 Pin TSOP-II (Reverse) (400mil) K: 24 Pin SOJ (300mil) S: 24 Pin TSOP-II(Forward) (300mil) SR: 24 Pin TSOP-II(Reverse) (300mil)
		3.3V±10%	KM41V16000A#	60/70/80	Fast Page(4K)	
			KM41V16000AL#			
			KM41V16000ALL#			
			KM41V16000ASL#			
	4Mx4	5V±10%	KM44C4000A#	50/60/70/80	Fast Page(4K)	
			KM44C4000AL#			
			KM44C4000ALL#			
			KM44C4000ASL#			
			KM44C4100A#		Fast Page(2K)	
			KM44C4100AL#			
			KM44C4100ALL#			
			KM44C4100ASL#			
			KM44C4002A#		Static Column(4K)	
			KM44C4102A#		Static Column(2K)	
			KM44C4003A#		Quad CAS(4K)	
			KM44C4003AL#			
			KM44C4003ALL#			
			KM44C4003ASL#			
			KM44C4103A#		Quad CAS(2K)	
			KM44C4103AL#			
			KM44C4103ALL#			
			KM44C4103ASL#			
			KM44C4004A#		EDO(4K)	
			KM44C4004AL#			
			KM44C4004ALL#			
			KM44C4004ASL#			
			KM44C4104A#		EDO(2K)	
			KM44C4104AL#			
			KM44C4104ALL#			
			KM44C4104ASL#			
			KM44C4010A#		Fast Page with WPB (4K)	
			KM44C4010AL#			
			KM44C4010ALL#			
			KM44C4010ASL#			
			KM44C4110A#		Fast Page with WPB (2K)	
			KM44C4110AL#			
			KM44C4110ALL#			
			KM44C4110ASL#			
			KM44C4005A#			
			KM44C4005AL#		EDO with Quad CAS (4K)	
			KM44C4005ALL#			

Dynamic RAM

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
16M bit	4Mx4	5V±10%	KM44C4005ASL#	50/60/70/80		J: 24 Pin SOJ (400mil) T:24 Pin TSOP-II (Forward) (400mil) TR:24 Pin TSOP-II (Reverse) (400mil) K: 24 Pin SOJ (300mil) S:24 Pin TSOP-II (Forward) (300mil) SR:24 Pin TSOP-II(Reverse) (300mil)
			KM44C4105A#		EDO with Quad CAS (2K)	
			KM44C4105AL#			
			KM44C4105ALL#			
			KM44C4105ASL#			
		3.3V±10%	KM44V4000A#	60/70/80	Fast Page(4K)	
			KM44V4000AL#			
			KM44V4000ALL#			
			KM44V4000ASL#			
			KM44V4100A#		Fast Page(2K)	
			KM44V4100AL#			
			KM44V4100ALL#			
			KM44V4100ASL#			
			KM44V4004A#		EDO(4K0	
			KM44V4004AL#			
			KM44V4004ALL#			
			KM44V4004ASL#			
			KM44V4104A#		EDO(2K)	
			KM44V4104AL#			
			KM44V4104ALL#			
			KM44V4104ASL#			
16M B/W	2Mx8	5V±10%	KM48C2000A#	50/ 60/70/80	Fast Page(4K)	J:28 Pin SOJ T:28 Pin TSOP-II (Forward) TR:24 Pin TSOP-II(Reverse)
			KM48C2000AL#			
			KM48C2000ALL#			
			KM48C2000ASL#			
			KM48C2100A#		Fast Page(2K)	
			KM48C2100AL#			
			KM48C2100ALL#			
			KM48C2100ASL#			
			KM48C2004A#		EDO(4K)	
			KM48C2004AL#			
			KM48C2004ALL#			
			KM48C2004ASL#			
			KM48C2104A#		EDO(2K)	
			KM48C2104AL#			
			KM48C2104ALL#			
			KM48C2104ASL#			

Dynamic RAM

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
16M B/W	2Mx8	3.3V±10%	KM48V2000A#	60/70/80	Fast Page(4K)	J:28 Pin SOJ
			KM48V2000AL#			T:28 Pin TSOP-II (Forward)
			KM48V2000ALL#			TR:28 Pin TSOP-II(Reverse)
			KM48V2100A#		Fast Page(2K)	
			KM48V2100AL#			
			KM48V2100ALL#			
			KM48V2004A#		EDO(4K)	
			KM48V2004AL#			
			KM48V2004ALL#			
			KM48V2104A#		EDO(2K)	
			KM48V2104AL#			
			KM48V2104ALL#			
	1Mx16	5V±10%	KM416C1000A#	60/70/80	Fast Page(4K)	J:42 Pin SOJ
			KM416C1000A#-L			T:44 Pin TSOP-II (Forward)
			KM416C1000A#-F			R:44 Pin TSOP-II(Reverse)
			KM416C1200A#		Fast Page(1K)	
			KM416C1200A#-L			
			KM416C1200A#-F			
			KM416C1004A#		EDO(4K)	
			KM416C1004A#-L			
			KM416C1004A#-F			
			KM416C1204A#		EDO(1K)	
			KM416C1204A#-L			
			KM416C1204A#-F			
		3.3V±10%	KM416V1000A#	60/70/80	Fast Page(4K)	
			KM416V1000A#-L			
			KM416V1000A#-F			
			KM416V1200A#		Fast Page(1K)	
			KM416V1200A#-L			
			KM416V1200A#-F			

Dynamic RAM

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
16M B/W	1Mx16	3.3V±10%	KM416V1004A#	50/60/70	EDO(4K)	J:42 Pin SOJ
			KM416V1004A#-L			T:44 Pin TSOP-II (Forward)
			KM416V1004A#-F			R:44 Pin TSOP-II(Reverse)
			KM416V1204A#		EDO(1K)	
			KM416V1204A#-L			
			KM416V1204A#-F			
64M bit	8Mx8	3.3V±10%	KM48V8000#	50/60/70	Fast Page(8K)	J:34 Pin SOJ
			KM48V8000#-L			T:34 Pin TSOP-II (Forward)
			KM48V8000#-F			R:34 Pin TSOP-II(Reverse)
			KM48V8100#		Fast Page(4K)	
			KM48V8100#-L			
			KM48V8100#-F			
			KM48V8004#		EDO(8K)	
			KM48V8004#-L			
			KM48V8004#-F			
			KM48V8104#		EDO(4K)	
			KM48V8104#-L			
			KM48V8104#-F			

2.2 Dynamic RAM Module

Org.	Part No.	Feature	Speed(ns)	Package	PCB Height	Refresh cycle/ms	C/S
DRAM SIMM Based on 4M DRAM							
1Mx8	KMM581000CN	F/P	60/70/80	S, 30 Pin SIMM	650	1024/16	NOW
1Mx9	KMM591000CN	F/P	60/70/80	S, 30 Pin SIMM	650	1024/16	NOW
4Mx8	KMM584000C	F/P	60/70/80	S, 72 Pin SIMM	805	1024/16	NOW
4Mx9	KMM594000C	F/P	60/70/80	S, 72 Pin SIMM	805	1024/16	NOW
1Mx32	KMM5321000CV/CVG	F/P	50/60/70/80	S, 72 Pin SIMM	855	1024/16	NOW
1Mx33	KMM5331000C/CG	F/P	60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
1Mx36	KMM5361000C2/C2G	F/P, PLCC	60/70/80	S, 72 Pin SIMM	1000	1024/16	NOW
1Mx36	KMM5361000CH	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	1024/16	NOW
1Mx36	KMM5361003C/CG	F/P, QCAS	50/60/70/80	S, 72 Pin SIMM	1000	1024/16	NOW
1Mx40	KMM5401000C/CG/CM	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	1024/16	NOW
2Mx32	KMM5322000CV/CVG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
2Mx36	KMM5362000C2/C2G	F/P, PLCC	60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
2Mx36	KMM5362000CH	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
2Mx36	KMM5362003C/CG	F/P, QCAS	50/60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
2Mx40	KMM5402000C/CG/CM	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
4Mx32	KMM5324000CV/CVG	Double Nocth	50/60/70/80	D, 72 Pin SIMM	1290	1024/16	NOW
4Mx33	KMM5334000CV/CVG	Double Nocth	50/60/70/80	D, 72 Pin SIMM	1290	1024/16	NOW
4Mx36	KMM5364000C/CG	Double Nocth	50/60/70/80	D, 72 Pin SIMM	1290	1024/16	NOW
DRAM SIMM Based on 4M B/W DRAM							
256Kx32	KMM532256BW/BWG	F/P	60/70/80	S, 72 Pin SIMM	1000	512/8	NOW
256Kx36	KMM536256BW/BWG	F/P	60/70/80	S, 72 Pin SIMM	1000	512/8	NOW
512Kx32	KMM532512BW/BWG	F/P	60/70/80	D, 72 Pin SIMM	1000	512/8	NOW
512Kx36	KMM536512BW/BWG	F/P	60/70/80	D, 72 Pin SIMM	1000	512/8	NOW
DRAM SIMM Based on 16M DRAM							
4Mx8	KMM584100AN	F/P	50/60/70/80	S, 30 Pin SIMM	650	2048/32	NOW
4Mx8	KMM584100AKN	F/P	50/60/70/80	S, 30 Pin SIMM	650	2048/32	'94, 4Q
4Mx9	KMM594100AN	F/P	50/60/70/80	S, 30 Pin SIMM	650	2048/32	NOW
4Mx9	KMM594100AN	F/P	50/60/70/80	S, 30 Pin SIMM	650	2048/32	'94, 4Q
16Mx8	KMM5816000A/AT	F/P	50/60/70/80	D, 30 Pin SIMM	900	4096/64	NOW
16Mx8	KMM5816000AK	F/P	50/60/70/80	D, 30 Pin SIMM	900	4096/64	'94, 4Q
16Mx9	KMM5916000A/AT	F/P	50/60/70/80	D, 30 Pin SIMM	900	4096/64	NOW
16Mx9	KMM5916000AK	F/P	50/60/70/80	D, 30 Pin SIMM	900	4096/64	'94, 4Q
4Mx32	KMM5324100AV/AVG	F/P	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	NOW
4Mx32	KMM5324000AV/AVG	F/P	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	NOW
4Mx32	KMM5324100AK/AKG	F/P	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	NOW
4Mx32	KMM5324000AK/AKG	F/P	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	NOW
4Mx33	KMM5334100A/AG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW

2.2 Dynamic RAM Module (Continued)

Org.	Part No.	Feature	Speed(ns)	Package	PCB Height	Refresh cycle/ms	C/S
DRAM SIMM Based on 16M DRAM							
4Mx36	KMM5364100A/AG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW
4Mx36	KMM5364100A1/A1G	F/P	50/60/70/80	S, 72 Pin SIMM	1250	2048/32	NOW
4Mx36	KMM5364100AH/AHG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	NOW
4Mx36	KMM5364000AH/AHG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	NOW
4Mx36	KMM5364100AKH/AKHG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	'94, 4Q
4Mx36	KMM5364000AKH/AKHG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	'94, 4Q
4Mx36	KMM5364103AK/AKG	F/P, QCAS	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	NOW
4Mx36	KMM5364003AK/AKG	F/P, QCAS	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	NOW
4Mx39	KMM5394100AM	F/P	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	NOW
4Mx39	KMM5394000AM	F/P	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	NOW
4Mx40	KMM5404100A/AG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	NOW
4Mx40	KMM5404000A/AG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	NOW
4Mx40	KMM5404100AK/AKG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	'94, 4Q
4Mx40	KMM5404000AK/AKG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	'94, 4Q
8Mx32	KMM5328100AV/AVG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW
8Mx32	KMM5328000AV/AVG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	4096/64	NOW
8Mx32	KMM5328100AK/AKG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW
8Mx32	KMM5328000AK/AKG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	4096/64	NOW
8Mx33	KMM5338100AKV/AKVG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW
8Mx36	KMM5368100A1/A1G	F/P	50/60/70/80	D, 72 Pin SIMM	1375	2048/32	NOW
8Mx36	KMM5368100AH/AHG	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1250	2048/32	NOW
8Mx36	KMM5368000AH/AHG	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1250	4096/64	NOW
8Mx36	KMM5368100AKH/AKHG	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	'94, 4Q
8Mx36	KMM5368000AKH/AKHG	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1000	4096/64	'94, 4Q
8Mx36	KMM5368103AK/AKG	F/P, QCAS	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW
8Mx36	KMM5368003AK/AKG	F/P, QCAS	50/60/70/80	D, 72 Pin SIMM	1000	4096/64	NOW
8Mx40	KMM5408100AK/AKG	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	'94, 4Q
8Mx40	KMM5408000AK/AKG	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1000	4096/64	'94, 4Q
DRAM SIMM Based on 16M B/W DRAM							
1Mx32	KMM5321200AW/AWG	F/P	60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
1Mx32	KMM5321000AW/AWG	F/P	60/70/80	D, 72 Pin SIMM	1000	4096/64	NOW
1Mx32	KMM5321203AW/AWG	F/P	60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
2Mx32	KMM5322200AW/AWG	F/P	60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
2Mx32	KMM5322000AW/AWG	F/P	60/70/80	D, 72 Pin SIMM	1000	4096/64	NOW
2Mx32	KMM5322103AU/AUG	F/P, QCAS	60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW
2Mx32	KMM5322208AU/AUG	F/P, AND	60/70/80	S, 72 Pin SIMM	1000	1024/16	NOW
2Mx36	KMM5362209AU/AUG	F/P, AND	60/70/80	S, 72 Pin SIMM	1000	1024/16	NOW

2.3 Video RAM

Capacity	Part Number	Orgnization	Speed(ns)	Technology	Features	Package	Remark
256K	KM424C64	64K×4	100/120	CMOS	M/F	24Pin DIP/ZIP	NOW
512K	KM428C64	64K×8	70/80/100	CMOS	M/F	40PIN SOJ	NOW
1M	KM424C256A	256K×4	60/70/80	CMOS	M/F	28Pin ZIP/SOJ	NOW
	KM424C257	256K×4	60/70/80	CMOS	E/F	28Pin ZIP/SOJ	NOW
	KM428C128	128K×8	60/70/80	CMOS	E/F	40Pin SOJ/TSOP-Ⅱ	NOW
2M	KM428C256	256K×8	60/70/80	CMOS	E/F	40Pin SOJ/TSOP-Ⅱ	NOW
	KM428V256	256K×8	70/80	CMOS	E/F(3.3V)	40Pin SOJ/TSOP-Ⅱ	NOW
	KM428C257	256K×8	60/70/80	CMOS	F/F	40Pin SOJ/TSOP-Ⅱ	NOW
	KM428C258	256K×8	60/70/80	CMOS	F/F	40Pin SOJ/TSOP-Ⅱ	NOW
4M	† KM4216C256	256K×16	60/70/80	CMOS	F/F	64Pin SSOP/TSOP-Ⅱ	2Q '94

* : New Product † : Under Development

2.4 Static RAM

Low power SRAM

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissipation		Package
					Active Max.(mA)	Standby Max.(μA)	
64K	KM6264BL/BL-L	8K x 8	70/100/120	CMOS	55	100/50	DIP/SDIP/SOP
256K	KM62256BL/BL-L	32K x 8	70/85/100/120	CMOS	70	100/20	DIP/SDIP/SOP/TSOP
	KM62256BLI/BLI-L	32K x 8	70/100	CMOS	70	100/20	DIP/SOP
	* KM62256CL/CL-L	32K x 8	55/70/85/100	CMOS	70	100/20	DIP/SDIP/SOP/TSOP
	* KM62256CLI/CLI-L	32K x 8	70/100	CMOS	70	100/20	SOP/TSOP
512K	KM68512L/L-L	64K x 8	70/85/100	CMOS	70	100/20	SOP/TSOP
	* KM68512AL/AL-L	64K x 8	55/70	CMOS	70	100/20	SOP/TSOP
1M	* KM681000BL/BL-L	128K x 8	55/70/85/100	CMOS	70	100/20	DIP/SOP/TSOP
	* KM681000BLI/BLI-L	128K x 8	70/100	CMOS	70	100/20	SOP/TSOP
4M	* KM684000L/L-L	512K x 8	55/70/85/100	CMOS	70	100/20	DIP/SOP/TSOP
	* KM684000LI/LI-L	512K x 8	70/85/100	CMOS	70	100/50	SOP/TSOP

Low Voltage SRAM

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissipation		Package
					Active Max.(mA)	Standby Max.(μA)	
256K	† KM62256CL-LV	32K x 8	70	CMOS	40	20/10	SOP/TSOP
1M	† KM68V1000BL/BL-L	128K x 8	70/100	CMOS	40	50/10	SOP/TSOP
4M	†† KM68V4000AL/AL-L	512K x 8	70/100/120	CMOS	70	50/10	SOP/TSOP
	†† KM616V4000AL/AL-L	256K x 16	70/100	CMOS	70	50/10	SOP/TSOP

Low Voltage SRAM

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissipation		Package
					Active Max.(mA)	Standby Max.(μA)	
1M	KM658128A/AL/AL-L	128K x 8	80/100/120	CMOS	70	100/20	DIP/SOP

* : New Product † : Preliminary Product †† : Under Development △ : Last Time by Product

High speed & Ultra High Speed SRAM

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissipation		Package
					Active Max.(mA)	Standby Max.(μA)	
64K	KM6465B	16K x 4	12/15/20/25	CMOS	140	1	22 SDIP
	KM6466B	16K x 4	12/15/20/25	CMOS	140	1	24 SDIP/SOJ
	KM6865B	8K x 8	12/15/20/25	CMOS	140	1	28 SDIP/SOJ
256K	△ KM64258B	64K x 4	15/20/25	CMOS	140	2	28 SDIP/SOJ
	KM64258C	64K X 4	12/15/20	CMOS	140	2	28 SOJ
	KM64V258C	64K x 4	15/17/20	CMOS	110	2	28 DIP/SOJ
	* KM64B261A	64K x 4	6/7/8	BiCMOS	160	20	28 SOJ
	* KM64B258A	64K x 4	8/10/12	BiCMOS	185	20	28 SOJ
	△ KM68257B	32K X 8	15/20/25	CMOS	150	2	28 DIP/SOJ
	KM68257C	32K X 8	12/15/20	CMOS	150	2	28 DIP/SOJ
	KM68V257C	32K X 8	15/17/20	CMOS	110	2	28 DIP/SOJ
	* KM68B261A	32K x 8	6/7/8	CMOS	170	20	32 SOJ
	* KM68B257A	32K x 8	8/10/12	CMOS	185	20	28 SOJ
	△ KM68V257	32K x 8	20/25/35	CMOS	90	0.1	28 DIP/SOJ
1M	△ KM611001	1M x 1	20/25/35	CMOS	130	2	28 DIP/SOJ
	KM641001	256K x 4	17/20/25/35	CMOS	150	2	28 SDIP/SOJ
	KM641003	256K x 4	15/17/20	CMOS	170	10	32 SOJ
	†† KM641003A	256K x 4	12/15/17/20	CMOS	185	3/0.2	32 SOJ/TSOP(II)
	†† KM64V1003A	256K x 4	12/15/17/20	CMOS	95	2/0.1	32 SOJ/TSOP(II)
	* KM64B1003	256K x 4	8/10/12/15	BiCMOS	165	10	32 SOJ
	KM681001	128K x 8	20/25/35	CMOS	170	2	32 SDIP/SOJ
	KM681002	128K x 8	15/17/20	CMOS	170	10	32 SOJ/TSOP(II)
	†† KM681002A	128K x 8	12/15/17/20	CMOS	185	3/0.2	32 SOJ/TSOP(II)
	†† KM68V1002A	128K x 8	12/15/17/20	CMOS	95	2/0.1	32 SOJ/TSOP(II)
	* KM68B1002	128K x 8	8/9/10/12/15	BiCMOS	175	10	32 SOJ/TSOP(II)
	KM6161002	64K x 16	15/17/20	CMOS	230	10	44 SOJ/TSOP(II)
	†† KM6161002A	64K x 16	12/15/20	CMOS	250	3/0.2	44 SOJ/TSOP(II)
	†† KM616V1002A	64K x 16	13/15/17/20	CMOS	170	2/0.1	44 SOJ/TSOP(II)
4M	KM644002/L	1M x 4	17/20/25	CMOS	170	10/0.5	32 SOJ
	† KM68B4002	1M x 4	10/12/15	BiCMOS	180	60/30	32 SOJ
	†† KM68BV4002	1M x 4	12/15/20	BiCMOS	170	60/30	32 SOJ
	KM684002/L	512k x 8	17/20/25	CMOS	160	10/0.5	36 SOJ
	† KM68B4002	512K x 8	10/12/15	BiCMOS	200	60/30	36 SOJ
	†† KM68BV4002	512K x 8	12/15/20	BiCMOS	180	60/30	36 SOJ
	KM6164002/L	256K x 16	20/25/35	CMOS	160	10/0.5	44 SOJ
	† KM616B4002	256K x 16	10/12/15	BiCMOS	240	60/30	44 SOJ/54 SOJ
	†† KM616BV4002	256K x 16	12/15/20	BiCMOS	200	60/30	44 SOJ/54 SOJ

* : New Product † : Preliminary Product †† : Under Development △ : Last Time by Product

Specialty SRAM

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissipation		Package
					Active Max.(mA)	Standby Max.(μA)	
288K	△ KM79C86	32K x 9	14/19/24	CMOS	190	50	44 PLCC
1M	KM741006	256K x 4	6.5/7/8	CMOS	190	40	46 SOJ
	† KM718B86	64K x 18	9/10/12	BiCMOS	280	80	52 PLCC
	† KM718B91	64K x 18	9/10/12	BiCMOS	280	80	52 PLCC
	† KM718BV87	64K x 18	9/10/12	BiCMOS	280	80	52 PLCC
	† KM718BV91	64K x 18	9/10/12	BiCMOS	280	80	52 PLCC

* : New Product † : Preliminary Product †† : Under Development △ : Last Time by Product

2.5 MASK ROM

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Package	Remark
256K	KM23C256(G)	32K x 8	120/150/200	CMOS	Programmable CE & OE	28DIP(32SOP)	NOW
512K	KM23C512(G)	64K x 8	120/150/200	CMOS	Programmable CE & OE	28DIP(32SOP)	NOW
1M	KM23C1000	128K x 8	120/150/200	CMOS	Programmable CE	28DIP	NOW
	KM23C1001	128K x 8	120/150/200	CMOS	Programmable OE	28DIP	NOW
	KM23C1010(G)	128K x 8	120/150/200	CMOS	Programmable CE & OE	32DIP(32SOP)	NOW
	KM23C1011(G)	128K x 8	120/150/200	CMOS	Programmable OE	32DIP(32SOP)	NOW
2M	KM23C2000A(G)	256K x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	NOW
	KM23C2001A(G)	256K x 8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	NOW
	KM23C2100A	256K x 8/ 128K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP	NOW NOW
	† KM23C2000B(G)	256K x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	4Q.'94
	† KM23C2001B(G)	256K x 8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	4Q.'94
	† KM23C2100B	256K x 8/ 128K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP	4Q.'94
4M	KM23C4000B(G)	512K x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	NOW
	KM23C4001B(G)	512K x 8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	NOW
	KM23C4100B(G)	512K x 8/ 256K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(40SOP)	NOW
	KM23C4200B	512K x 8/ 256K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP	NOW
	† KM23C4000C(G)	512K x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	4Q.'94
	† KM23C4001C(G)	512K x 8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	4Q.'94
	† KM23C4100C(G)	512K x 8/ 256K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(40SOP)	4Q.'94
	† KM23C4200C	512K x 8/ 256K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP	4Q.'94
	* KM23V4000B(G)	512K x 8	150/200/250	CMOS	3.3V Operation	32DIP(32SOP)	NOW
	* KM23V4001B(G)	512K x 8	150/200/250	CMOS	3.3V Operation	32DIP(32SOP)	NOW
	* KM23V4100B(G)	512K x 8/ 256K x 16	150/200/250	CMOS	3.3V Operation	40DIP(40SOP)	NOW
8M	KM23C8000B(G)	1M x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	NOW
	KM23C8001B(G)	1M x 8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	NOW
	KM23C8100B(G)	1M x 8/ 512K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	42DIP(44SOP)	NOW
	* KM23C8000C(G)	1M x 8	120/150/200	CMOS	Programmable CE & OE	32DIP(32SOP)	NOW
	* KM23C8001C(G)	1M x 8	120/150/200	CMOS	Programmable OE	32DIP(32SOP)	NOW
	* KM23C8100C(G)	1M x 8/ 512K x 16	120/150/200	CMOS	Programmable CE & OE Word/Byte Mode	42DIP(44SOP)	NOW
	KM23C8105B(G)	1M x 8/ 512K x 16	100/120/150 (tP>50)	CMOS	4Word Page	42DIP(44SOP)	NOW
	* KM23V8000B(G)	1M x 8	200/250/300	CMOS	3.3V Operation	32DIP(32SOP)	NOW
	* KM23V8001B(G)	1M x 8	200/250/300	CMOS	3.3V Operation	32DIP(32SOP)	NOW
	* KM23V8100B(G)	1M x 8/ 512K x 16	200/250/300	CMOS	3.3V Operation	42DIP(44SOP)	NOW

2.5 MASK ROM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Package	Remark
16M	KM23C16101A KM23C16000A(G)	2M x 8 2M x 8/ 1M x 16	120/150/200 120/150/200	CMOS CMOS	Programmable OE Programmable CE & OE Word/Byte Mode	36DIP 42DIP(44SOP)	NOW NOW
	* KM23C16101B * KM23C16000B(G)	2M x 8 2M x 8/ 1M x 16	120/150/200 120/150/200	CMOS CMOS	Programmable OE Programmable CE & OE Word/Byte Mode	36DIP 42DIP(44SOP)	NOW NOW
	KM23C16005A(G)	2M x 8/ 1M x 16	120/150/200 (tP > 50)	CMOS	8Word Page	42DIP(44SOP)	NOW
	* KM23V16101A * KM23V16000A(G)	2M x 8 2M x 8/ 1M x 16	200/250/300 200/250/300	CMOS CMOS	3.3V Operation 3.3V Operation	36DIP 42DIP(44SOP)	NOW NOW
32M	KM23C32110 KM23C32000 KM23C32000G	4M x 8 2M x 16 4M x 8/ 2M x 16	150/200/250 150/200/250 150/200/250	CMOS CMOS CMOS	Programmable CE & OE Programmable CE & OE Programmable CE & OE	42DIP 42DIP(44SOP) 42DIP(44SOP)	NOW NOW NOW
	† KM23C32101A † KM23C32110A † KM23C32000A † KM23C32000AG	4M x 8 4M x 8 2M x 16 4M x 8/ 2M x 16	120/150/200 120/150/200 120/150/200 120/150/200	CMOS CMOS CMOS CMOS	Programmable OE Programmable CE & OE Programmable CE & OE Programmable CE & OE Word/Byte Mode	36DIP 42DIP 42DIP 44SOP	4Q.'94 4Q.'94 4Q.'94 4Q.'94
	KM23C32005 KM23C32005G	2M x 16 4M x 8/ 2M x 16	150/200/250 150/200/250	CMOS CMOS	8Word Page 8word Page	42DIP 44SOP	NOW NOW
	† KM23C32005AG	4M x 8/ 2M x 16	100/120/150 (tP > 30)	CMOS	8Word Page	44SOP	1Q.'95
	† KM23C32205ASG	2M x 16 1M x 32	100/120/150 (tP > 30)	CMOS	8word Page	70SSOP	2Q.'95
64M	† KM23C64000G	8M x 8/ 4M x 16	120/150/200	CMOS	Programmable CE & OE Word/Byte Mode	44SOP	3Q.95
	KM23C64200SG	4M x 16/ 2M x 32	120/150/200	CMOS	Programmable CE & OE	70SSOP	3Q.'95

* : New Product
† : Under Development

2.6 EEPROM

Density	Part Number	Organization	Speed(ns)	Technology	Features	Package	Remark
1K bit	KM93C46/G/GD/I	64×16	1MHz	CMOS	Self-timed	8DIP/8SOP	Now
	KM93C46V/VG/VGD/I	64×16	250KHz	CMOS	3.0V-Operation	8DIP/8SOP	Now
2K bit	KM93C56/G/GD/I	128×16	1MHz	CMOS	Auto Erase, Self-timed	8DIP/8SOP	Now
	KM93C57/G/GD/I	128×16/256×8	1MHz	CMOS	Select Organization	8DIP/8SOP	3Q,94
	KM93C56V/VG/VGD/I	128×16	1MHz	CMOS	3.0V Operation	8DIP/8SOP	Now
	KM93C57V/VG/VGD/I	128×16/256×8	1MHz	CMOS	3.0V Operation	8DIP/8SOP	Now
4K bit	KM93C66/G/GD/I	256×16	1MHz	CMOS	Auto Erase, Self-timed	8DIP/8SOP	Now
	KM93C67/G/GD/I	256×16/512×8	1MHz	CMOS	Select Organization	8DIP/8SOP	3Q,94
	KM93C66V/VG/VGD/I	256×16	1MHz	CMOS	3.0V Operation	8DIP/8SOP	Now
	KM93C67V/VG/VGD/I	256×16/512×8	1MHz	CMOS	3.0V Operation	8DIP/8SOP	Now
64K bit	KM28C64A/AJ	8K×8	120/150/200	CMOS	64B Page Mode, D-P, T-B	28DIP/32PLCC	Now
	KM28C64AI/AJI	8K×8	120/150/200	CMOS	Industrial	28DIP/32PLCC	Now
	KM28C65A/AJ	8K×8	120/150/200	CMOS	64B Page Mode, D-P, T-B R-B	28DIP/32PLCC	Now
	KM28C65AI/AJI	8K×8	120/150/200	CMOS	Industrial	28DIP/32PLCC	Now
	KM28C64B/BJ	8K×8	90/120/150	CMOS	64B Page Mode, D-P, T-B	28DIP/32PLCC	3Q,94
	KM28C64BII/BJI	8K×8	90/120/150	CMOS	Industrial	28DIP/32PLCC	3Q,94
	KM28C65B/BJ	8K×8	90/120/150	CMOS	64B Page Mode, D-P, T-B, R-B	28DIP/32PLCC	3Q,94
	KM28C65BI/BJI	8K×8	90/120/150	CMOS	Industrial	28DIP/32PLCC	3Q,94
1M bit	KM29C010/J/T	128K×8	100/120/150	CMOS	128B Page Mode, D-P, T-B	32DIP/32PLCC	Now
16M bit	KM29N16000T/TS	2M×8	t_R = 15 μs	CMOS	256B Page Mode	44(40)TSOP	3Q.94
	KM29N16000R/RS		t_{RC} = 80ns		4K Block Erase		
32M bit	KM29N32000T/TS	4M×8	t_R = 10 μs	CMOS	512B Page Mode	44(40)TSOP	2Q.94
	KM29N32000R/RS		t_{RC} = 50ns		8K Block Erase		

* D-P : Data-Polling, R/B : Ready/Busy, T-B : Toggle Bit

2.7 DRAM Card

Card Style	Vcc	Density	Part No.	Organization	Speed(ns)	PKG	Features
JEIDA/JEDEC	5.0V	2M Byte	KMCJ532512	512Kx32/1Mx16	60/70/80	88 Pin Two Piece	• Fast Page Mode Operation • Low Power Consumption • $\overline{RAS}$ only and Hidden Refresh • $\overline{CAS}$ before $\overline{RAS}$ Refresh
			KMCJ536512	512Kx36/1Mx18	60/70/80	88 Pin Two Piece	
		4M Byte	KMCJ5321000	1Mx32/2Mx16	60/70/80	88 Pin Two Piece	
			KMCJ5361000	1Mx36/2Mx18	60/70/80	88 Pin Two Piece	
		8M Byte	KMCJ5322000	2Mx32/4Mx16	60/70/80	88 Pin Two Piece	
			KMCJ5362000	2Mx36/4Mx18	60/70/80	88 Pin Two Piece	
		16M Byte	KMCJ5324000	4Mx32/8Mx16	60/70/80	88 Pin Two Piece	
			KMCJ5324100	4Mx32/8Mx16	60/70/80	88 Pin Two Piece	
			KMCJ5364100	4Mx36/8Mx18	60/70/80	88 Pin Two Piece	
	3.3V	2M Byte	KMCV532512	512Kx32/1Mx16	60/70/80	88 Pin Two Piece	
		4M Byte	KMCV5321000	1Mx32/2Mx16	60/70/80	88 Pin Two Piece	
		8M Byte	KMCV5322000	2Mx32/4Mx16	60/70/80	88 Pin Two Piece	
		16M Byte	KMCV5324000	4Mx32/8Mx16	60/70/80	88 Pin Two Piece	
			KMCV5324100	4Mx32/8Mx16	60/70/80	88 Pin Two Piece	

SRAM Card

Card Style	Vcc	Capacity	Part No.	Organization	Speed(ns)	PKG	Features
PCMCIA/JEIDA Standard	5.0V	512K Byte	KMCJ616256	256Kx16/512Kx8	150/200/250	68 Pin Two Piece	• 8KByte Attri bute Memory • Replaceable & Rechargeable Battery • High Speed : 150ns
		1M Byte	KMCJ616512	512Kx16/1Mx8	150/200/250	68 Pin Two Piece	
		2M Byte	KMCJ6161000	1Mx16/2Mx8	150/200/250	68 Pin Two Piece	

3.1 Video RAM

Density	Feature	Organization	Samsung	Micron	Toshiba	NEC	Hitachi	Ti
256K	Minimum	64K×4	KM424C64	MT42C4064		μPD41264 μPD42264	HM53461(2)	TMS4461
512K	Minimum	64K×8	KM428C64					
1M	Minimum	256K×4	KM424C256 KM424C256A		TC524256 TC524256A TC524256B TC524257	μPD42273	HM534251 HM534251A HM534252	TMS44C250 SMJ44C250
		128K×8			TC528126A TC528126B		HM538121 HM538121A	TMS48C121
	Extended	256K×4	KM424C257	MT42C4256 MT42C4255	TC524258A TC524258B TC524259B	μPD42274	HM534253A	TMS44C251 SMJ44C251 SMJ44C251A
		128K×8	KM428C128	MT42C8128 MT42C8128	TC528128A TC528128B TC528129B	μPD42275	HM538123A	
2M	Extended	256K×8	KM428C256	MT42C8255				
	Full	256K×8	KM428C257 KM428C258	MT42C8256 MT42C8254	TC528267	μPD482234 μPD482235	HM538253	
4M	Full	256K×32	KM4216C256	MT42C256K16A1				

3.2 Static RAM

Low power SRAM

Den.	Org.	SAMSUNG	HITACHI	SONY	TOSHIBA	MITSUBISHI	NEC
64K	8K x 8	KM6264BL/BL-L	HM6264A/AL/AL-L	CXK5864B-L/B-LL	TC6565AL/AL-L	M5M5165/L	μPD4364L/L-L
256K	32K x 8	KM62256CL/CL-L	HM62256AL/AL-L	CXK58257A-L/A-LL	TC55257BL/BL-L	M5M5255B-L/B-LL	μPD43256B/BL
512K	64K x 8	KM68512AL/AL-L					
1M	128K x 8	KM681000BL/BL-L	HM628128AL/AL-L	CXK581000/L	TC551001AL-AL-L	M5M51008/L	μPD431000AL/ALL
4M	512K x 8	KM628512	HM628512/L/L-L	CXK584000(1)-L	TC554002	M5M54008L/LL	μPD434000/L/LL

Low power SRAM

Den.	Org.	SAMSUNG	HITACHI	TSOHIBA	NEC	OKI	MOTOROLA
1M	128K x 8	KM658128A/AL/AL-L	HM658128A/AL/AL-L	TC518129A/AL/AL-L	μPD428128A/AL/AL-L	MSM548128	MCM518128

High Speed SRAM

Den.	Org.	Samsung	Hitachi	Cypress	Fujitsu	Micron	IDT	Motorola	Toshiba	sony
64K	16K x 4	KM6465B	HM6288	CY7C164A	MB81C74	MT5C6404	IDT7188	MCM6288C	TC55416	CXK5466
	16Kx4(With OE)	KM6466B	HM6289	CY7C166A	MB81C75	MT5C6405	IDT6198		TC55417	CXK5465
	8K X 8	KM6865B		CY7C186A	MB81C78	MT5C6408	IDT7164	MCM6264C	TC5588	CXK5863
256K	64K X 4(5V)	KM64458C	HM67909A	CY7C196	MB81C84A	MT5C2565	IDT61298SA	MCM629C	TC55464A	
	64K X 4(3.3V)	KM64B258C				MT5LC2565				
	32K X 8(5V)	KM68257C	HM62832H	CY7C199		MT5C2568	IDT71256SA	MCM6206D	TC55328A	CXK58258B
	32K x 8(3.3V)	KM68V257C				MT5LC2568	IDT713256	MCM62V06D	TC55V328	
1M	1M x 1(E)	KM11001		CY7C1007		MT5C1001	IDT71281	MCM6227B		
	256K x 4(E)	KM641001	HM624256A	CY7C1006		MT5C1005	IDT71028	MCM6229A		CXK541000
	256K x 4(R)	KM641003	HM674256UH			MT5C256K4A1				
	128K x 8(E)	KM681001	HM6268127H	CY7C1009	MB82008	MT5C1008	IDT71024	MCM6226B		CXK541020
	128K x 8(R)	KM681002				MT5C128K8A1				
	64K x 16(R)	KM6161002		CY7C108		MT5C64K16A1			TC551664	
4M	1M x 4	KM644002	HM624100		MB82201	MT5C1M4B2			TC551402	
	512K x 8	KM684002				MT5C512K8B2				
	256K x 16	KM6164002				MT5C256KX16				

BiCMOS SRAM

Den.	Org.	Samsmung	Hitachi	NEC	Toshiba	Motorola	IDT
256K	64K x 4(With OE)-R	KM64B261A				MCM6709R	
	64K x 4(with-OE)-E	KM64B258A	HM6709SH		TC55B465	MCM6709A	IDT61B298
	32K x 8-R	KM68B261A		μPD46258		MCM6706R	
	32K x 8-E	KM68B257A	HM6783SH		TC55B328	MCM6706A	IDT71256
1M	256K x 4(With OE)-R	KM64B1003			TC55B4257	MCM6729A	
	128K x 8-R	KM68B1002			TC55B8128	MCM6726A	IDT71B024

Specialty SRAM

Den.	Org.	SMAMSUNG	Motorola	Micron	Cypress	ICW
1M	256K x 4	KM741006	MCM67Q804			
	64K x 18	KM718B86	MCM67B618		CY7C1031	ICW73B596
		KM718B90		MT58LC64K18M1		
		KM718BV87	MCM67H618	MT58LC64K18B2		
		KM718BV90		MT58LC64K18M1		

3.3 MASK ROM

DTY	Samsung	NEC	Hitachi	Toshiba	Sharp	Mitsubishi	Fujitsu	Sony
256K	KM23C256		HN623257P HN623258P		LH23255 LH53259	M5M23256P	MB83256	CXK38256
512K	KM23C512			TC53512C	LH53514 LH53515		MB83512	
1M	KM23C1000	uPD23C1000A	HN62321P HN62321BP HN62331P	TC531000C	LH231000B LH531000A	M5M23C100 M5M231000	MB831000 MB831124	CXK381000P
	KM23C1001	uPD23C1010A	HN62321EP HN62331EP			M5M231001		
	KM23C1010	uPD23C1001E	HN62321A	TC531001C	LH231100B			
		uPD23C1000E	HN62331A		LH530800			
	KM23C1011	uPD23C100EA			LH530900			
2M	KM23C2000A	uPD23C2001	HN62302B	TC532000A	LH532300 LH532100B		MB832000 MB832001	CXK382001
	KM23C2001A				LH532200B LH532400			
	KM23C2100A	uPD23C2000	HN62412P		LH532000B			
		uPD23C2000A	HN62422P		LH532500			
4M	KM23C4000B	uPD23C4001E	HN62335 HN62344B	TC534000A	LH534100B	M5M23C401AP	MB834000A	CXK384001
	KM23C4000C		HN62335 HN62344B				MB834000AL	
	KM23V4001B		HN62W335B					
	KM23C4001B				LH534300 LH534400			
	KM23C4001C				LH534300 LH534400			
	KM23C4100B	uPD23C4000	HN62404P	TC534200	LH534000B	M5M23C400AP	MB834100A	
		uPD23C4000A	HN62414P HN62424P HN62444P		LH534500'		MB834200A	
	KM23C4100C	uPD23C4000	HN62404P		LH534000B		MB834100AL	
		uPD23C4000A	HN62414P HN62424P HN62444P		LH534500			
	KM23V4100B KM23C4200B KM23C4200C		HNW15					

3.3 MASK ROM (Continued)

DTY	Samsung	NEC	Hitachi	Toshiba	Sharp	Mitsubishi	Fujitsu	Sony
8M	KM23C8000B	uPD23C8001E	HN62318B	TC538000A	LH538100 LH538200	M5M23801P	MB838000	CXK388000
	KM23C8000C	uPD23C8001E	HN62318B		LH538100 LH538200	M5M23801P	MB838000	
	KM23V8000B		HN62W328B					
	KM23C8001B							
	KM23C8001C							
	KM23V8001B							
	KM23C8100B	uPD23C8000	HN62418P	TC538200A	LH538000	M5M23800P	MB838200	
	KM23C8100C	uPD23C8000	HN62428P	TC538200A	LH538000	M5M23800P		
	KM23C8105B							
	KM23V8100B						MB838200L	
16M	KM23C16101A							
	KM23C16101B							
	KM23V16101A							
	KM23C16000A	uPD23C16000	HN624316P	TC5316200A	LH53160000	M5M23160P	MB831620P	
	KM23C16000B	uPD23C16000	HN624316P	TC5316200A	LH53160000	M5M23160P	MB831620P	
	KM23C16005A					M5M23168P		
	KM23V16000A		HN62W4116					
32M	KM23C32000	uPD23C32000			LH5332000			
	KM23C32000A	uPD23C32000			LH5332000			
	KM23C32005							
	KM23C32005A							
	KM23C32205A							

3.4 EEPROM

***Serial I/O EEPROM**

Density	Samsung	N. S	Exar	Micro Chip	SGSThomson	Catalyat	Rohm	Atmel
1K	KM93C46	NM9346	XRM93C46A	93C46	ST93C46T	CAT93C46A	BR93C46	AT93C46
	KM93C46V	NM93C46L						
2K	KM93C56	NM93C56A	XRM93C56A				BR93C56A	AT93C56
	KM93C57			93C56	ST93C56	CAT36C102		
	KM93C56V	NM93C56L					BR93C56B	
	KM93C57V							
4K	KM93C66	NM93C66	XRM93C66B				BR93C66A	AT93C66
	KM93C67			93C66		CAT35C104		
	KM93C66V	NM93C66L					BR93C66B	
	KM93C67V					CAT33T104		

***Parallel EEPROM**

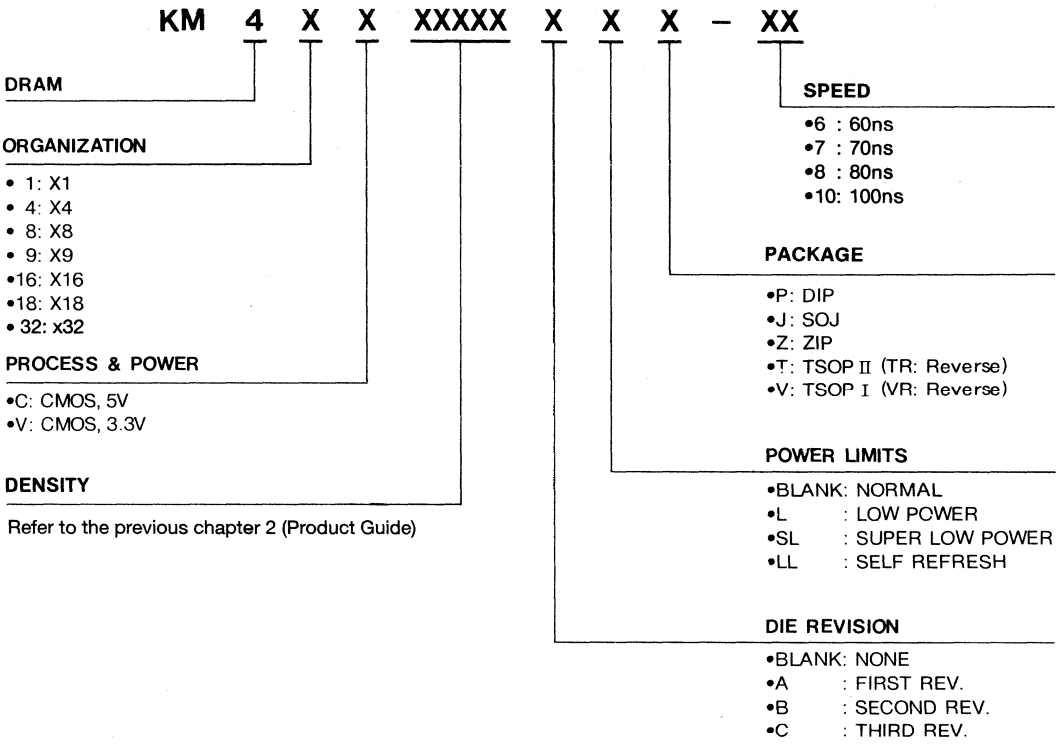
Density	Samsung	Xicor	Seeq	Exel	Atmel	Hitachi	Oki	Catalyat
64K	KM28C64A	X2864A/B X28C64	DQ28C64	XL2864 XL28C64A	AT28C64	HN58064	MSM28C64A	CAT28C65A
	KM28C65A		DQ28C65 DQ2864	XL2865 XL28C65A		HN58C65/66		CAT28C65A
	KM28C64B	X2864A/B X28C64	DQ28C64	XL2864 XL28C64A	AT28C64	HN58064	MSM28C64A	CAT28C65A
	KM28C65B		DQ28C65 DQ2864	XL2865 XL28C65A		HN58C65/66		CAT28C65A

3.5 Flash

Density	Samsung	Toshiba	Seeq	Exel	Atmel	Hitachi	Oki	Catalyat
1M	KM29C010				AT29C010			
16M	KM29N16000	TC5816FT/TR						
32M	KM29N32000	TC5832FT/TR						

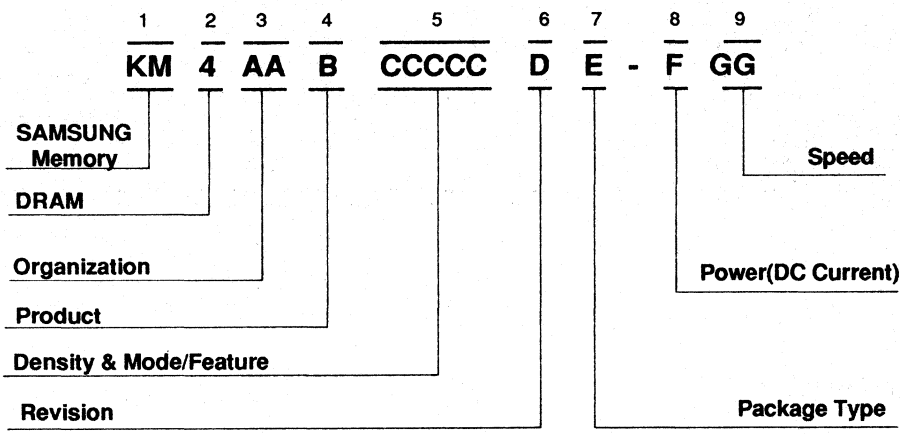
4. ORDERING INFORMATION

4.1 DRAM



* NEW DRAM ORDERING SYSTEM

This new DRAM ordering system will be used for all SAMSUNG's DRAM products in '95.
In '94 DRAM Databook, only used for 16M Byte Word Wide 2nd Gen. and 64M DRAM.



1. SAMSUNG Memory

2. DRAM(4)

3. Organization

1	x 1
4	x 4
8	x 8
9	x 9
16	x 16
18	x 18
32	x 32

4. Product

C	5V
V	3.3V

5. Density & Mode/Feature (Same)

6. Revision

Blank	1st Gen.
A	2nd Gen.
B	3rd Gen.
C	4th Gen.

7. Package Type

J	SOJ
T	TSOP II (Forward)
R	TSOP II (Reverse)
V	TSOP I (Forward)
U	TSOP I (Reverse)
K	SOJ(Shrinked PKG,SOJ)
S	TSOP II (Shrinked PKG,Forward)
W	TSOP II (Shrinked PKG,Reverse)

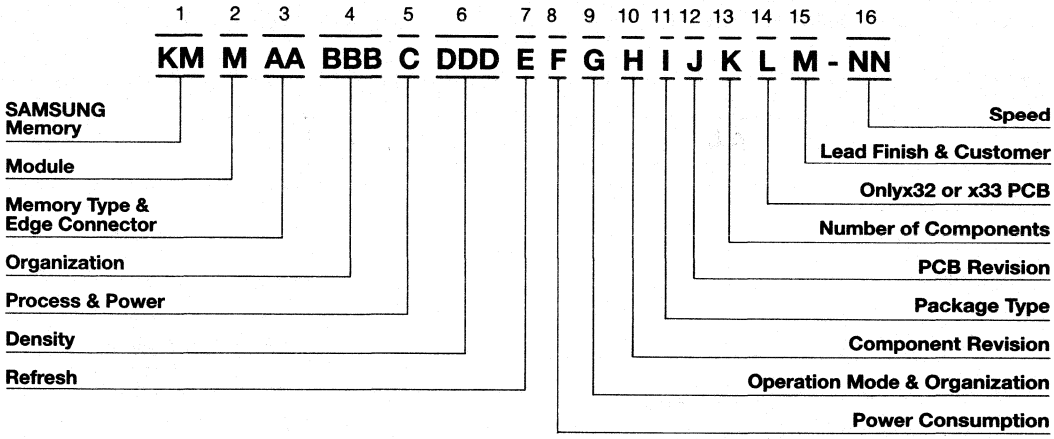
8. Power(DC Current)

Blank	Normal
L	Low power
H	Super Low power
F	Self Refresh with L.P

9 . Speed

- 5	50 ns
- 6	60 ns
- 7	70 ns
- 8	80 ns

4.2 DRAM Module



1. SAMSUNG Memory
2. Module
3. Memory Type & Edge Connector
-1 ····· FLASH
-2 ····· Mask ROM
-3 ····· DRAM DIMM
-4 ····· DRAM SIP
-5 ····· DRAM SIMM
-6 ····· SRAM
-7 ····· Pseudo SRAM
-8 ····· ASSP
-9 ····· VRAM

4. Organization
-8/9 ····· x8/x9 bit wide
-18 ····· x18 bit wide
-32/33 ····· x32/x33
-36/40 ····· x36/x39/x40
-64/66 ····· x64/x66
-72/80 ····· x72/x80
-144 ····· x144 bit wide

5. Process & Operation Voltage
-Blank ····· CMOS 5V
-V ····· CMOS 3.3V
-S ····· Sync 3.3V

6. Density
-16 ····· 16M
-8 ····· 8M
-4 ····· 4M
-2 ····· 2M
-1 ····· 2M
-512 ····· 512K
-256 ····· 256K

7. Refresh (16M DRAM Based)
-0 ····· 4K
-1 ····· 2K
-2 ····· 1K

8. Power Consumption
-0 ····· Normal
-2 ····· Low Power
-4 ····· Super Low Power
-6 ····· Self Refresh

9. Operation Mode & Organization
-0 ····· F/P
-1 ····· Nibble
-2 ····· Static Column
-3 ····· Using Quad CAS
-4 ····· Using EDO
-5 ····· Using EDO & Quad CAS
-8 ····· Using Non Memory Logic
-9 ····· Using Non Memory Logic & Quad CAS

10. Component Revision
-Blank ····· None
-A ····· First Rev.
-B ····· Second Rev.
-C ····· Third Rev.

11. Package Type
-Blank ····· SOJ or PLCC
-T ····· TSOP

12. PCB Revision
-Blank ····· None
-1 ····· First Rev.
-2 ····· Second Rev.
-3 ····· Third Rev.

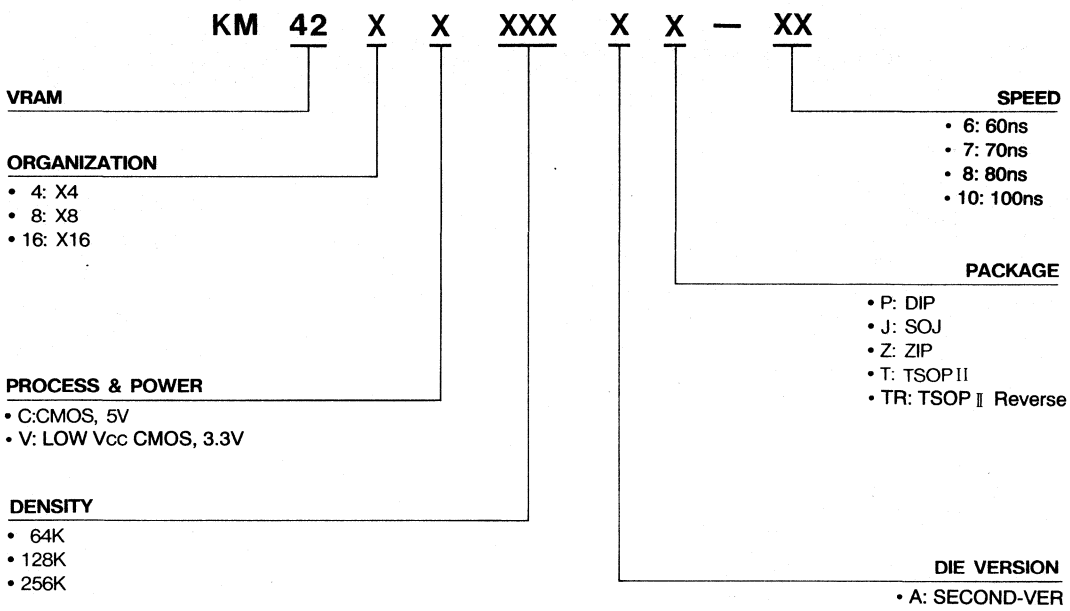
13. Number of Components
-Blank ····· more than 7 chip
-N ····· less than 8 chip
-U ····· Byte Wide Base
-W ····· Word Wide Base

14. Only x32 or x33 PCB
-V ····· x32 or x33 PCB

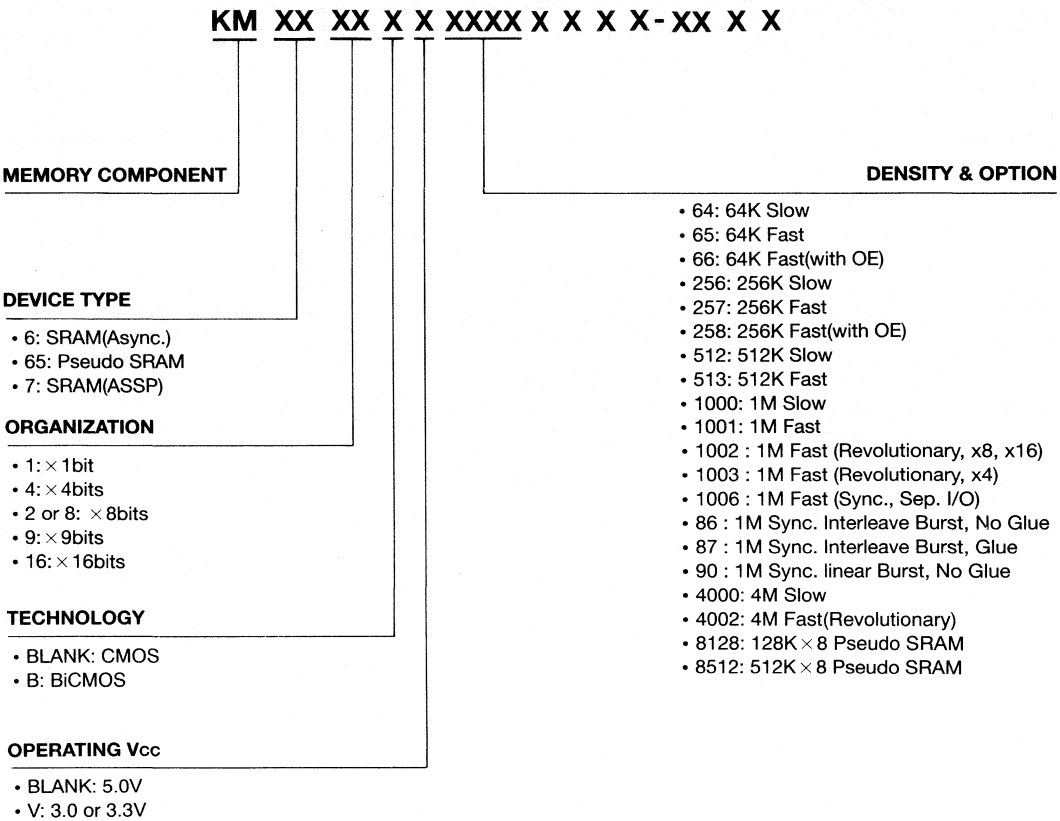
15. Lead Finish & Customer
-Blank ····· Solder
-G ····· Gold
-D ····· DEC
-H ····· HP
-M ····· IBM
-P ····· Nickel
-Q ····· Compaq
-X ····· Cambex

16. Speed
-5 ····· 50ns
-6 ····· 60ns
-7 ····· 70ns
-8 ····· 80ns

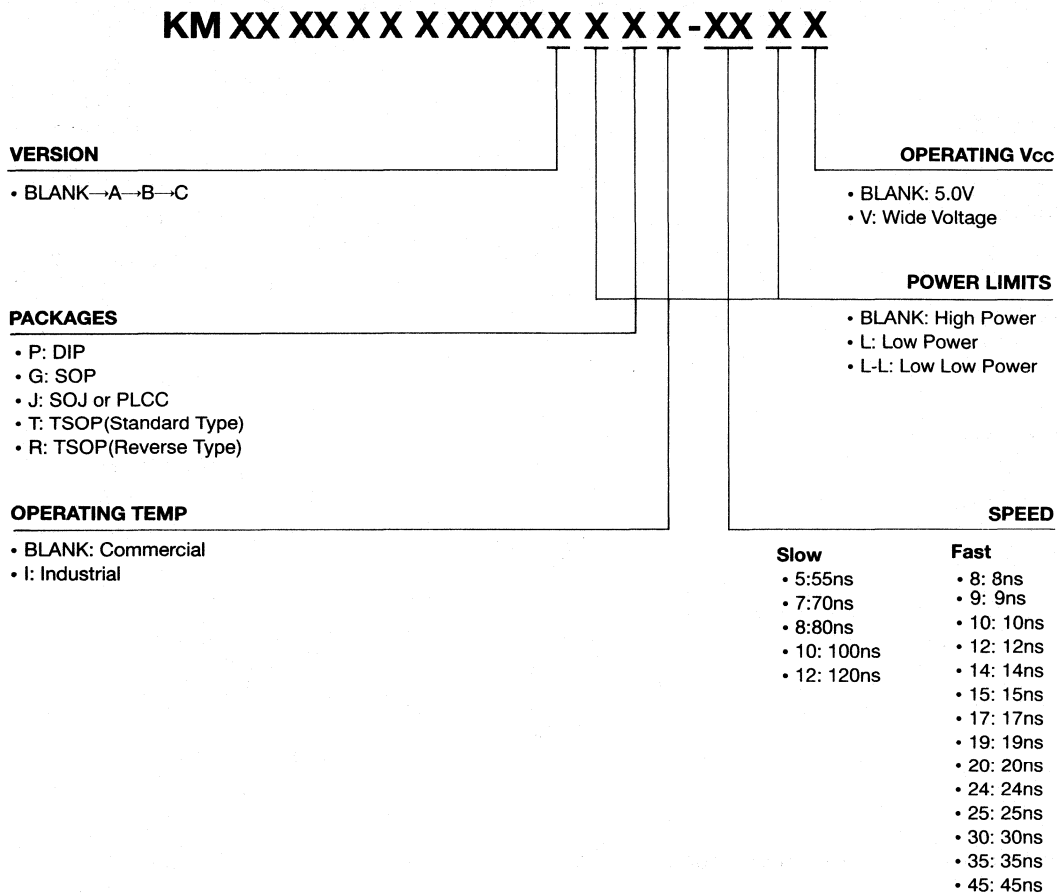
4.3 VRAM


KM 42 X X XXX X X — XX
VRAM
ORGANIZATION
• 4: X4
• 8: X8
• 16: X16
PROCESS & POWER
• C:CMOS, 5V
• V: LOW Vcc CMOS, 3.3V
DENSITY
• 64K
• 128K
• 256K
SPEED
• 6: 60ns
• 7: 70ns
• 8: 80ns
• 10: 100ns
PACKAGE
• P: DIP
• J: SOJ
• Z: ZIP
• T: TSOP II
• TR: TSOP II Reverse
DIE VERSION
• A: SECOND-VER

4.4 Static RAM



4.4 Static RAM



4.5 MASK ROM

KM 23 X XXX XX X X XX - XX

MEMORY

DEVICE TYPE

- 23 : MASK ROM

PROCESS & POWER

- C : CMOS, 5V
- V : CMOS, 3.3V

DENSITY

- 256 : 256K
- 512 : 512K
- 1 : 1M
- 2 : 2M
- 4 : 4M
- 8 : 8M
- 16 : 16M
- 32 : 32M
- 64 : 64M

ORGANIZATION

- 00 : x 8 bit (1M 28DIP, 2M, 4M, 8M)
  x 16 bit (16M, 32M, 64M)
- 01 : x 8 bit (1M 32Pin)
- 10 : x 8 bit (16M, 32M, 64M)
  x 16 bit (2M, 4M, 8M)
- 11 : x 8 bit (32M 42DIP)
- 20 : x 16 bit & EPROM TYPE PIN OUT (4M)
  x 32 bit (16M, 32M, 64M)

TYPE & MODE

- 0 : COMMERCAL
- 1 : Multi OE
- 5 : PAGE MODE

VERSION

- BLANK→A→B→C

PKG

- BLANK : DIP
- G : SOP
- SG : SSOP

SPEED

- 10 : 100ns
- 12 : 120ns
- 15 : 150ns
- 20 : 200ns

* Internal KF · CODE Inforamtion

KF X X XX X

MASK ROM

DENSITY

- 3 : 256K
- Z : 512K
- 4 : 1M
- Y : 2M
- 5 : 4M
- X : 8M
- 6 : 16M
- W : 32M

PRODUCTION LINE

- 1 : LINE 1
- 2 : LINE 2
- 3 : LINE 3

SERIAL NO.

Intermal Ver. NO.

4.6 EEPROM

***Serial EEPROM**

KM 93 C XX X XX X

93 : Micro Wire Type

CMOS Process

DENSITY
46 : 1K Bit
56 : 2K Bit
57 : 2K Bit,x8/x16 Select
66 : 4K Bit
67 : 4K Bit,x8/x16 Select

BLANK: Commercial
I : Industrial

Blank : DIP Package
G : SOIC PKG
GD : SOIC PKG,DIP pin Conf

Blank : 5V Operation.
V : 3V Operation.

***Parallel EEPROM**

KM 28(29) C XXX X X X - XX

28 : Pallel EEPROM
29 : Flash Memory

CMOS Process

Density
64 : 64K Bit
010 : 1M Bit

Revision
Blank : 1st Gen.
A : 2nd Gen.
B : 3rd Gen.

SPEED
9 : 90ns
10 : 100ns
12 : 120ns
15 : 150ns
20 : 200ns

BLANK : Commercial
I : Industrial

Package
Blank : DIP PKG
J : PLCC PKG
T : TSOP I PKG

4.7 Flash

KM 29 N XXXXX X X

Flash Memory

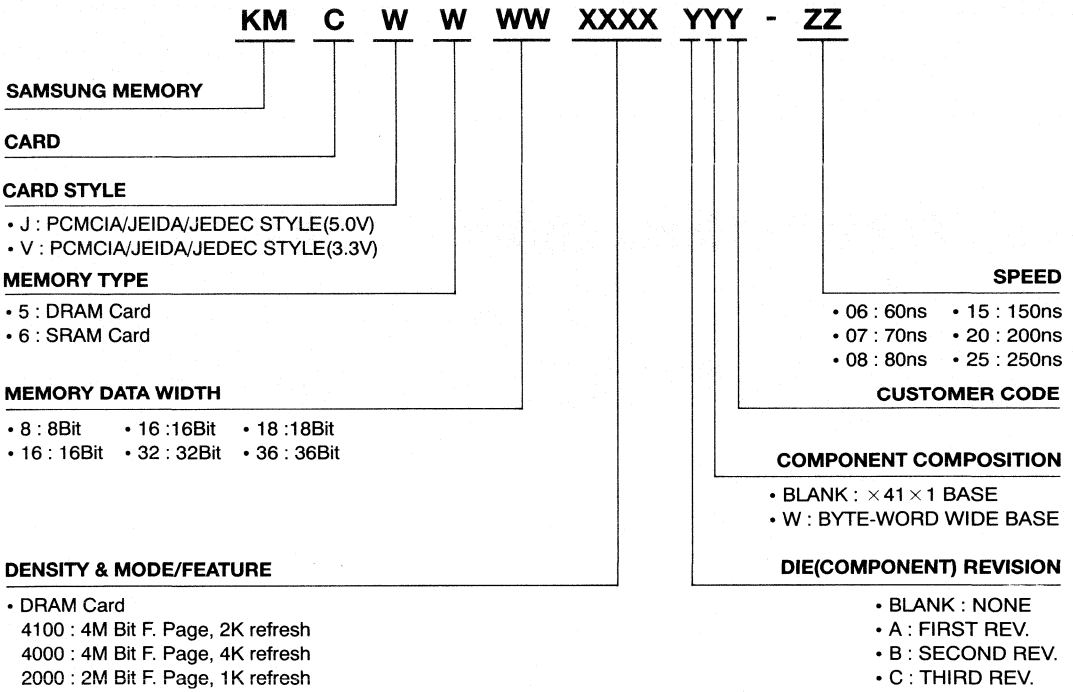
NAND Type (CMOS)

Density
16000 : 16M Bit.
32000 : 32M Bit.
64000 : 64M Bit.

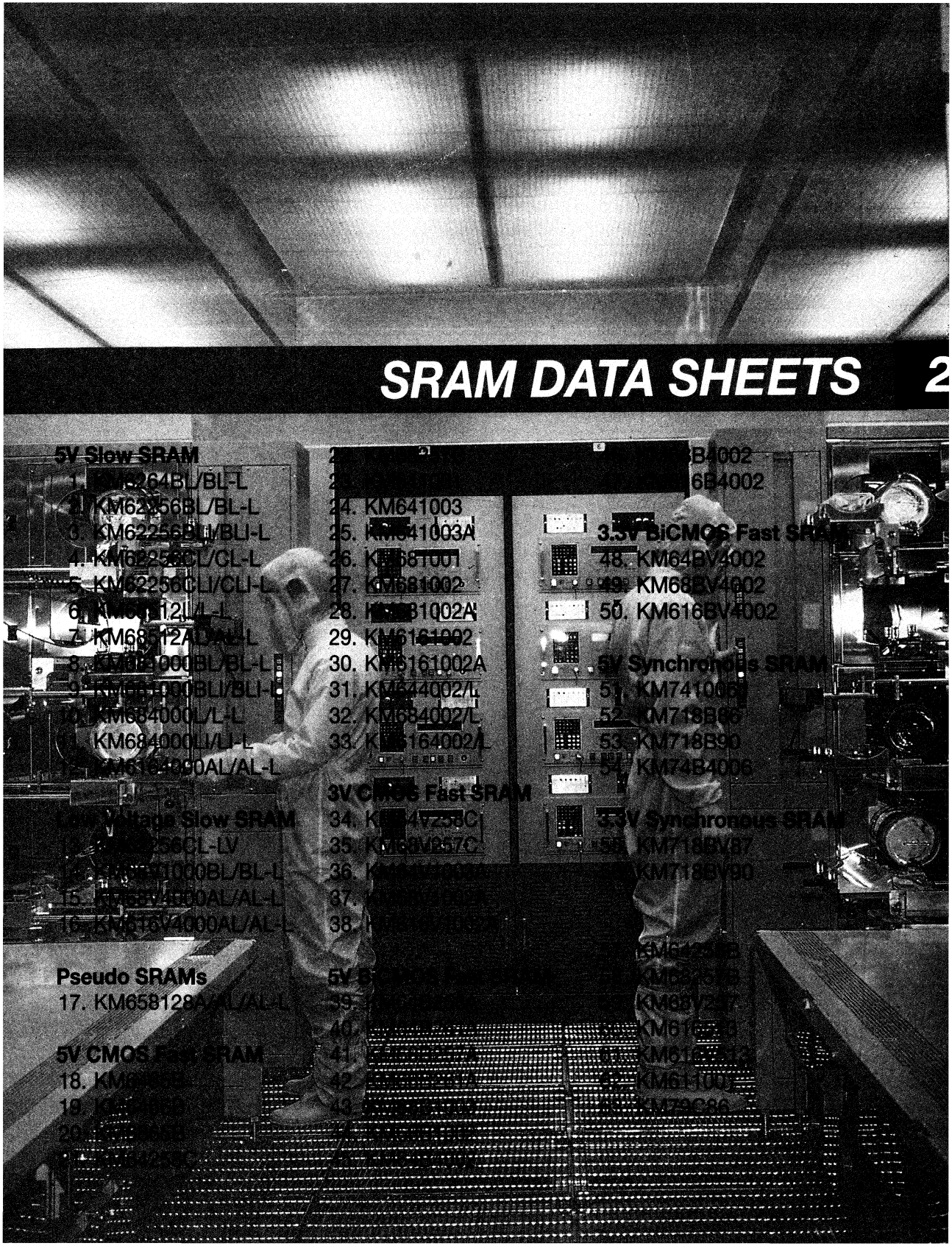
BLANK : Good Block=502~511
S : Good Block=512

Package
T : TSOP Forward Type
R : TSOP Reverse Type

4.8 Memory Card



NOTES



SRAM DATA SHEETS 2

8K x 8 Bit Static RAM

FEATURES

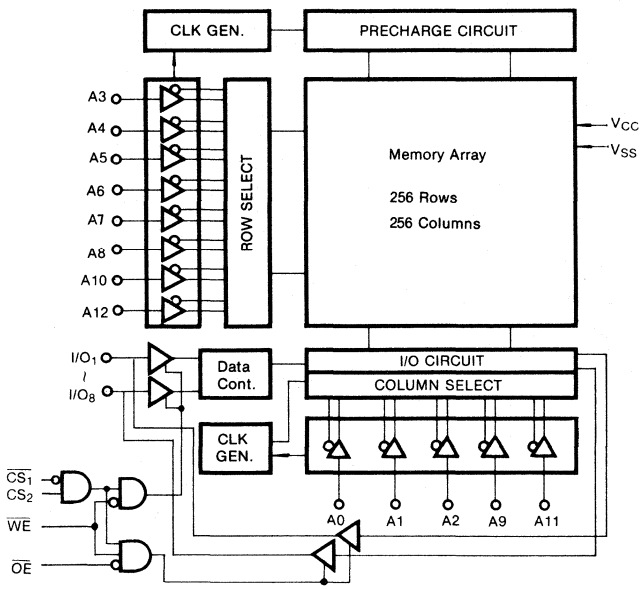
- **Fast Access Time : 70, 100, 120ns (Max.)**
- **Low Power Dissipation**
  Standby (CMOS) : 10μW (typ) L.Version
  : 5μW (typ) LL.Version
  Operating:55mW/1MHz
- **Single 5V±10% power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - No clock or refresh required
- **Three state Output**
- **Low Data Retention Voltage : 2V (Min.)**
- **JEDEC Standard pin coniguration**
  KM6264BLP/BLP-L : 28-DIP-600B
  KM6264BLS/BLS-L : 28-DIP-300
  KM6264BLG/BLG-L : 28-SOP-450

GENERAL DESCRIPTION

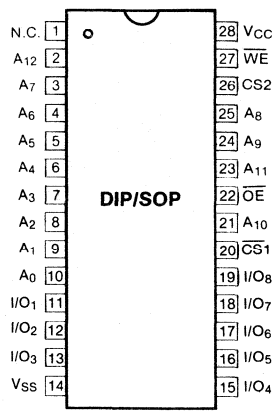
The KM6264BL/BL-L is 65,536-bit high-speed Static Random Access Memory organized as 8, 192 words by 8 bits.
The device is fabricated using Samsung's advanced CMOS process.
The KM6264 BL/BL-L has an output enable input for precise control of the data outputs.
It also has chip select inputs for the minimum current power down mode.
The KM6264 BL/BL-L has been designed for high speed and low power applications.
It is particularly well suited for battery back-up non-volatile memory applications

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



Pin Name	Pin Function
A_0-A_{12}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS1}$, CS2	Chip Select Inputs
$\overline{OE}$	Output Enable Input
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260° C, 10 sec(Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.5*	—	0.8	V

* V_{IL}(min)=-3.0V for $\leq$ 50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V$\pm$10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-2	—	2	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IN} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}		-2	—	2	μA
Operation Power Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, $\overline{CS2}$=V_{IH} V_{IN}=V_{IH} or V_{IL} $I_{I/O}$=0mA		—	—	15	mA
Average Operating Current	I_{CC1}	Cycle Time=1μS, 100% Duty $\overline{CS1}\leq$0.2V, $\overline{CS2}\geq V_{CC}$-0.2V $V_{IL}\leq$0.2V $V_{IH}\geq V_{CC}$-0.2V, $I_{I/O}$=0mA		—	—	10	mA
	I_{CC2}	Min Cycle. 100% Duty $\overline{CS1}$=V_{IL},	70ns	—	—	55	mA
		$\overline{CS2}$=V_{IH}, V_{IN}=V_{IH} or V_{IL} I_{OUT}=0mA	100/120ns	—	—	45	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or $\overline{CS2}$=V_{IL}		—	0.2	2	mA
	I_{SB1}	$\overline{CS1}\geq V_{CC}$-0.2V, $\overline{CS2}\leq$0.2V or $\overline{CS2}\geq V_{CC}$-0.2V,	L	—	2	100	μA
		$V_{IN}\geq V_{CC}$-0.2 or $V_{IN}\leq$0.2V	LL	—	1	10	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1.0mA		2.4	—	—	V

*Typ: V_{CC}=5V, T_A=25° C

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF

* Note: Capacitance is sampled and not 100% tested.

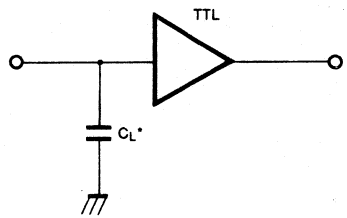
AC CHARACTERISTICS

TEST CONDITIONS ($Ta = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	$^*C_L = 100$ pF + 1 TTL

*C_L=30pF for KM6264BL-7/7L

TEST CIRCUIT



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM6264BL-7 KM6264BL-7L		KM6264BL-10 KM6264BL-10L		KM6264BL-12 KM6264BL-12L		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		100		120		ns
Address Access Time	t_{AA}		70		100		120	ns
Chip Select to Output	t_{CO1}, t_{CO2}		70		100		120	ns
Output Enable to Valid Output	t_{OE}		35		50		60	ns
Chip Enable to Low-Z Output	t_{LZ1}, t_{LZ2}	5		10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5		ns
Chip Disable to High-Z Output	t_{HZ1}, t_{HZ2}	0	30	0	35	0	40	ns
Output Disable to High-Z Output	t_{OHZ}	0	30	0	35	0	40	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

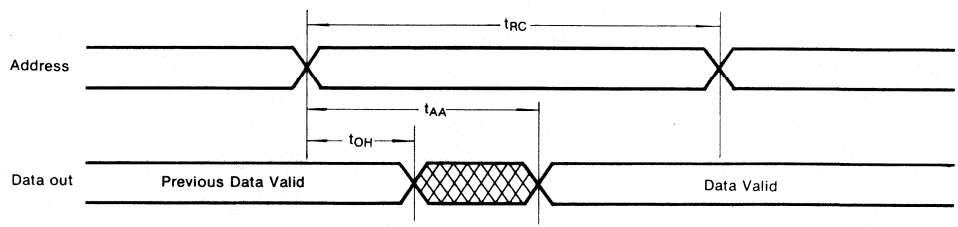
WRITE CYCLE

Parameter	Symbol	KM6264BL-7 KM6264BL-7L		KM6264BL-10 KM6264BL-10L		KM6264BL-12 KM6264BL-12L		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		100		120		ns
Chip Select to End of Write	t_{CW}	60		80		85		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	60		80		85		ns
Write Pulse Width	t_{WP}	40		60		70		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WHZ}	0	30	0	30	0	30	ns
Data to Write Time Overlap	t_{DW}	30		40		50		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		10		ns

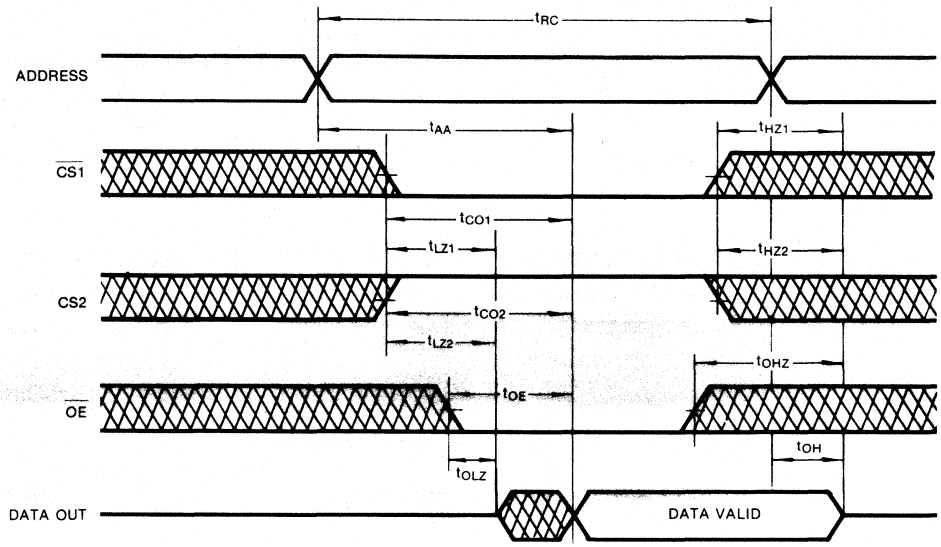
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE NO. 1

($\overline{CS1} = \overline{OE} = V_{IL}$, $CS2 = \overline{WE} = V_{IH}$)



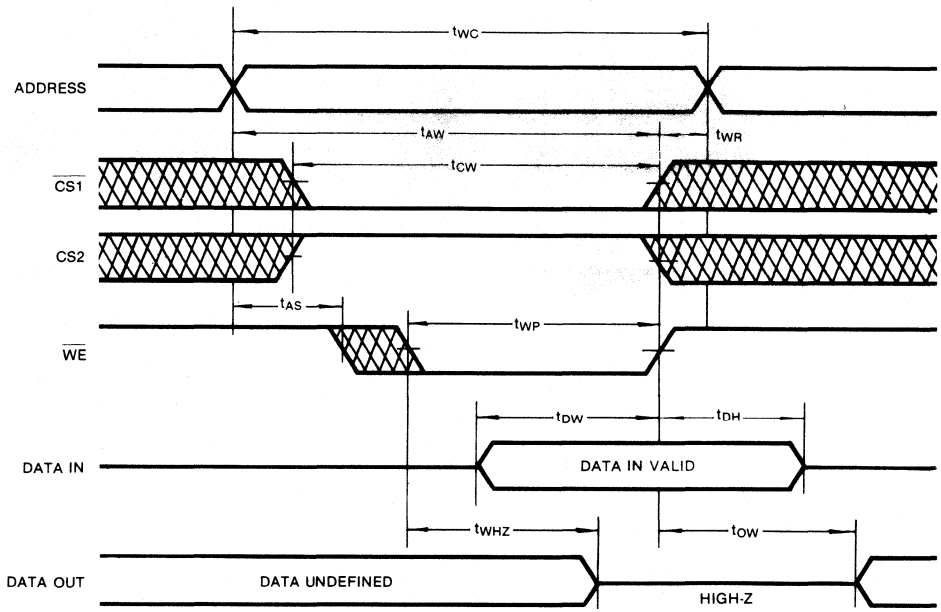
TIMING WAVEFORM OF READ CYCLE NO. 2 ($\overline{WE}$ = V_{IH})



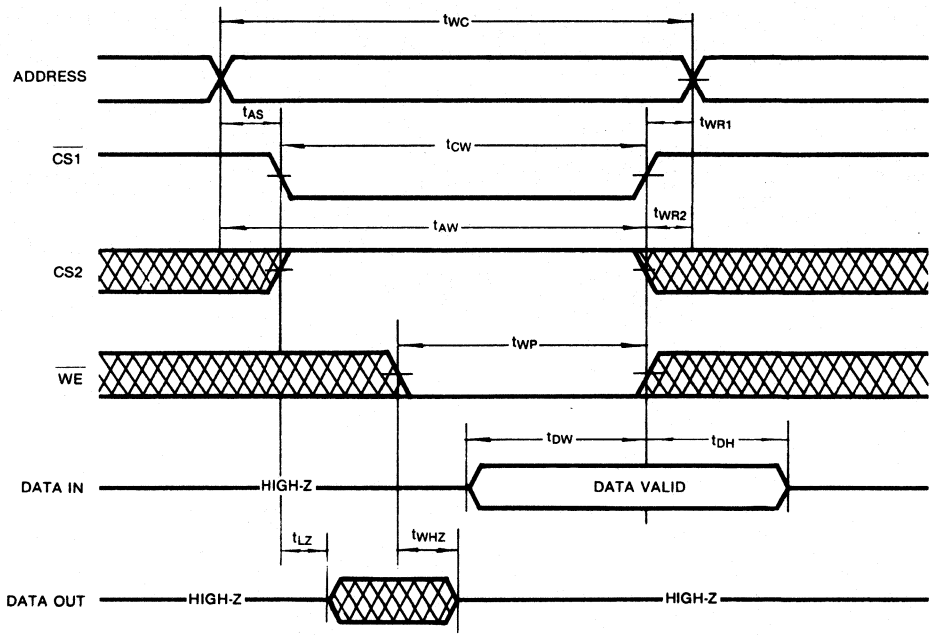
Note (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
2. At any given temperature and voltage condition, t_{HZ}(max) is less than t_{LZ}(min) both for a given device and from device to device.

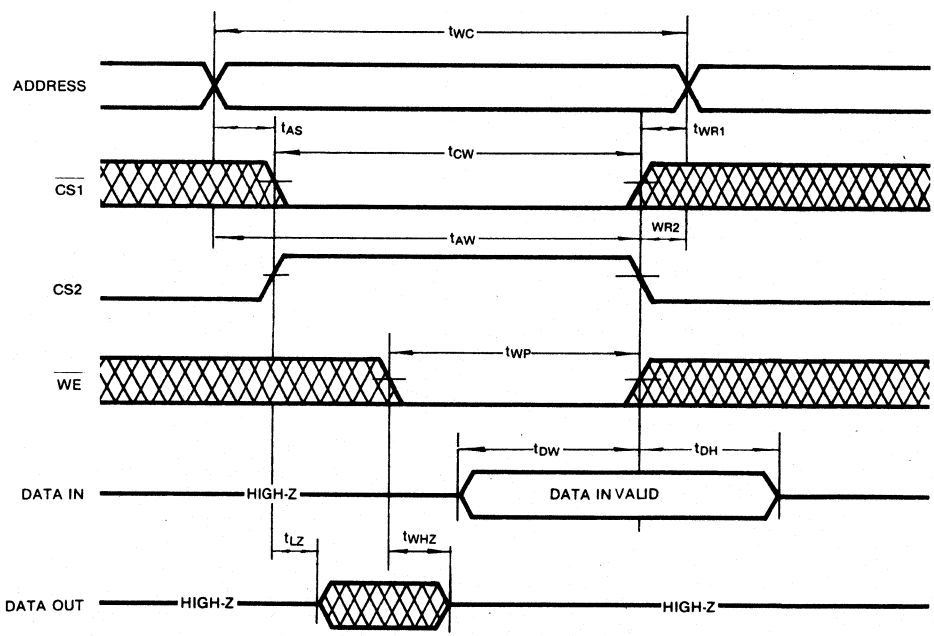
TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (CS2 Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low: A write ends at the earlist transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as $\overline{CS1}$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS2 going low.
5. If $\overline{OE}$, CS2 and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the read data of the new address.
8. When $\overline{CS1}$ is low and CS2 is high; I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

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FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
X*	L	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

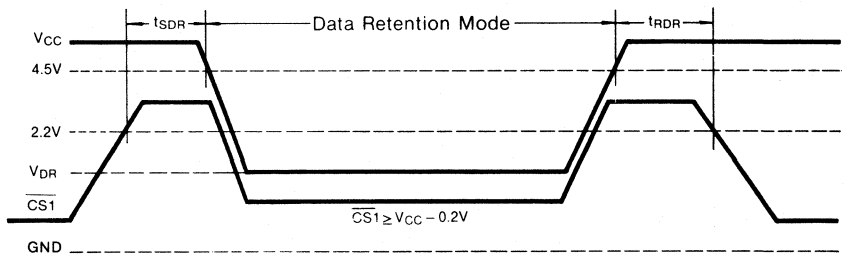
* Note: X means Don't Care.

DATA RETENTION CHARACTERISTICS (T_A = 0 to 70°C)

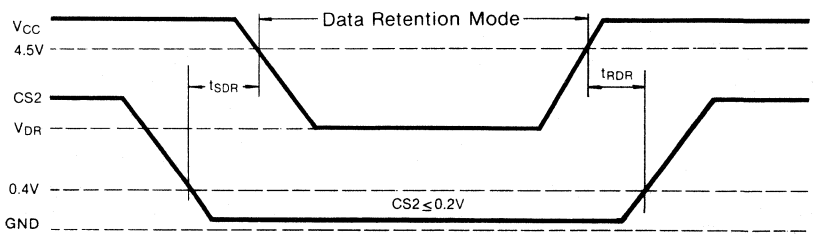
Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1} \geq V_{CC} - 0.2V$*		2.0		5.5	V
Data Retention Current	I_{DR}	V_{CC} = 3V $\overline{CS1} \geq V_{CC} - 0.2V$, CS2 $\geq V_{CC} - 0.2V$ or CS2 $\leq$ 0.2V	L		1	50	μA
			LL		0.5	5**	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Wave forms (below)		0			ns
Recovery Time	t_{RDR}			t_{RC}***			ns

* $\overline{CS1} \geq V_{CC}$-0.2V, CS2 $\geq V_{CC}$-0.2V ($\overline{CS1}$ Controlled) or CS2 $\leq$ 0.2V (CS2 Controlled)
** 1μA (max.) at 0°C~40°C
*** t_{RC}=Read cycle time

DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM (2) (CS2 Controlled)



32,768 WORD x 8 Bit CMOS Static RAM

FEATURES

- **Fast Access Time: 70, 85, 100, 120ns (Max.)**
- **Low Power Dissipation**
  - **Standby (CMOS): 10μW (Typ.) L-Version**
  - **5μW (Typ.) LL-Version**
  - **Operating : 35mW/1MHz (Max.)**
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three State Outputs**
- **Low Data Retention Voltage: 2V (Min.)**
- **Standard Pin Configuration**
  - **KM62256BLP/BLP-L : 28-DIP-600B**
  - **KM62256BLG/BLG-L : 28-SOP-450**
  - **KM62256BLS/BLS-L : 28-DIP-300**
  - **KM62256BLTG/BLTG-L : 28-TSOP1-0813.4F**
  - **KM62256BLRG/BLRG-L : 28-TSOP1-0813.4R**

GENERAL DESCRIPTION

The KM62256BL/BL-L is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.

The device is fabricated using Samsung's advanced CMOS process with polyresistors.

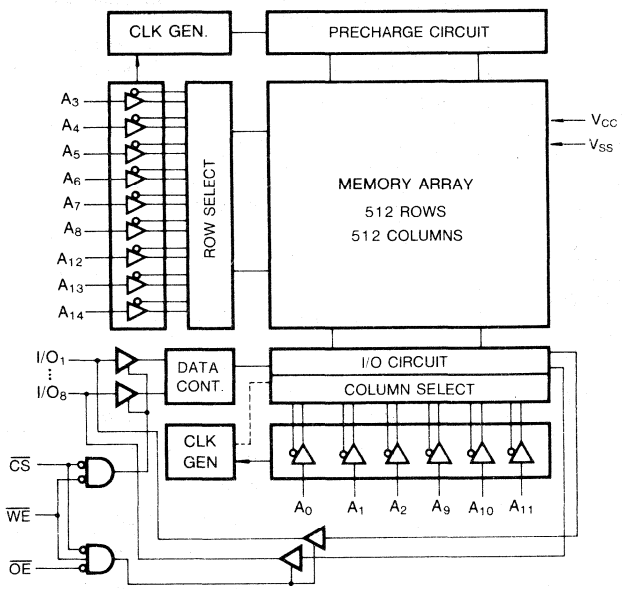
The KM62256BL/BL-L has an output enable input for precise control of the data outputs.

It also has a chip enable input for the minimum current power down mode.

The KM62256BL/BL-L has been designed for high speed and low power application. It is particularly well suited for battery back-up nonvolatile memory application.

2

FUNCTIONAL BLOCK DIAGRAM

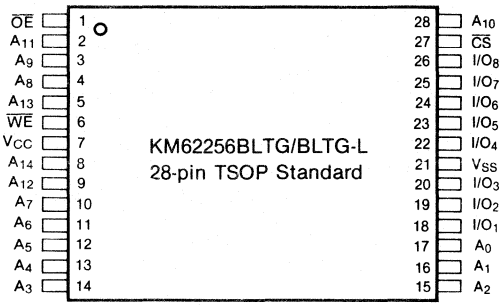


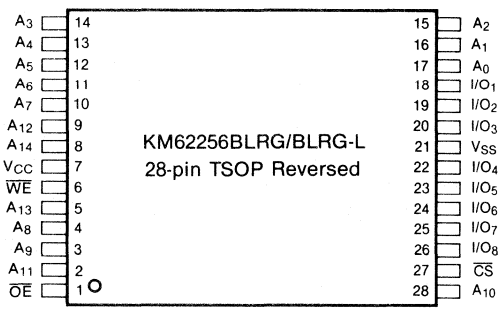
PIN CONFIGURATIONS

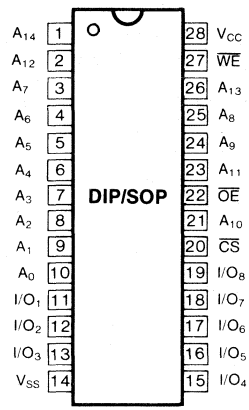
Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection (32-TSOP only)

PIN CONFIGURATIONS (Top View)

28-pin TSOP (0813.4)







ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to V_{CC} +5.5	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260° C, 10 sec(Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.5*	—	0.8	V

* V_{IL}(min)=-3.0V for $\leq$ 50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V$\pm$10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-1	—	1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IN} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}		-1	—	1	μA
Operation Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL} $I_{I/O}$=0mA		—	7	15	mA
Average Operating Current	I_{CC1}	Cycle Time=1μS, 100% Duty $\overline{CS}\leq$0.2V, $V_{IL}\leq$0.2V $V_{IH}\geq V_{CC}$-0.2V, $I_{I/O}$=0mA		—	—	7	mA
	I_{CC2}	Min Cycle. 100% Duty $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH} $I_{I/O}$=0mA		—	45	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}		—	—	1	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}$-0.2V, $V_{IN}\geq V_{CC}$-0.2 or $V_{IN}\leq$0.2V	L-Ver	—	2	100	μA
			LL-Ver	—	1	20	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1.0mA		2.4	—	—	V

*Typ: V_{CC}=5V, T_A=25° C

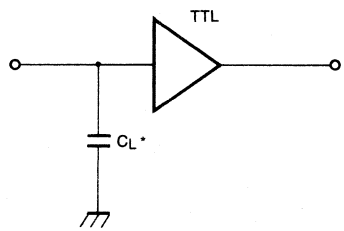
CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF

Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS ($T_A = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Loads	$C_L = 100pF + 1$ TTL



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM62256BL-7 KM62256BL-7L		KM62256BL-8 KM62256BL-8L		KM62256BL-10 KM62256BL-10L		KM62256BL-12 KM62256BL-12L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		120		ns
Address Access Time	t_{AA}		70		85		100		120	ns
Chip Select to Output	t_{CO}		70		85		100		120	ns
Output Enable to Valid Output	t_{OE}		35		45		50		60	ns
Chip Select to Low-Z Output	t_{LZ}	10		10		10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5		5		ns
Chip Disselect to High-Z Output	t_{HZ}	0	30	0	30	0	35	0	40	ns
Output Disable to High-Z Output	t_{OHZ}	0	30	0	30	0	35	0	40	ns
Output Hold from Address Change	t_{OH}	5		5		10		10		ns

WRITE CYCLE

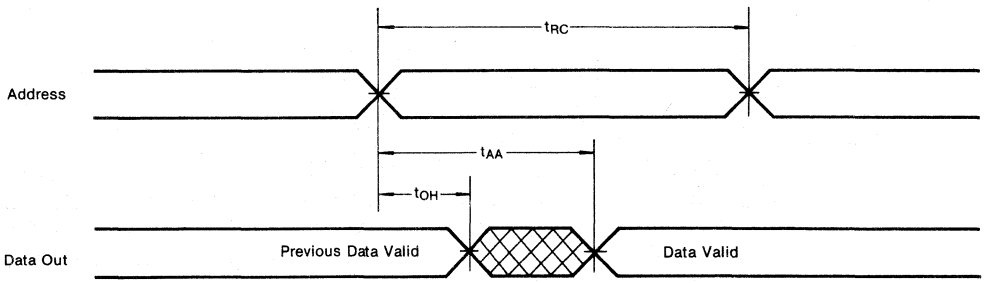
Parameter	Symbol	KM62256BL-7 KM62256BL-7L		KM62256BL-8 KM62256BL-8L		KM62256BL-10 KM62256BL-10L		KM62256BL-12 KM62256BL-12L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		120		ns
Chip Select to End of Write	t_{CW}	60		75		80		85		ns
Address Valid to End of Write	t_{AW}	60		75		80		85		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Write Pulse Width	t_{WP}	50		60		60		70		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WHZ}	0	25	0	30	0	30	0	40	ns
Data to Write Time Overlap	t_{DW}	30		40		40		50		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		5		5		ns

2

TIMING DIAGRAMS

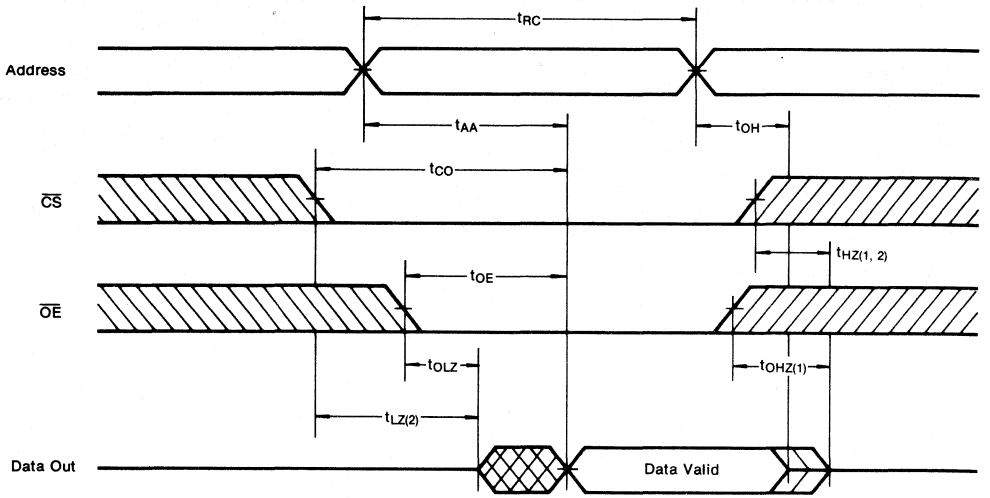
TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)



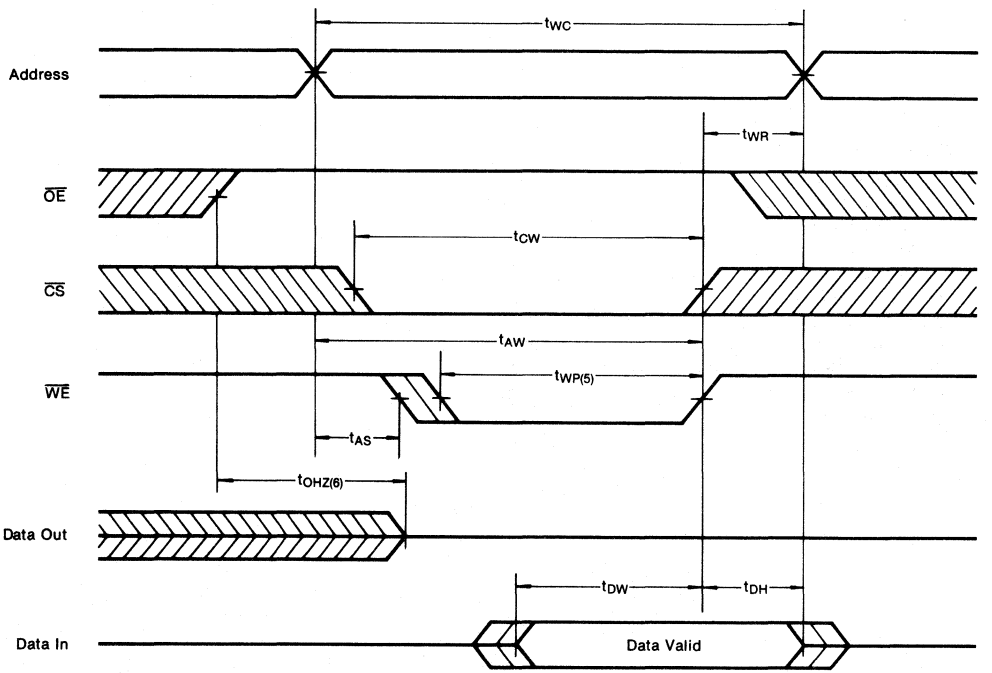
TIMING WAVEFORM OF READ CYCLE (2)

($\overline{WE}$ = V_{IH}) (Note 1, 2, 3, 4)



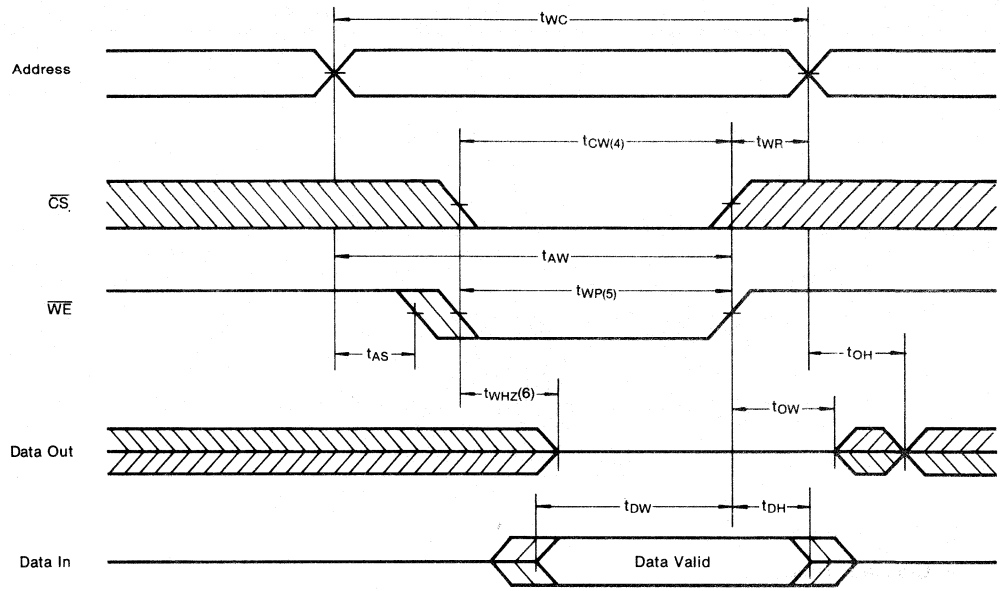
TIMING WAVEFORM OF WRITE CYCLE (3)

($\overline{OE}$ Clocked) (Note 5, 6, 7, 8)



TIMING WAVEFORM OF WRITE CYCLE (4)

($\overline{OE}$ Low Fixed) (Note 5, 6, 7, 8, 9)



Notes

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to the V_{OH} or V_{OL} level.
2. At any given temperature and voltage condition t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ transition Low.
5. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and $\overline{WE}$.
6. During this period, I/O pins are in the output state. The input signals out of phase must not applied.
7. $\overline{CS}$ or $\overline{WE}$ must be high during address transition state.
8. If $\overline{OE}$ is high, I/O pins remain in a high-impedance state.
9. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

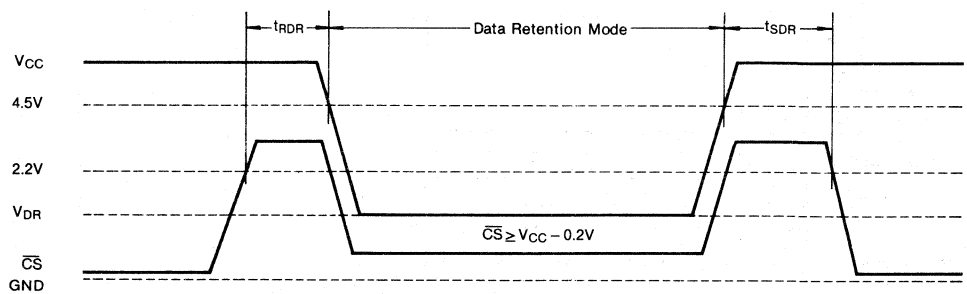
* X means Don't Care.

DATA RETENTION CHARACTERISTICS (T_A=0 to 70°C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$		2.0		5.5	V
Data Retention Current	I_{DR}	V_{CC} = 3.0V $\overline{CS} \geq V_{CC} - 0.2V$	L		1	50*	μA
			L-L		0.5	10**	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)		0			ns
Recovery Time	t_{RDR}			t_{RC}***			ns

* 20μA (Max.) at 0°C~40°C
** 3μA (Max.) at 0°C~40°C
*** t_{RC}: Read Cycle Time

DATA RETENTION WAVEFORM ($\overline{CS}$ Controlled)



32,768 WORD x 8 Bit CMOS Static RAM *(Industrial Temperature Range Operation)*

FEATURES

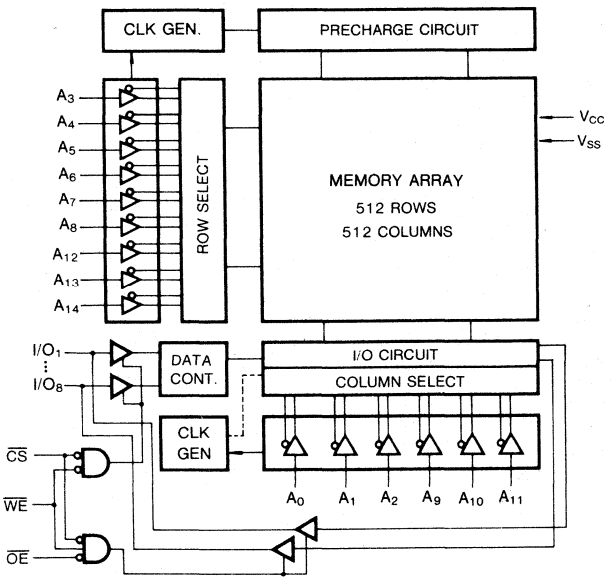
- **Industrial Temperature Range : -40 to 85° C**
- **Fast Access Time: 70, 100ns(max.)**
- **Low Power Dissipation**
  Standby (CMOS) : 275μW(max.)
  Operating : 110mW(max.)
- **Single 5V±10% power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - No clock or refresh required
- **Three State Output**
- **Low Data Retention Voltage: 2V(Min.)**
- **Jedec Standard Pin Configuration**
  KM62256BLPI : 28-DIP-600B
  KM62256BLGI : 28-SOP-450

GENERAL DESCRIPTION

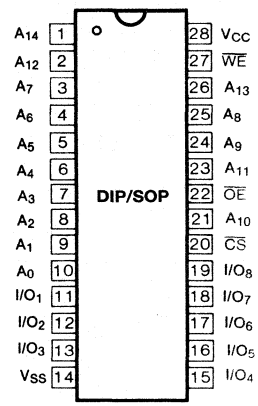
The KM62256BLI/BLI-L is a 262,144-bit high speed Static Random Access Memory organized as 32,768 words by 8 bits.
The device is fabricated using Samsung's advanced CMOS technology.
The KM62256BLI/BLI-L has been designed for high speed and low power applications. It is particularly well suited for battery back-up memory application.
And -40 to 85° C operating temperature range makes it ideal for industrial use.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A14	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select I
$\overline{OE}$	Output Enable
I/O1~I/O8	Data Inputs/Outputs
VCC	Power(+5V)
VSS	Ground

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to + 150	°C
Operating Temperature	T_A	-40 to 85	°C
Soldering Temperature and Time	T_{SOLDER}	260°C, 10sec(Lead only)	—

* Stresses greater than those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=-40 to 85°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.5	—	0.8	V

* V_{IL}(min.)=-3.0V for$\leq$50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=-40 to 85°C, V_{CC}=5V$\pm$10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-1		1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IN} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}		-1		1	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL} II/O=0mA			7	20	mA
Average Operating Current	I_{CC1}	Cycle Time=1μs, $\overline{CS}\leq$0.2V, $V_{IL}\leq$0.2V $V_{IH}\geq V_{CC}$-0.2V, $I_{I/O}$=0mA				10	mA
	I_{CC2}	$\overline{CS}$=V_{IL}, Min Cycle,100% Duty $I_{I/O}$=0mA				70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}				2	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}$-0.2V $V_{IN}\geq V_{CC}$-0.2V or $V_{IN}\leq$0.2V	L-Ver			100	μA
			LL-Ver			20	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA				0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1.0mA		2.2			V

* Typ : V_{CC}=5V, T_A=25°C

CAPACITANCE (f=1MHz, T_A=25°C)

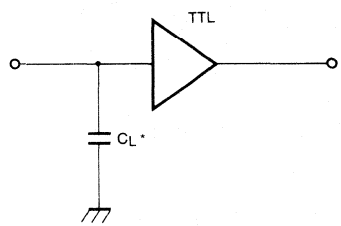
Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note : Capacitance is sampled and not 100% tested.

TEST CONDITIONS (T_A=-40 to 85°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	C_L=100pF+1TTL Load

TEST CIRCUIT



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM62256BLI-7 KM62256BLGI-7		KM62256BLI-10 KM62256BLGI-10		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		100		ns
Address Access Time	t_{AA}		70		100	ns
Chip Select to Output	t_{CO}		70		100	ns
Output Enable to Valid Output	t_{OE}		35		50	ns
Chip Select to Low-Z Output	t_{LZ}	10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Chip Deselect to High-Z Output	t_{HZ}	0	30	0	35	ns
Output Disable to High-Z Output	t_{OHZ}	0	30	0	35	ns
Output Hold from Address Change	t_{OH}	5		10		ns

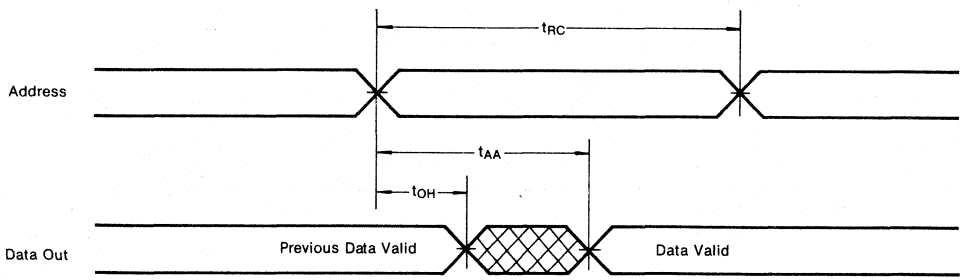
WRITE CYCLE

Parameter	Symbol	KM62256BLI-7 KM62256BLGI-7		KM62256BLI-10 KM62256BLGI-10		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		100		ns
Chip Select to End of Write	t_{CW}	60		80		ns
Address Set-up Time	t_{AS}	0		0		ns
Address Valid to End of Write	t_{AW}	60		80		ns
Write Pulse Width	t_{WP}	50		60		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to Output High-Z	t_{WHZ}	0	25	0	35	ns
Data to Write Time Overlap	t_{DW}	30		50		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Output Low-Z	t_{OW}	5		10		ns

TIMING DIAGRAMS

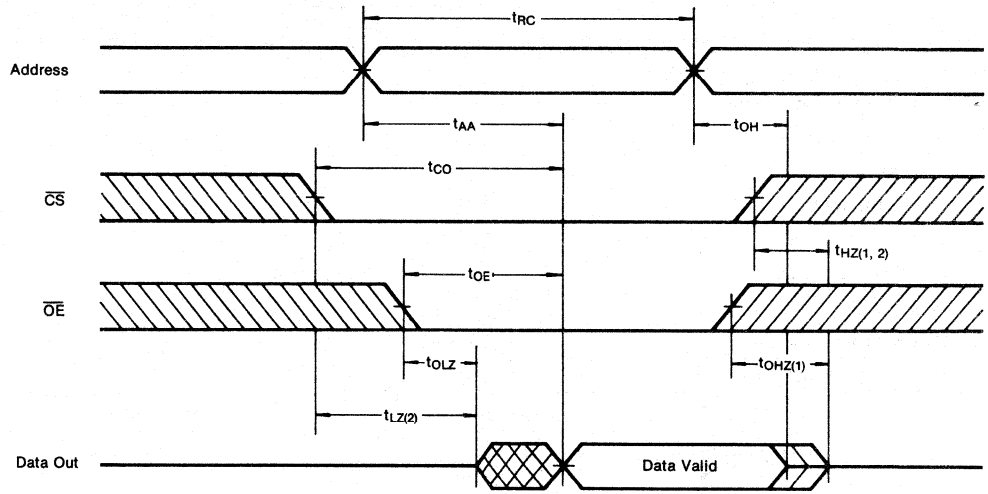
TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=$\overline{OE}$, V_{IL}, $\overline{WE}$=V_{IH})



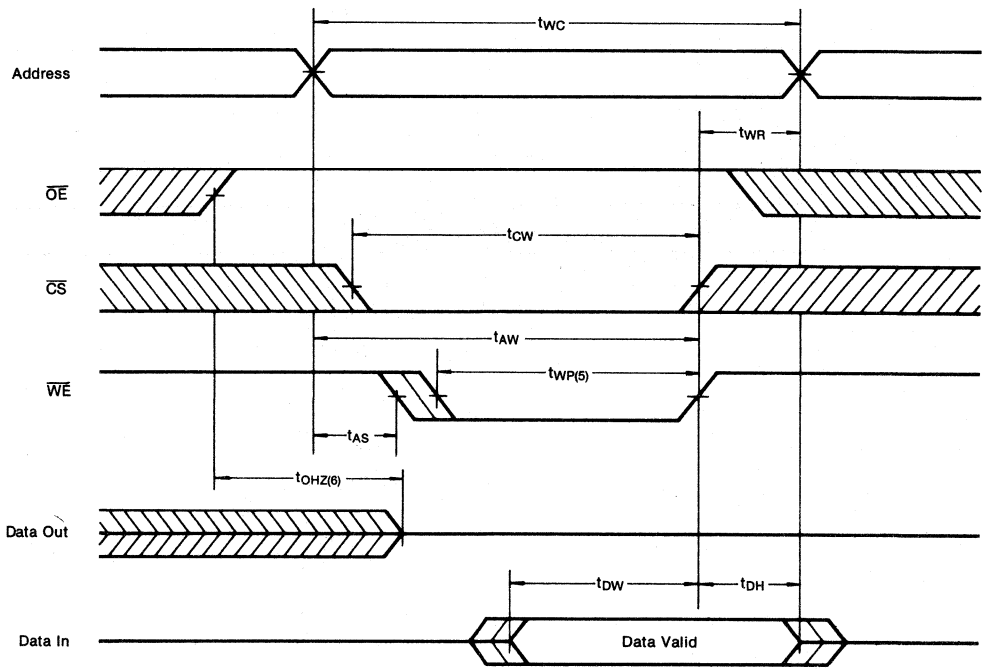
TIMING WAVEFORM OF READ CYCLE (2)

($\overline{WE}$ = V_{IH}) (Note 1, 2, 3, 4)



TIMING WAVEFORM OF WRITE CYCLE (3)

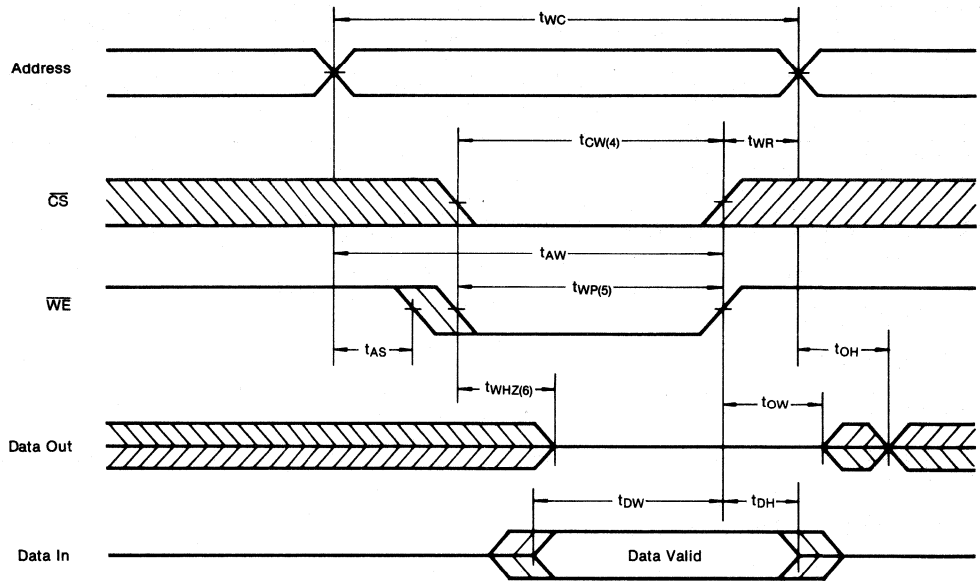
($\overline{OE}$ Clocked) (Note 5, 6, 7, 8)



SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE (4)

($\overline{OE}$ Low Fixed) (Note 5, 6, 7, 8, 9)



Notes

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to the V_{OH} or V_{OL} level.
2. At any given temperature and voltage condition t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ transition Low.
5. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and WE.
6. During this period, I/O pins are in the output state. The input signals out of phase must not applied.
7. $\overline{CS}$ or $\overline{WE}$ must be high during address transition state.
8. If $\overline{OE}$ is high, I/O pins remain in a high-impedance state.
9. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).

FUNCTIONAL DESCRIPTION

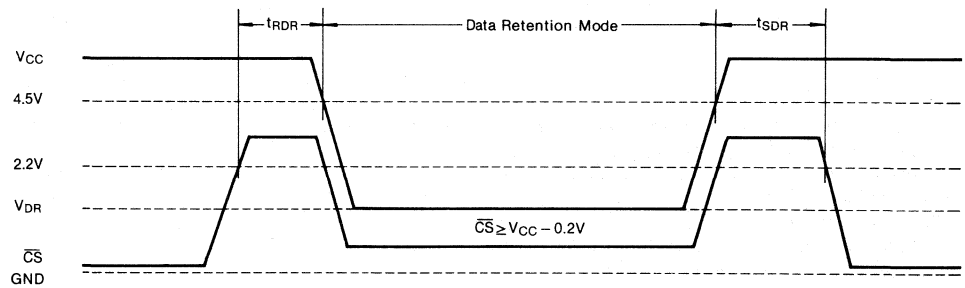
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Vcc Current
H	X*	X	Power down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* X means Don't Care

DATA RETENTION CHARACTERISTICS (T_A=-40 to 85°C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Vcc for Data Retention	V_{DR}	$\overline{CS}1 \geq V_{CC}$-0.2V		2.0		5.5	V
Data Retention Current	I_{DR}	$V_{CC} \geq 3.0V$	L	-		50	μA
		$\overline{CS} \geq V_{CC}$-0.2V	LL	-		10	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms(below)		0			ns
Recovery Time	t_{RDR}			t_{RC}*			ns

* Read Cycle Time



SAMSUNG ELECTRONICS

32,768 WORD x 8 Bit CMOS Static RAM

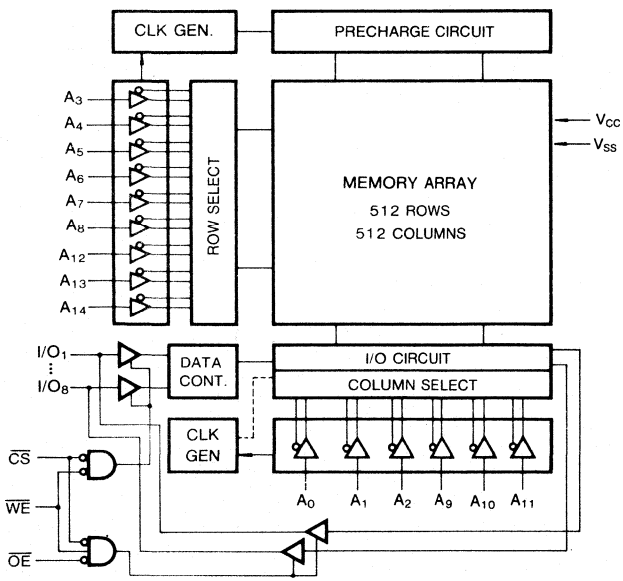
FEATURES

- **Fast Access Time : 55, 70, 85, 100ns(Max.)**
- **Low Power Dissipation**
  Standby (CMOS) : 10μW(Typ.) L-Version
  5μW(Typ.) LL-Version
  Operating : 35mW/1MHz(Max.)
- **Single 5V$\pm$10% power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - No clock or refresh required
- **Three state Output**
- **Low Data Retention Voltage : 2V (Min.)**
- **Standard Pin Configuration**
  KM62256CLP/CLP-L : 28-DIP-600B
  KM62256CLG/CLG-L : 28-SOP-450
  KM62256CLS/CLS-L : 28-DIP-300
  KM62256CLTG/CLTG-L : 28-TSOP1-0813.4F
  KM62256CLRG/CLRG-L : 28-TSOP1-0813.4R

GENERAL DESCRIPTION

The KM62256CL/CL-L is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.
The device is fabricated using Samsung's advanced CMOS process with poly resistors.
The KM62256CL/CL-L has an output enable input for precise control of the data outputs.
It also has a chip enable input for the minimum current power down mode.
The KM62256CL/CL-L has been designed for high speed and low power application. It is particularly well suited for battery back-up nonvolatile memory application.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)

Pin Name	Pin Function
A0-A14	Address Inputs
$\overline{WE}$	Write Enable input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power(5V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to V_{CC} + 0.5	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{SOLDER}	260°C, 10sec(Lead only)	—

* Stresses greater than those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.5*	—	0.8	V

* V_{IL}(min.)=-3.0V for$\leq$50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V$\pm$10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-1	—	1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}		-1	—	1	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL} II/O=0mA		—	7	15	mA
Average Operating Current	I_{CC1}	Cycle Time=1μs, 100% Duty $\overline{CS}\leq$0.2V, $V_{IL}\leq$0.2V, $V_{IH}\geq V_{CC}$-0.2V, $I_{I/O}$=0mA		—	—	7	mA
	I_{CC2}	Min Cycle,100% Duty $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH} $I_{I/O}$=0mA		—	45	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}		—	—	1	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}$-0.2V $V_{IN}\geq V_{CC}$-0.2V	L-Ver	—	2	100	μA
		or $V_{IN}\leq$0.2V	LL-Ver	—	1	20	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1.0mA		2.4	—	—	V

* Typ : V_{CC}=5V, T_A=25°C

CAPACITANCE (f=1MHz, T_A=25°C)*

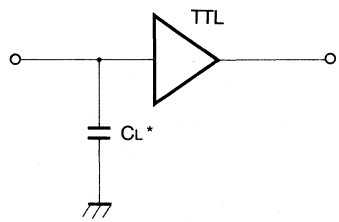
Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note : Capacitance is sampled and not 100% tested.

TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	C_L=100pF+1TTL

TEST CIRCUIT



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM62256CL-5 KM62256CL-5L		KM62256CL-7 KM62256CL-7L		KM62256CL-8 KM62256CL-8L		KM62256CL-10 KM62256CL-10L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	55		70		85		100		ns
Address Access Time	t_{AA}		55		70		85		100	ns
Chip Select to Output	t_{CO}		55		70		85		100	ns
Output Enable to Valid Output	t_{OE}		25		35		45		50	ns
Chip Select to Low-Z Output	t_{LZ}	10		10		10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5		5		ns
Chip Deselect to High-Z Output	t_{HZ}	0	20	0	30	0	30	0	35	ns
Output Disable to High-Z Output	t_{OHZ}	0	20	0	30	0	30	0	35	ns
Output Hold from Address Change	t_{OH}	5		5		10		10		ns

WRITE CYCLE

Parameter	Symbol	KM62256CL-5 KM62256CL-5L		KM62256CL-7 KM62256CL-7L		KM62256CL-8 KM62256CL-8L		KM62256CL-10 KM62256CL-10L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	55		70		85		100		ns
Chip Select to End of Write	t_{CW}	45		60		75		80		ns
Address Valid to End of Write	t_{AW}	45		60		75		80		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Write Pulse Width	t_{WP}	40		50		60		60		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WHZ}	0	20	0	25	0	30	0	30	ns
Data to Write Time Overlap	t_{DW}	25		30		40		40		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		5		5		ns

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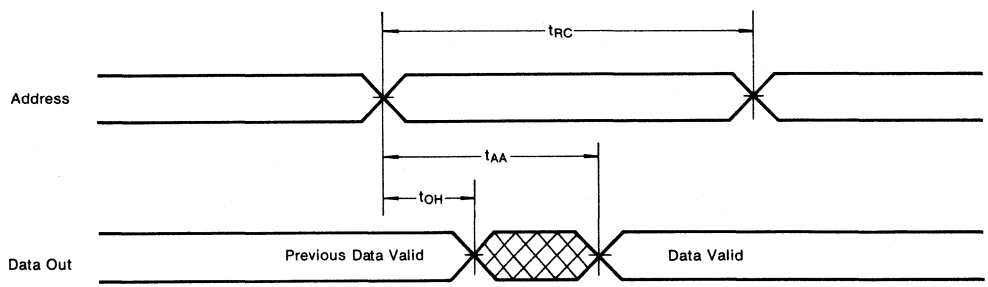
TIMING DIAGRAMS

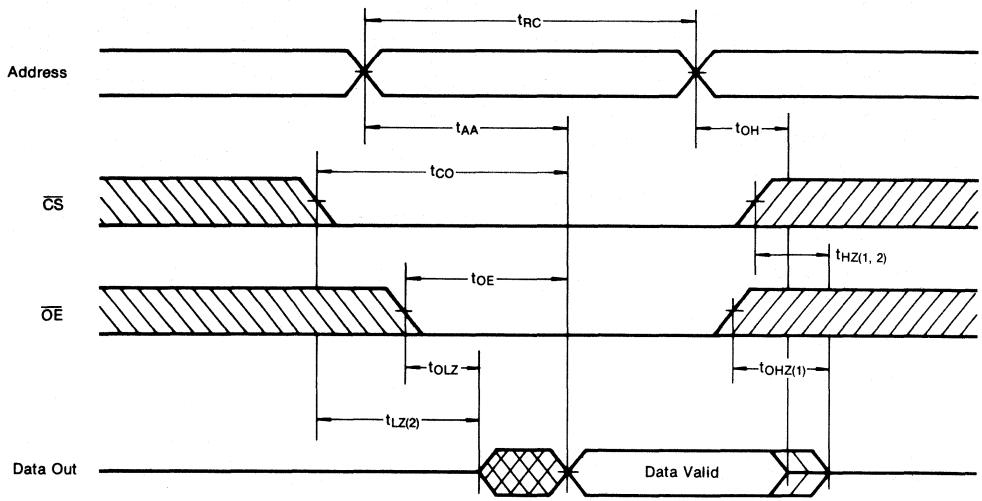
TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)



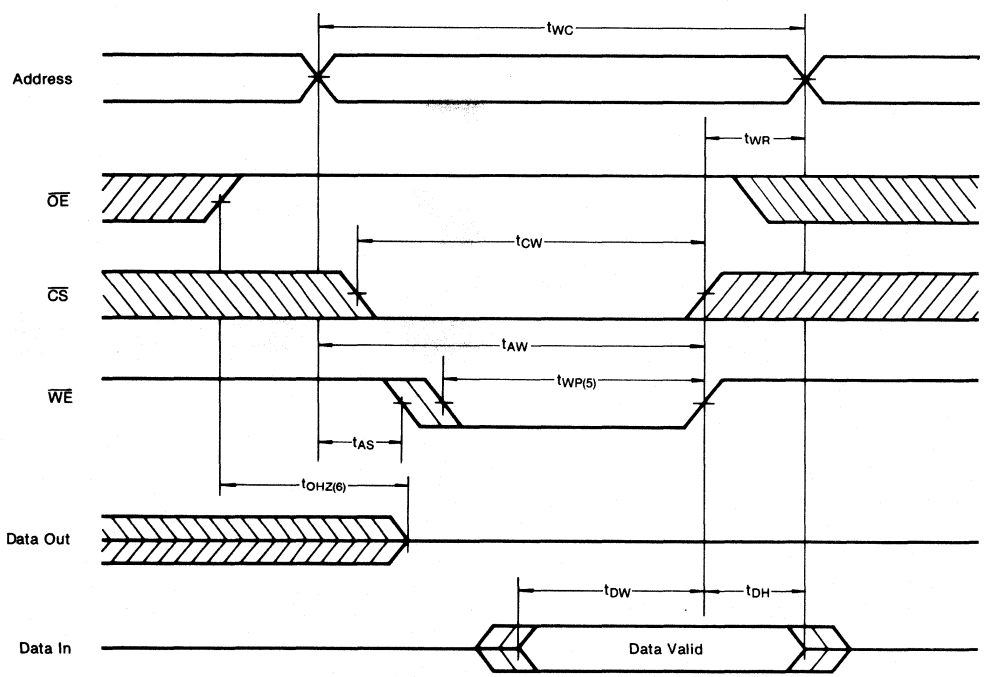
TIMING WAVEFORM OF READ CYCLE (2)

($\overline{WE}$ = V_{IH}) (Note 1, 2, 3, 4)



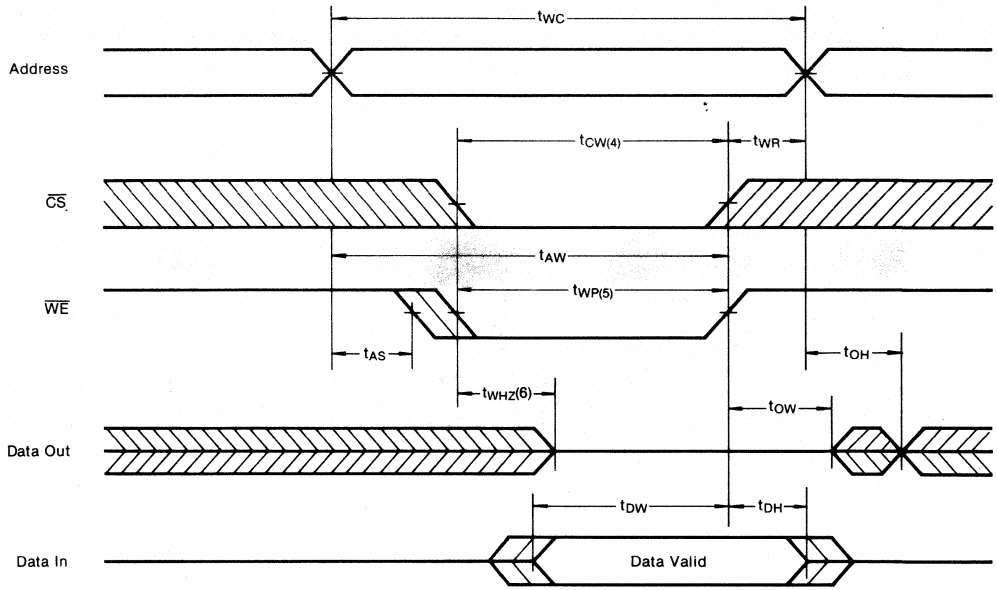
TIMING WAVEFORM OF WRITE CYCLE (3)

($\overline{OE}$ Clocked) (Note 5, 6, 7, 8)



TIMING WAVEFORM OF WRITE CYCLE (4)

($\overline{OE}$ Low Fixed) (Note 5, 6, 7, 8, 9)



Notes

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to the V_{OH} or V_{OL} level.
2. At any given temperature and voltage condition t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ transition Low.
5. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and $\overline{WE}$.
6. During this period, I/O pins are in the output state. The input signals out of phase must not applied.
7. $\overline{CS}$ or $\overline{WE}$ must be high during address transition state.
8. If $\overline{OE}$ is high, I/O pins remain in a high-impedance state.
9. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

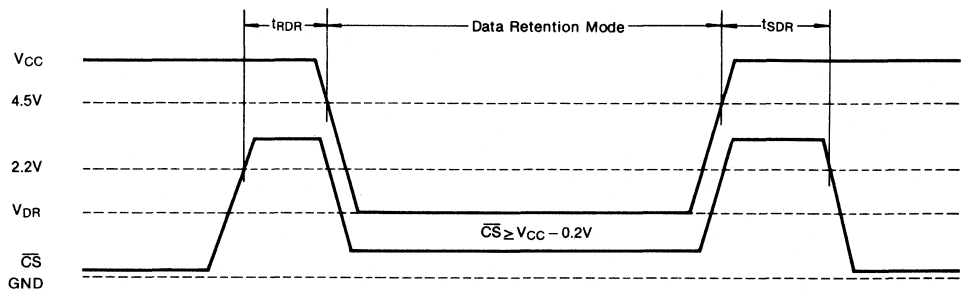
* X means Don't Care.

DATA RETENTION CHARACTERISTICS (T_A = 0 to 70°C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$		2.0		5.5	V
Data Retention Current	I_{DR}	V_{CC} = 3.0V $\overline{CS} \geq V_{CC} - 0.2V$	L		1	50*	μA
			L-L		0.5	10**	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)		0			ns
Recovery Time	t_{RDR}			t_{RC}***			ns

* 20μA (Max.) at 0°C~40°C
** 3μA (Max.) at 0°C~40°C
*** t_{RC}: Read Cycle Time

DATA RETENTION WAVEFORM ($\overline{CS}$ Controlled)



32,768 WORD x 8 Bit CMOS Static RAM

FEATURES

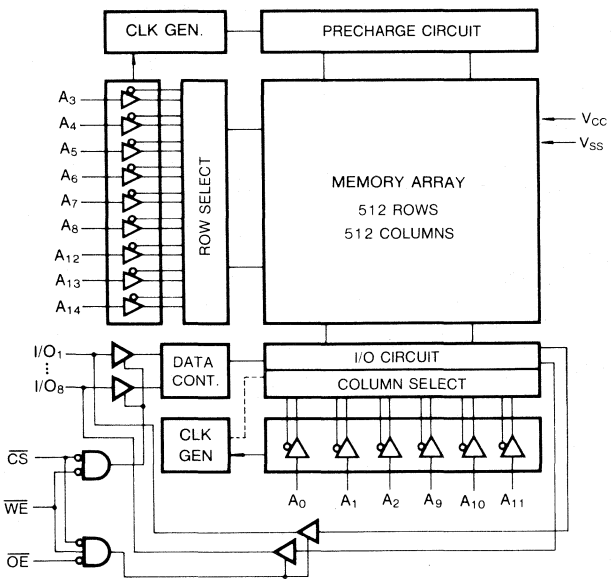
- **Industrial Temperature Range : -40 to 85℃**
- **Fast Access Time : 70,100ns(Max.)**
- **Low Power Dissipation**
  Standby (CMOS) : 275μW(Max.)
  Operating : 110mW(Max.)
- **Single 5V±10% power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - No clock or refresh required
- **Three State Outputs**
- **Low Data Retention Voltage: 2V(Min.)**
- **Jedec Standard Pin Configuration**
  KM62256CLGI/CLGI-L : 28-SOP-450
  KM62256CLTGI/CLTGI-L : 28-TSOP1-0813.4F
  KM62256CLRGI/CLRGI-L : 28-TSOP1-0813.4R

GENERAL DESCRIPTION

The KM62256CLI/CLI-L is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.
The device is fabricated using Samsung's advanced CMOS techology. The KM62256CLI/CLI-L has an output enable input for precise control of the data outputs.
It also has a chip enable input for the minimum current power down mode.
The KM62256CLI/CLI-L has been designed for high speed and low power application. It is particularly well suited for battery back-up memory application.
And - 40 to 85℃ operating temperature range makes it ideal for industrial use.

2

FUNCTIONAL BLOCK DIAGRAM

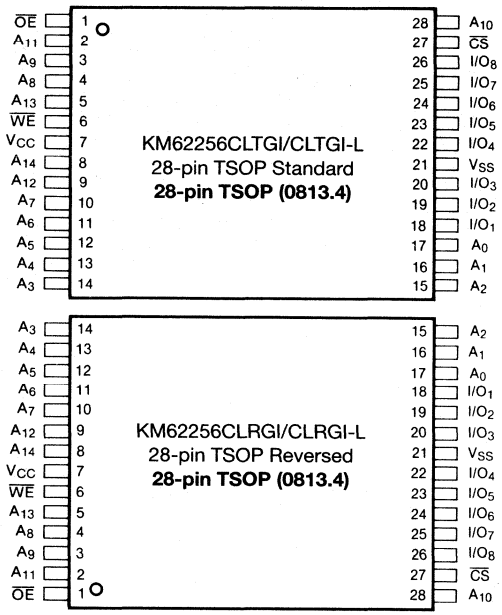


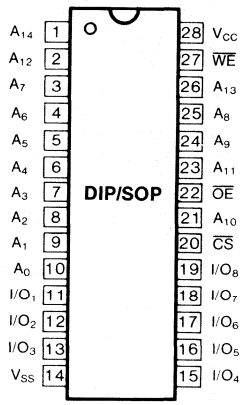
PIN CONFIGURATION (Top Views)

Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1~I/O_8	Data Inputs/Outputs
V_{CC}	Power(+5V)
V_{SS}	Ground

PIN CONFIGURATIONS (Top View)

28-pin TSOP (0813.4)





ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-40 to 85	°C
Soldering Temperature and Time	T_{SOLDER}	260°C, 10sec(Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A=-40 to 85°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.5	—	0.8	V

* V_{IL}(min.)=-3.0V for≤50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=-40 to 85°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-1		1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}		-1		1	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL} $I_{I/O}$=0mA			7	20	mA
Average Operating Current	I_{CC1}	Cycle Time=1μs, $\overline{CS}$≤0.2V, V_{IL}≤0.2V V_{IH}≥V_{CC}-0.2V, $I_{I/O}$=0mA				10	mA
	I_{CC2}	$\overline{CS}$=V_{IL}, Min. Cycle,100% Duty $I_{I/O}$=0mA				70	mA
Standby Power	I_{SB}	$\overline{CS}$=V_{IH}				2	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, V_{IN}≤0.2V	L-Ver			100	μA
		or V_{IN}≥V_{CC}-0.2V	LL-Ver			20	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA				0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1.0mA		2.4			V

* Typ : V_{CC}=5V, T_A=25°C

CAPACITANCE (f=1MHz, T_A=25°C)*

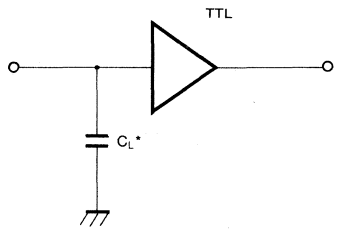
Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note : Capacitance is sampled and not 100% tested.

TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	C_L=100pF+1TTL Load

TEST CIRCUIT



*Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM62256CLGI-7 KM62256CLTGI-7		KM62256CLGI -10 KM62256CLTGI -10		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		100		ns
Address Access Time	t_{AA}		70		100	ns
Chip Select to Output	t_{CO}		70		100	ns
Output Enable to Valid Output	t_{OE}		35		50	ns
Chip Select to Low-Z Output	t_{LZ}	10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Chip Deselect to High-Z Output	t_{HZ}	0	30	0	35	ns
Output Disable to High-Z Output	t_{OHZ}	0	30	0	35	ns
Output Hold from Address Change	t_{OH}	5		10		ns

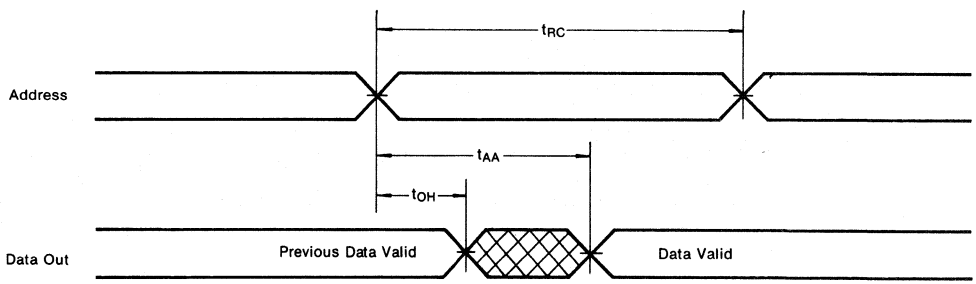
WRITE CYCLE

Parameter	Symbol	KM62256CLGI -7 KM62256CLTGI -7		KM62256CLGI -10 KM62256CLTGI -10		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		100		ns
Chip Select to End of Write	t_{CW}	60		80		ns
Address Set-up Time	t_{AS}	0		0		ns
Address Valid to End of Write	t_{AW}	60		80		ns
Write Pluse Width	t_{WP}	50		60		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to Output High-Z	t_{WHZ}	0	25	0	35	ns
Data to Write Time Overlap	t_{DW}	30		50		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Wirte to Output Low-Z	t_{OW}	5		10		ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

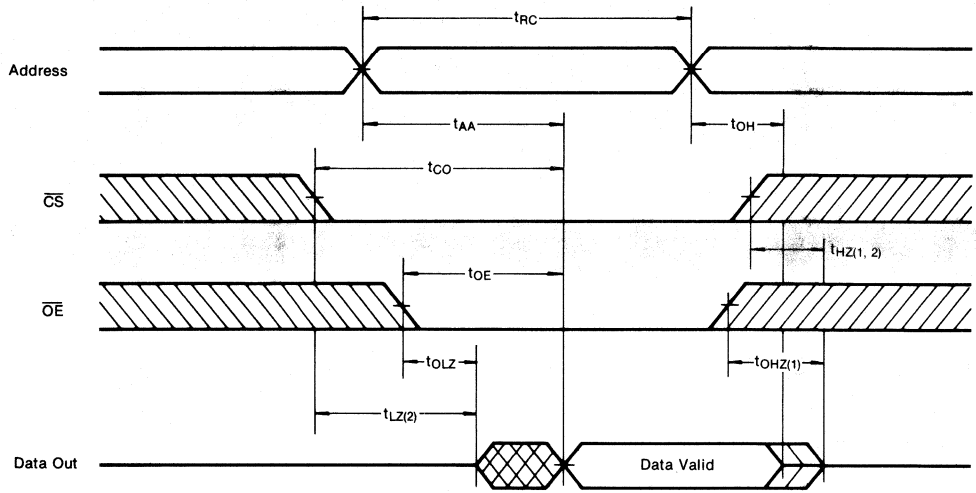
($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



SAMSUNG ELECTRONICS

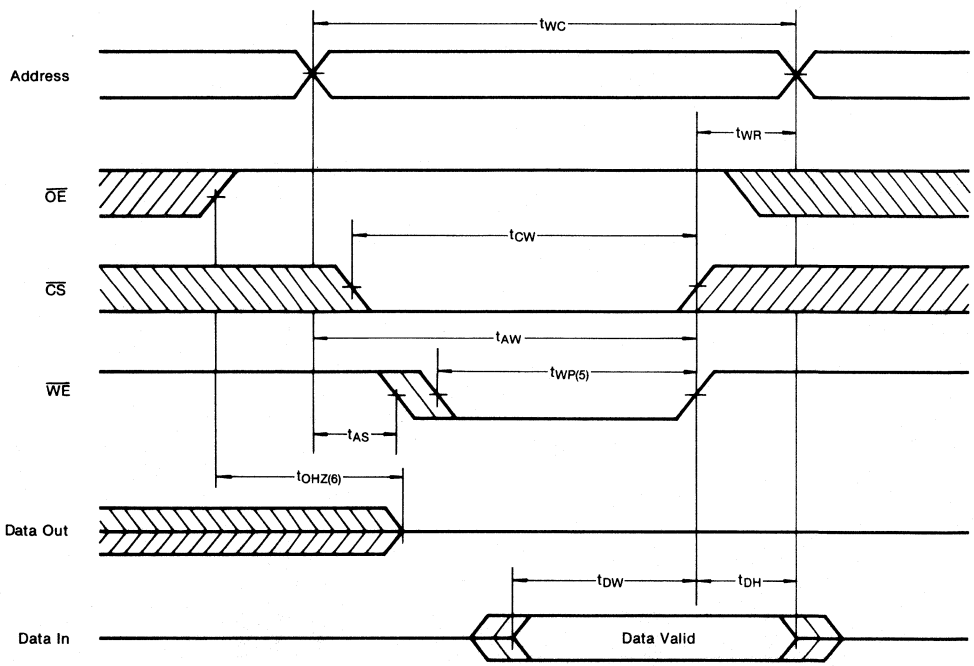
TIMING WAVEFORM OF READ CYCLE (2)

($\overline{WE}$ = V_{IH}) (Note 1, 2, 3, 4)



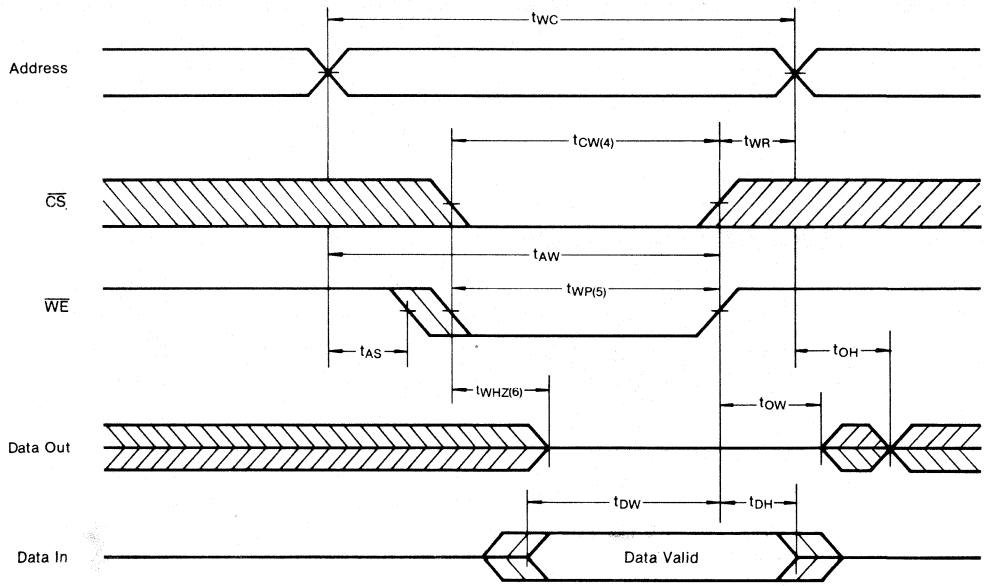
TIMING WAVEFORM OF WRITE CYCLE (3)

($\overline{OE}$ Clocked) (Note 5, 6, 7, 8)



TIMING WAVEFORM OF WRITE CYCLE (4)

($\overline{OE}$ Low Fixed) (Note 5, 6, 7, 8, 9)



Notes

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to the V_{OH} or V_{OL} level.
2. At any given temperature and voltage condition t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ transition Low.
5. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and $\overline{WE}$.
6. During this period, I/O pins are in the output state. The input signals out of phase must not applied.
7. $\overline{CS}$ or WE must be high during address transition state.
8. If $\overline{OE}$ is high, I/O pins remain in a high-impedance state.
9. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

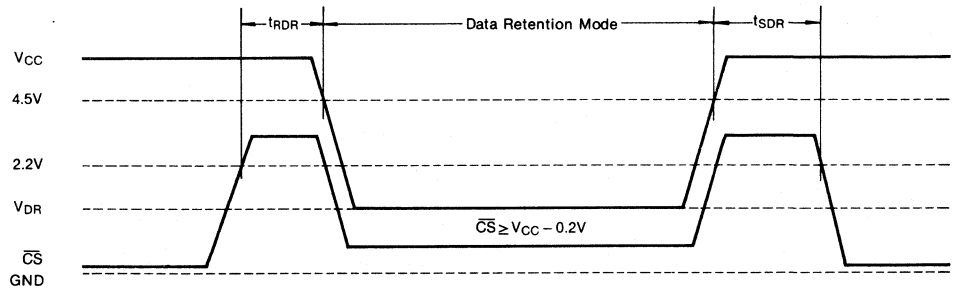
* X means Don't Care.

DATA RETENTION CHARACTERISTICS (T_A=-40 to 85°C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V		2.0		5.5	V
Data Retention Current	I_{DR}	V_{CC}=3V	L	-		50	μA
		$\overline{CS} \geq V_{CC}$-0.2V	LL	-		10	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention		0			ns
Recovery Time	t_{RDR}	Waveforms(below)		t_{RC}*			ns

* Read Cycle Time

DATA RETENTION WAVEFORM (CS Controlled)



65,536 WORD × 8 Bit High Speed CMOS Static RAM

FEATURES

- **Fast Access Time 70, 85, 100ns (max.)**
- **Low Power Dissipation**
  - **Standby (CMOS): 10μW (typ.) L-Version**
  - **5μW (typ.) LL-Version**
  - **Operating : 55mW/1MHz (Max.)**
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  - **—No clock or refresh required**
- **Three State Outputs**
- **Low Data Retention Voltage: 2V (Min.)**
- **Standard Pin Configuration**
  - **KM68512LG/LG-L: 32-SOP-525**
  - **KM68512LT/LT-L : 32-TSOP1-0820F**

GENERAL DESCRIPTION

The KM68512L/L-L is a 524,288-bit high-speed Static Random Access Memory organized as 65,536 words by 8 bits.

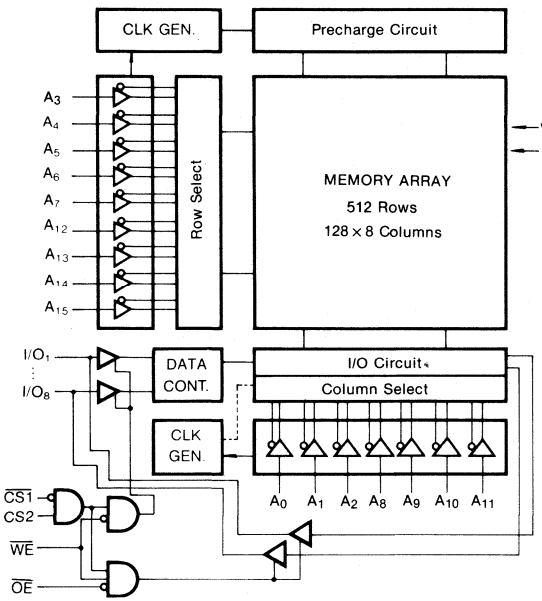
The KM68512L/L-L uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.

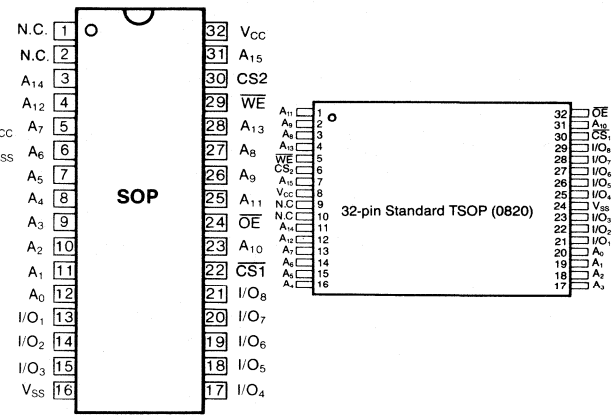
The KM68512L/L-L is particularly well suited for use in high-density high-speed system and low power app-lications.

It is particularly well suited for battery back-up nonvolatile memory application.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Pin Name	Pin Function
A_0-A_{15}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS1}$, CS2	Chip Select Inputs
$\overline{OE}$	Output Enable Input
I/O_1-I/O_8	Data Inputs/Qutputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{SOLDER}	260°C, 10 sec (Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

* V_{IL}(min.) = −3.0V for ≤50 ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}		−1	—	1	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$=V_{IH} $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}		−1	—	1	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH} V_{IN} = V_{IL} or V_{IH}, $I_{I/O}$ = 0mA		—	7	15	mA
Average Operating Current	I_{CC1}	Cycle Time = 1μs, 100% Duty $\overline{CS1}$ ≤ 0.2V, CS2 ≥ V_{CC} − 0.2V V_{IL} ≤ 0.2V, V_{IH} ≥ V_{CC} − 0.2V, $I_{I/O}$ = 0mA		—	—	10	mA
	I_{CC2}	Min Cycle, 100% Duty $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, $I_{I/O}$ = 0mA		—	—	70	mA
Standby Power Current	I_{SB}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL}		—	—	3	mA
	I_{SB1}	$\overline{CS1}$ ≥ V_{CC} − 0.2V, CS2 ≥ V_{CC} − 0.2V or CS2 ≤ 0.2V	L	—	2	100	μA
			LL	—	1	20	μA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −1.0mA		2.4	—	—	V

* Typ: V_{CC} = 5V, T_A = 25°C

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

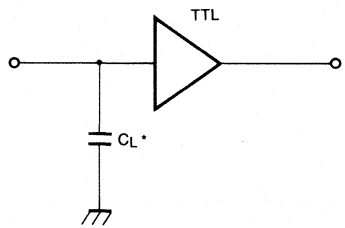
Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF

Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS ($T_A = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V
Output Load	$C_L = 100*pF + 1$ TTL

TEST CIRCUIT



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68512-7/7L		KM68512-8/8L		KM68512-10/10L		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		ns
Address Access Time	t_{AA}		70		85		100	ns
Chip Select to Output	t_{CO1}, t_{CO2}		70		85		100	ns
Output Enable to Output	t_{OE}		35		45		50	ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5	5	ns
Chip Enable to Low-Z Output	t_{LZ1}, t_{LZ2}	10		10		10		ns
Output Disable to High-Z Output	t_{OHZ}	0	25	0	30	0	30	ns
Chip Disable to High-Z Output	t_{HZ1}, t_{HZ2}	0	25	0	30	0	30	ns
Output Hold from Address Change	t_{OH}	10		10		15		ns

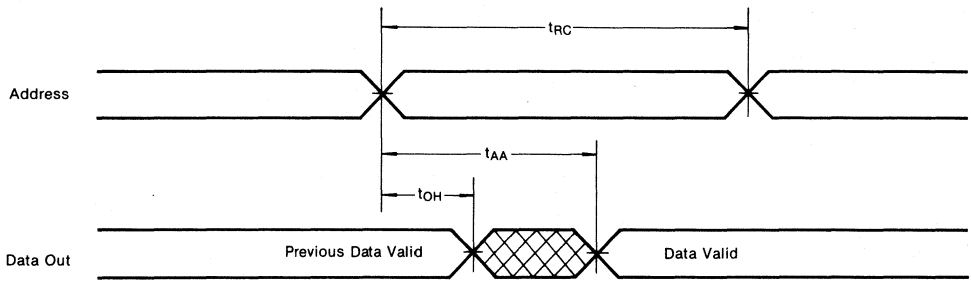
WRITE CYCLE

Parameter	Symbol	KM68512-7/7L		KM68512-8/8L		KM68512-10/10L		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		ns
Chip Select to End of Write	t_{CW}	60		70		80		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	60		70		80		ns
Write Pulse Width	t_{WP}	50		55		60		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WHZ}	0	25	0	30	0	30	ns
Data to Write Time Overlap	t_{DW}	30		35		40		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End of Write to Output Low-Z	t_{OW}	5		5		5		ns

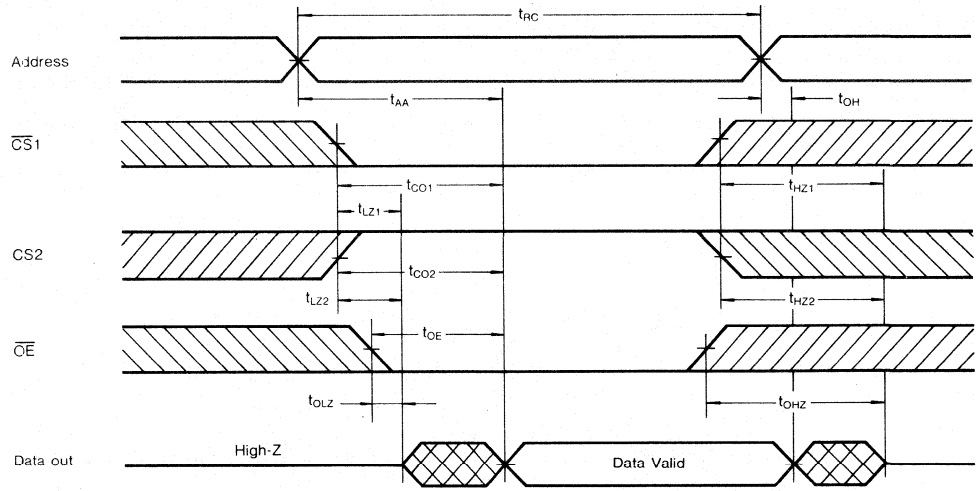
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS1} = \overline{OE} = V_{IL}$, $CS2 = V_{IH}$, $\overline{WE} = V_{IH}$)



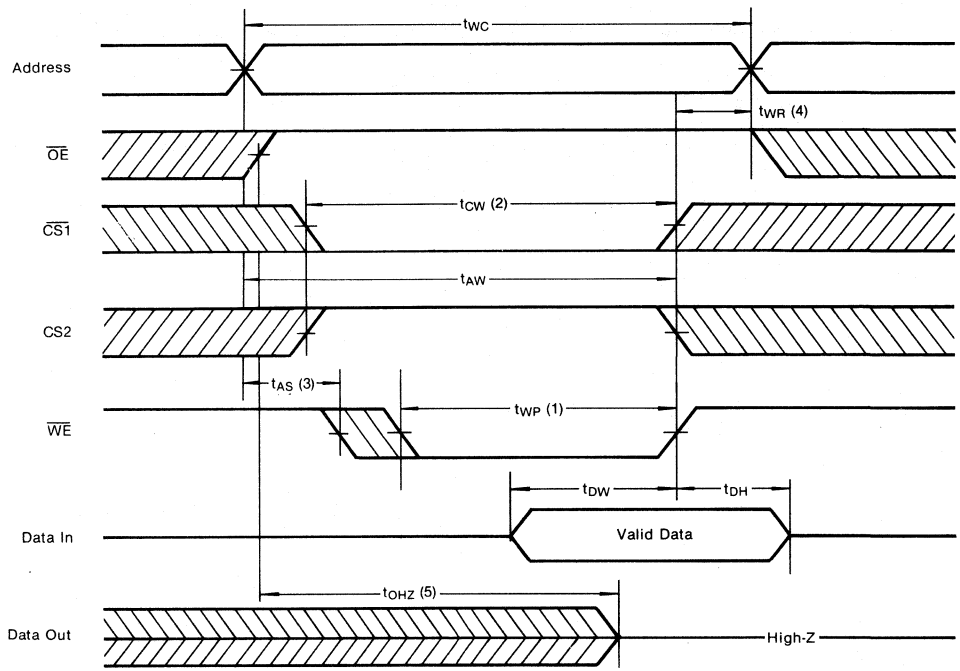
TIMING WAVEFORM OF READ CYCLE (2) ($\overline{WE}$ = V_{IH})



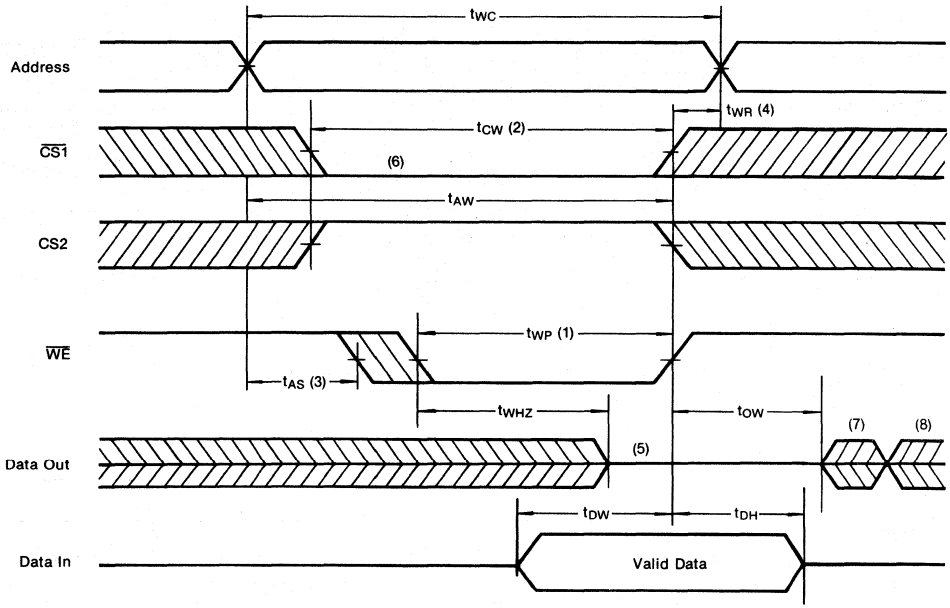
Notes (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. This parameter is sampled and not 100% tested.
2. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{OE}$ Low Fixed)



Notes (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write end as $\overline{CS1}$, or $\overline{WE}$ going high, or CS2 going low.
5. During this period, I/O pins are in the output state, therefore, the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the same phase of the latest written data in this write cycle.
8. D_{OUT} is the read data of next address.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

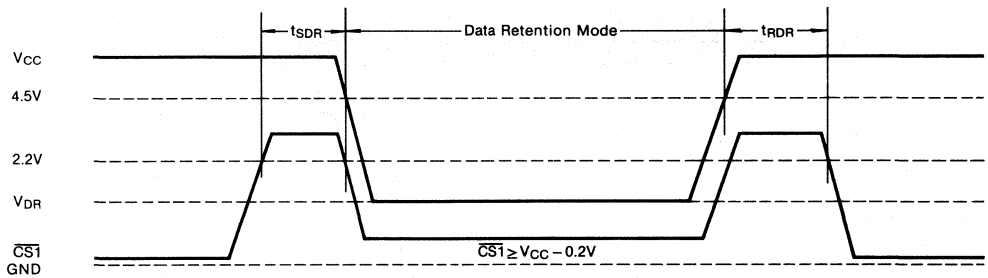
DATA RETENTION CHARACTERISTICS (T_A = 0 to 70°C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	CS1* ≥ V_{CC} − 0.2V		2.0	—	5.5	V
Data Retention Current	I_{DR}	V_{CC} = 3.0V CS1 ≥ V_{CC} − 0.2V	L	—	1	50	μA
			LL	—	0.5	10	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)		0	—	—	ns
Recovery Time	t_{RDR}			t_{RC}**	—	—	ns

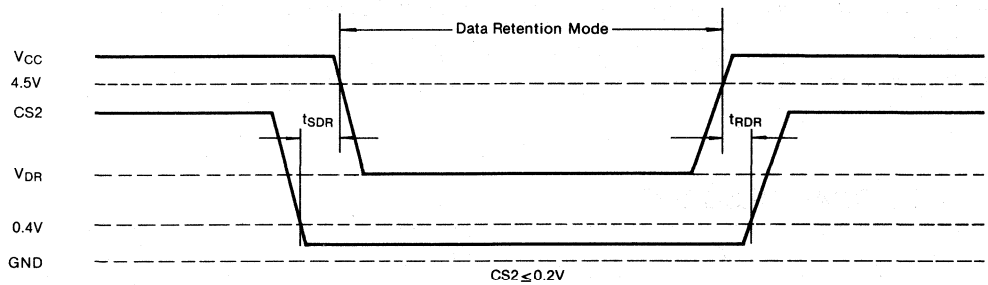
* : CS1 ≥ V_{CC} − 0.2, CS2 ≥ V_{CC} − 0.2 (CS1 Controlled) or CS2 ≤ 0.2 (CS2 Controlled)
** : Read Cycle Time

2

DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM (2) (CS2 Controlled)



65,536 WORD x 8 Bit High Speed CMOS Static RAM

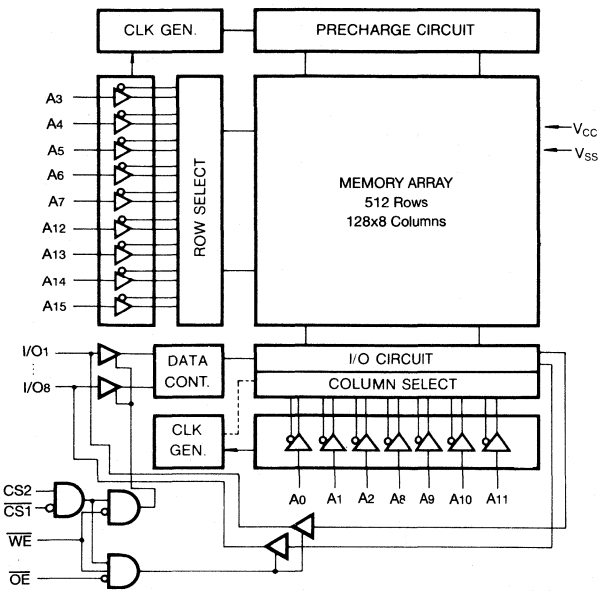
FEATURES

- **Fast Access Time : 55, 70ns(Max.)**
- **Low Power Dissipation**
  Standby (CMOS) : 10μW(Typ.) L-Version
  5μW(Typ.) LL-Version
  Operating : 35mW(Typ.)
- **Single 5±10%V power supply**
- **TTL Compatible inputs and outputs**
- **Fully Static Operation**
  - No clock or refresh required
- **Three State Output**
- **Low Data Retention Voltage: 2V(Min.)**
- **Standard Pin Configuration**
  KM68512ALG/ALG-L : 32-SOP-525
  KM68512ALT/ALT-L : 32-TSOP1-0820F

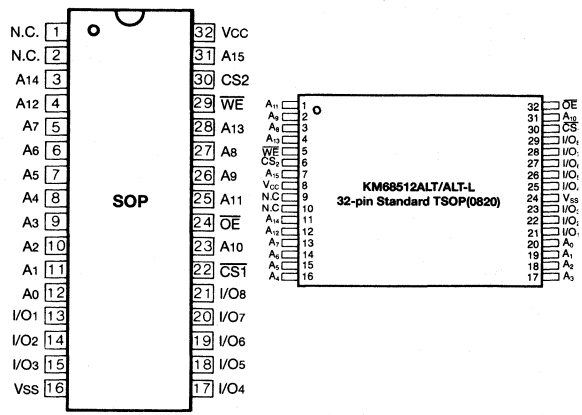
GENERAL DESCRIPTION

The KM68512AL/AL is a 524,288-bit high speed Static Random Access Memory organized as 65,536 words by 8 bits.
The KM68512AL/AL-L uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applicatians.
It is particularly well suited for use in high-density high-speed system and low power applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A0-A15	Address Inputs
$\overline{WE}$	Write Enable input
$\overline{CS1}$, CS2	Chip Select Input
$\overline{OE}$	Output Enable input
I/O1~I/O8	Data Inputs/Outputs
VCC	Power(+5V)
VSS	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{SOLDER}	260°C, 10sec(Lead only)	—

* Stresses greater than those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.3*	—	0.8	V

* V_{IL}(min.)=-3.0V for≤50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5±10%, unless otherwise specified)

Items	Symbol	Test Condition		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-1		+1	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}		-1		+1	μA
DC operating Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, CS2=V_{IH} V_{IN}=V_{IL} or V_{IH}, $V_{I/O}$=0mA			7	15	mA
Average Operating Current	I_{CC1}	Cycle Time=1μs, 100% Duty $\overline{CS1}$≤0.2V, CS2≥ V_{CC}-0.2V $I_{I/O}$=0mA, V_{IL}≤0.2V, V_{IH}≥V_{CC}-0.2V				10	mA
	I_{CC2}	Min Cycle,100% Duty $I_{I/O}$=0mA, $\overline{CS1}$=V_{IL}, CS2=V_{IH}				70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}				3	mA
	I_{SB1}	$\overline{CS1}$≥V_{CC}-0.2V	L		2	100	μA
		CS2≥V_{CC}-0.2V or CS2≤0.2V	LL		1	20	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA				0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1.0mA		2.4			V

* Typ : V_{CC}=5V, T_A=25°C

CAPACITANCE (f=1MHz, T_A=25°C)*

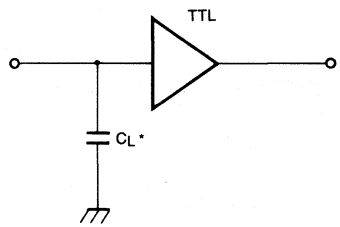
Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note : Capacitance is sampled and not 100% tested.

TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	C_L*=100pF+1TTL

TEST CIRCUIT



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68512A-5		KM68512A-7		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	55		70		ns
Address Access Time	t_{AA}		55		70	ns
Chip Select to Output	t_{CO1},t_{CO2}		55		70	ns
Output Enable to Output	t_{OE}		25		35	ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Chip Enable to Low-Z Output	t_{LZ1},t_{LZ2}	10		10		ns
Output Disable to High-Z Output	t_{OHZ}	0	20	0	25	ns
Chip Disable to High-Z Output	t_{HZ1},t_{HZ2}	0	20	0	25	ns
Output Hold from Address Change	t_{OH}	10		10		ns

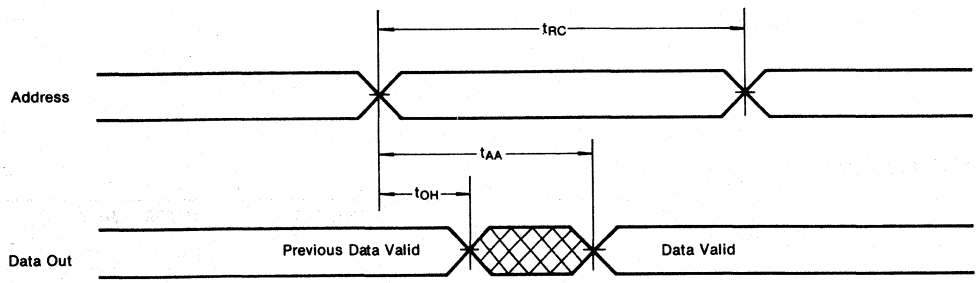
READ CYCLE

Parameter	Symbol	KM68512A-5		KM68512A-7		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	55		70		ns
Chip Select to End of Write	t_{CW}	45		60		ns
Address Set-up Time	t_{AS}	0		0		ns
Address Valid to End of Write	t_{AW}	50		60		ns
Write Pulse Width	t_{WP}	40		50		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to Output High-Z	t_{WHZ}	0	20	0	25	ns
Data to Write Time Overlap	t_{DW}	25		30		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End of Write to Output Low-Z	t_{OW}	5		5		ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS1} = \overline{OE} = V_{IL}$, $CS2 = V_{IH}$, $\overline{WE} = V_{IH}$)



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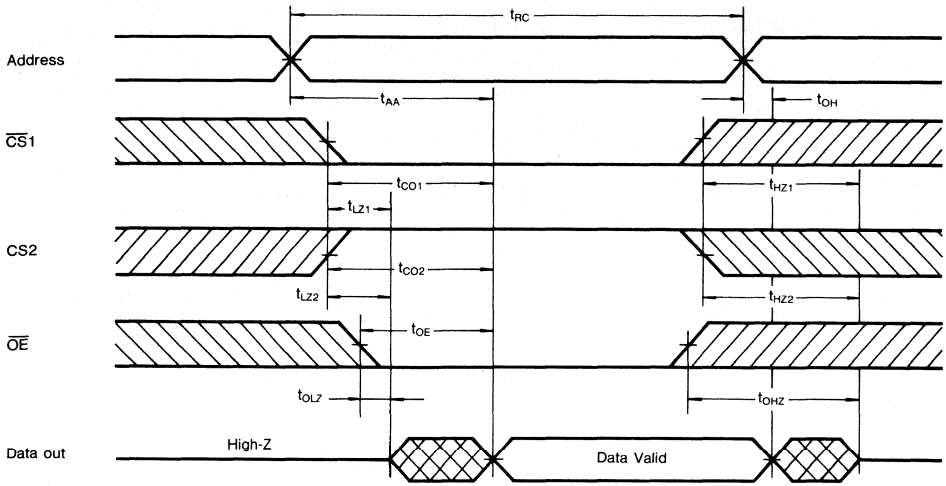
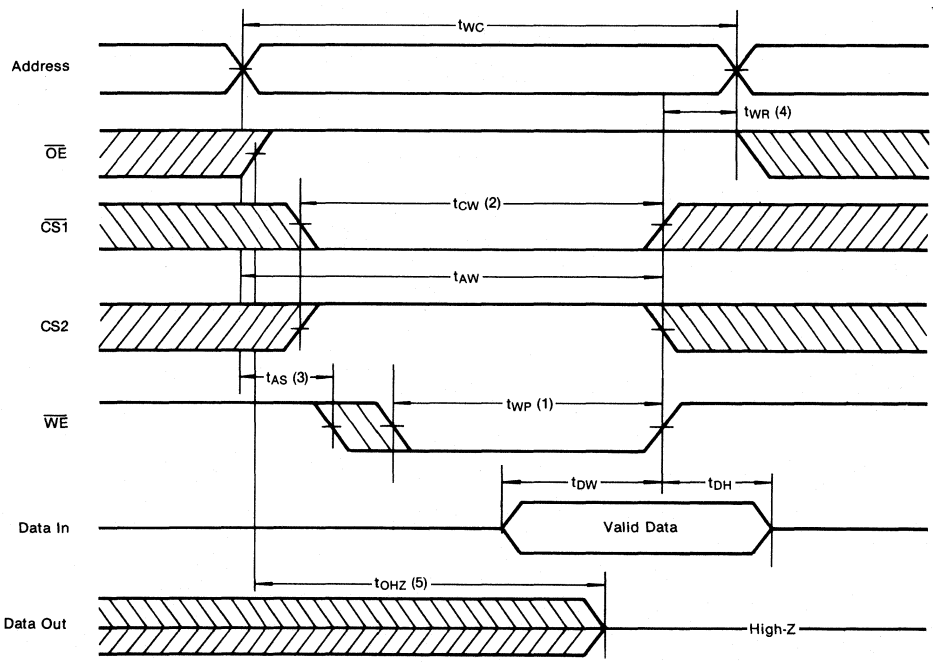
TIMING WAVEFORM OF READ CYCLE (2) ($\overline{WE}$ = V_{IH})



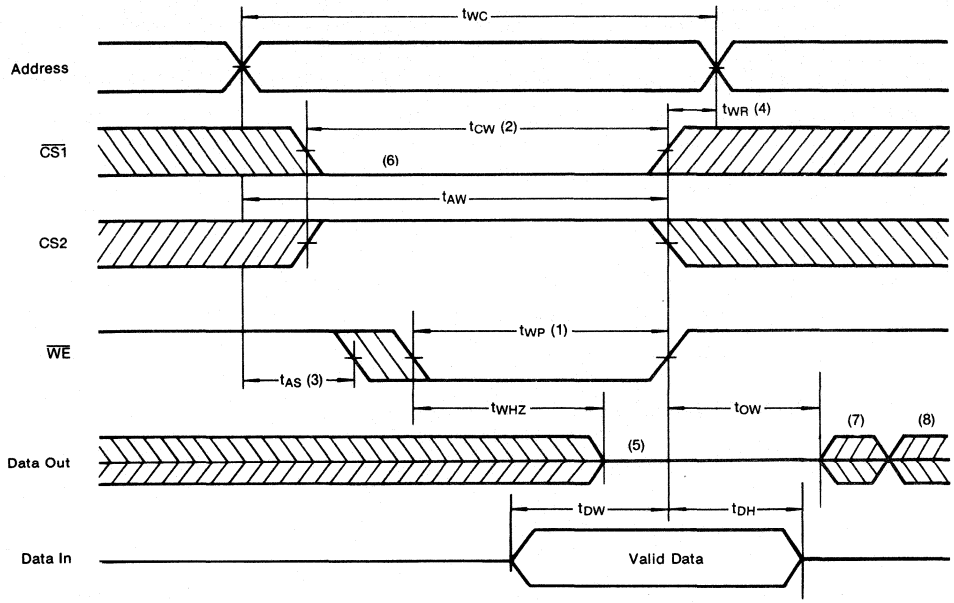
Notes (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. This parameter is sampled and not 100% tested.
2. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{OE}$ Low Fixed)



Notes (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write end as $\overline{CS1}$, or $\overline{WE}$ going high, or CS2 going low.
5. During this period, I/O pins are in the output state, therefore, the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the same phase of the latest written data in this write cycle.
8. D_{OUT} is the read data of next address.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

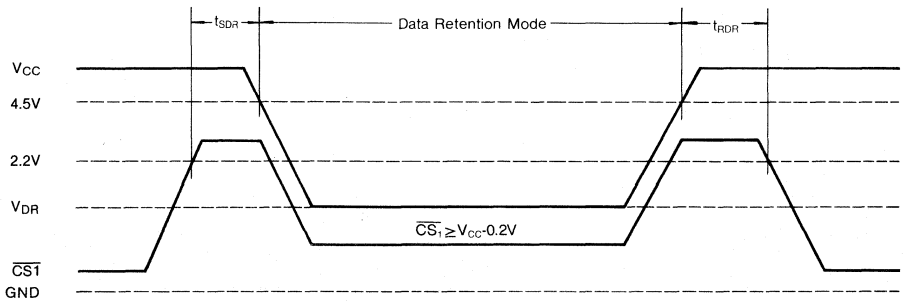
* Note: X means Don't Care.

DATA RETENTION CHARACTERISTICS (T_A=0 to 70°C)

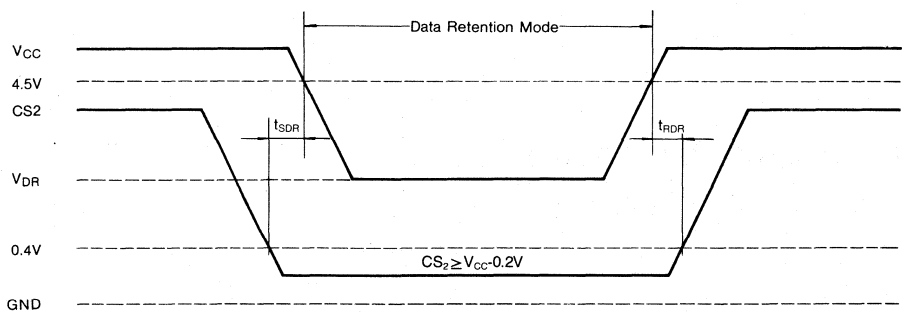
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1} \geq V_{CC}$-0.2V		2.0		5.5	V
Data Retention Current	I_{DR}	V_{CC}=3.0V	L		1	50	μA
		$\overline{CS1} \geq V_{CC}$-0.2V	LL		0.5	10	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention		0			ns
Recovery Time	t_{RDR}	Waveforms(below)		t_{RC}**			ns

* $\overline{CS1} \geq V_{CC}$-0.2, CS2 $\geq V_{CC}$-0.2(CS1 Controlled) or CS2 $\leq$ 0.2(CS2 Controlled)
** Read Cycle Time

DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM (2) (CS2 Controlled)



131,072 WORD x 8 Bit CMOS Static RAM

FEATURES

- **Fast Access Time : 55, 70, 85, 100ns(Max.)**
- **Low Power Dissipation**
  Standby (CMOS) : 10μW(Typ.) L-Version
  5μW(Typ.) LL-Version
  Operating : 55mW/1MHz (Max.)
- **Single 5±10%V power supply**
- **TTL Compatible inputs and outputs**
- **Fully Static Operation**
  - No clock or refresh required
- **Three State Output**
- **Low Data Retention Voltage: 2V(Min)**
- **Standard Pin Configuration**
  KM681000BLP/BLP-L : 32-DIP-600
  KM681000BLG/BLG-L : 32-SOP-525
  KM681000BLT/BLT-L : 32-TSOP1-0820F
  KM681000BLR/BLR-L : 32-TSOP1-0820R

GENERAL DESCRIPTION

The KM681000BL/BL-L is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits.
The device is fabricated using Samsung's advanced CMOS process.
The KM681000BL/BL-L has an output enable input for precise control of the data outputs.
It also has a chip enable input for the minimum current power down mode.
The KM681000BL/BL-L has been designed for high speed and low power applications.
It is particularly well suited for low battery back-up nonvolatile memory application.

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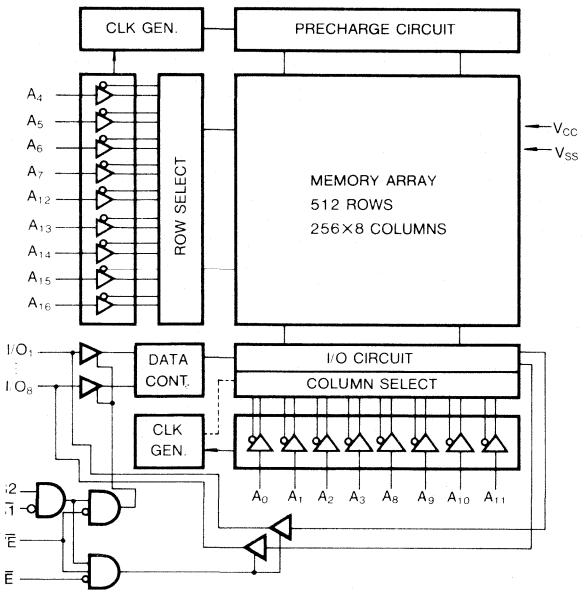
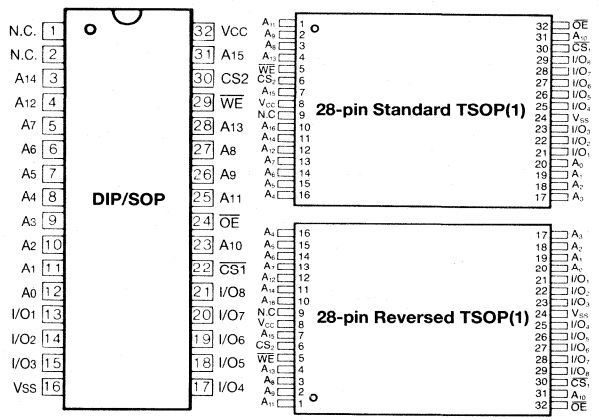
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A16	Address Inputs
$\overline{WE}$	Write Enable input
$\overline{CS1}$, CS2	Chip Seet Input
$\overline{OE}$	Output Enable input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power(+5V)
Vss	Ground
N.C.	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{SOLDER}	260°C, 10sec(Lead only)	—

* Stresses greater than those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.5*	—	0.8	V

* V_{IL}(min.)=-3.0V for$\leq$50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5$\pm$10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CC}		-1		$\pm$1	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL}, $V_{I/O}$=Vss to V_{CC}		-1		$\pm$1	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, CS2=V_{IH} V_{IN}=V_{IL} or V_{IH}, $V_{I/O}$=0mA			7	15	mA
Average Operating Current	I_{CC1}	Cycle Time=1μs, 100% Duty $\overline{CS1}\leq$0.2V, CS2$\geq$$V_{CC}$-0.2V $I_{I/O}$=0mA				10	mA
	I_{CC2}	Min Cycle,100% Duty $I_{/O}$=0mA $\overline{CS1}$=V_{IL}, CS2=V_{IH}				70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}				3	mA
	I_{SB1}	$\overline{CS1}\geq V_{CC}$-0.2V	L		2	100	μA
		$\overline{CS1}\geq V_{CC}$-0.2V or CS2$\leq$0.2V	L-L		1	20	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA				0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1.0mA		2.4			V

* Typ : V_{CC}=5V, T_A=25°C

CAPACITANCE (f=1MHz, T_A=25°C)

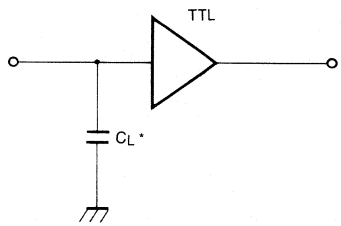
Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note : Capacitance is sampled and not 100% tested.

TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	C_L=100pF+1TTL

TEST CIRCUIT



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM681000BL-5 KM681000BL-5L		KM681000BL-7 KM681000BL-7L		KM681000BL-8 KM681000BL-8L		KM681000BL-10 KM681000BL-10L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	55		70		85		100		ns
Address Access Time	t_{AA}		55		70		85		100	ns
Chip Select to Output	t_{CO1}, t_{CO2}		55		70		85		100	ns
Output Enable to Valid Output	t_{OE}		25		35		45		50	ns
Chip Enable to Low-Z Output	t_{LZ1}, t_{LZ2}	10		10		10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5		5		ns
Chip Disable to High-Z Output	t_{HZ1}, t_{HZ2}	0	20	0	25	0	30	0	30	ns
Output Disable to High-Z Output	t_{OHZ}	0	20	0	25	0	30	0	30	ns
Output Hold from Address Change	t_{OH}	10		10		10		15		ns

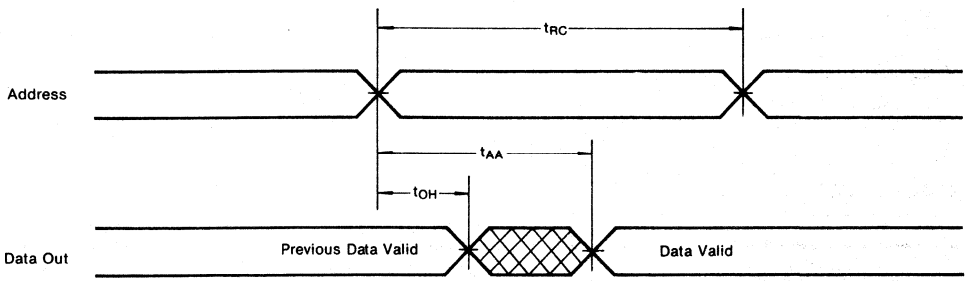
WRITE CYCLE

Parameter	Symbol	KM681000BL-5 KM681000BL-5L		KM681000BL-7 KM681000BL-7L		KM681000BL-8 KM681000BL-8L		KM681000BL-10 KM681000BL-10L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	55		70		85		100		ns
Chip Select to End of Write	t_{CW}	50		60		70		80		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AW}	45		60		70		80		ns
Write Pulse Width	t_{WP}	40		50		55		60		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WHZ}	0	20	0	25	0	30	0	35	ns
Data to Write Time Overlap	t_{DW}	25		30		35		40		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End of Write to Output Low-Z	t_{OW}	5		5		5		5		ns

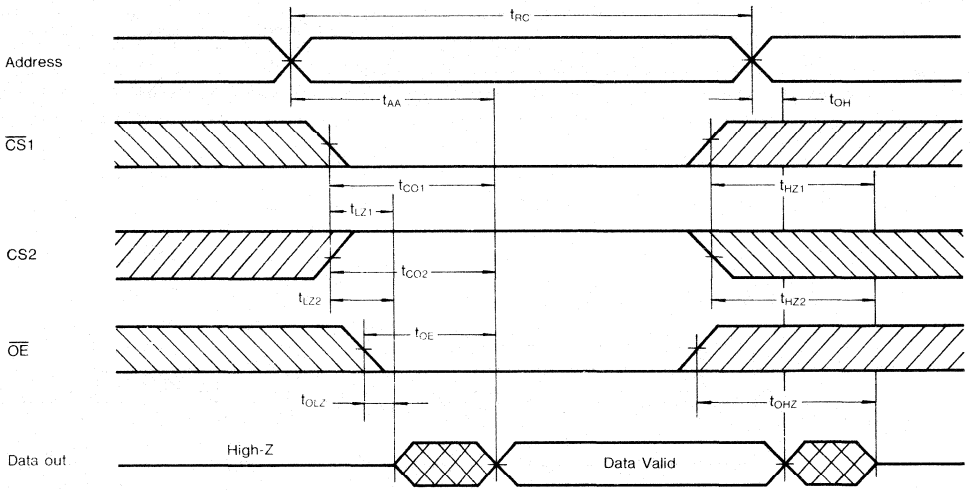
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$ = $\overline{OE}$ V_{IL}, $\overline{WE}$ = V_{IH})



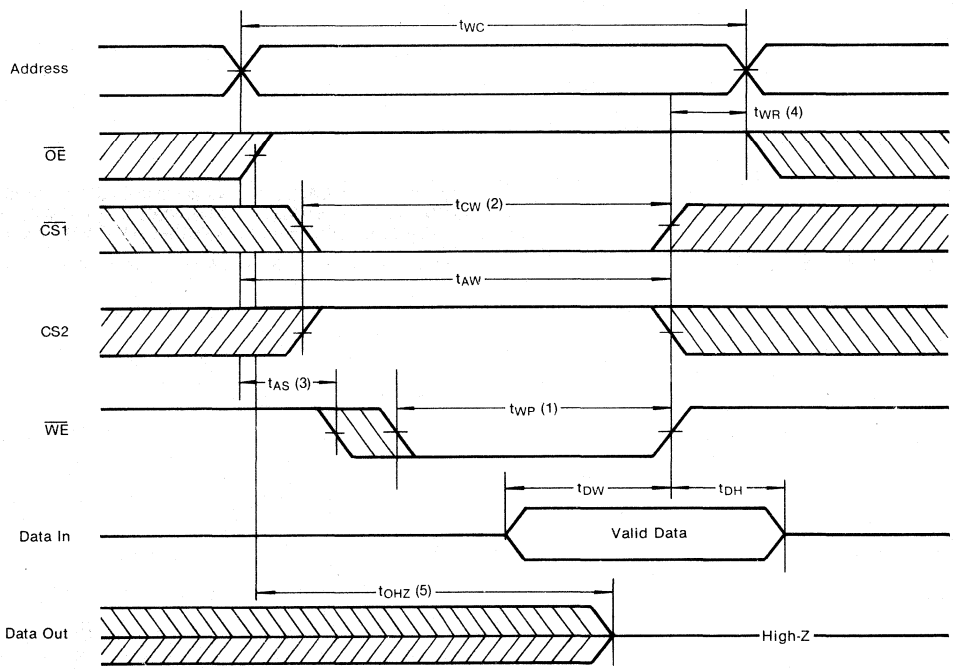
TIMING WAVEFORM OF READ CYCLE (2) ($\overline{WE}$ = V_{IH})



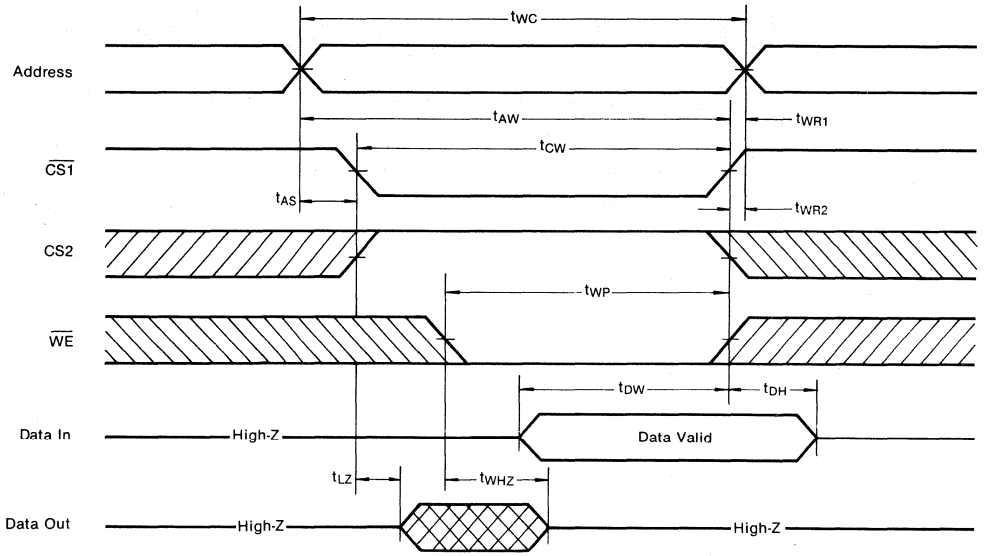
Notes (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. This parameter is sampled and not 100% tested.
2. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.

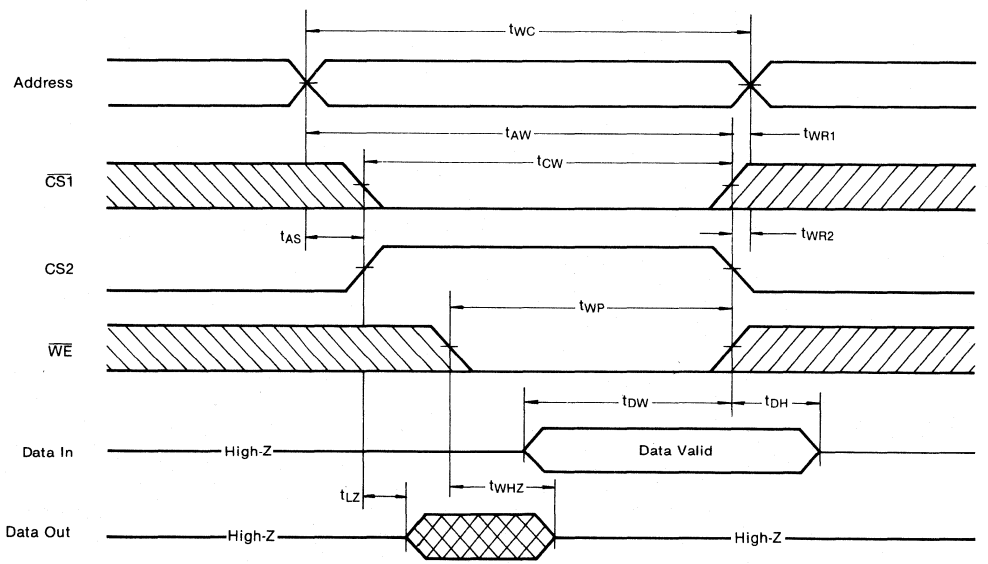
TIMING WAVEFORM OF WRITE CYCLE (1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (3) ($\overline{CS2}$ Controlled)



Notes(WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends at $\overline{CS1}$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS2 going low
5. If $\overline{OE}$, CS2 and $\overline{WE}$ are in the read mode during this period, the I/O pins are in the output low-Z state, inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the read data of next address.
8. When $\overline{CS1}$ is low and CS2 is high: 1/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

2

FUNCTIONAL DESCRIPTION

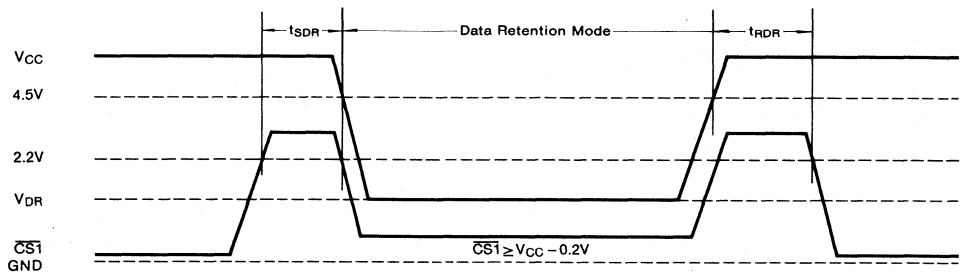
$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Vcc Current
H	X*	X	X	Power down	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Power down	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

DATA RETENTION CHARACTERISTICS (T_A=0 to 70°C)

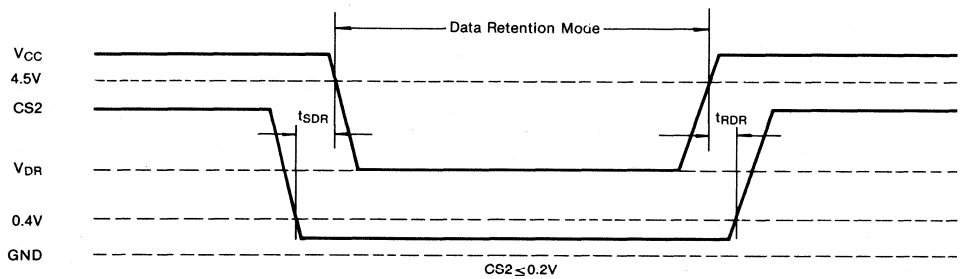
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1}$(1)≥V_{CC}-0.2V		2.0		5.5	V
Data Retention Current	I_{DR}	V_{CC}=3.0V	L		1	50(2)	μA
		$\overline{CS1}$≥V_{CC}-0.2V	LL		0.5	10(3)	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention		0			ns
Recovery Time	t_{RDR}	Waveforms(below)		t_{RC}(4)			ns

(1) $\overline{CS1}$≥V_{CC}-0.2, CS2≥V_{CC}-0.2($\overline{CS1}$ Controlled) or CS2≤0.2(CS2 Controlled)
(2) 20μA(max.) at 0°C to 40°C(Guaranteed only for L-version)
(3) 3μA(max.) at 0°C to 40°C(Guaranteed only for LL-version)
(4) t_{RC}=Read Cycle Time

DATA RETENTION WAVEFORM 1 ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM 2 (CS2 Controlled)



131,072 WORD x 8 Bit CMOS Static RAM *(Industrial Temperature Range Operation)*

FEATURES

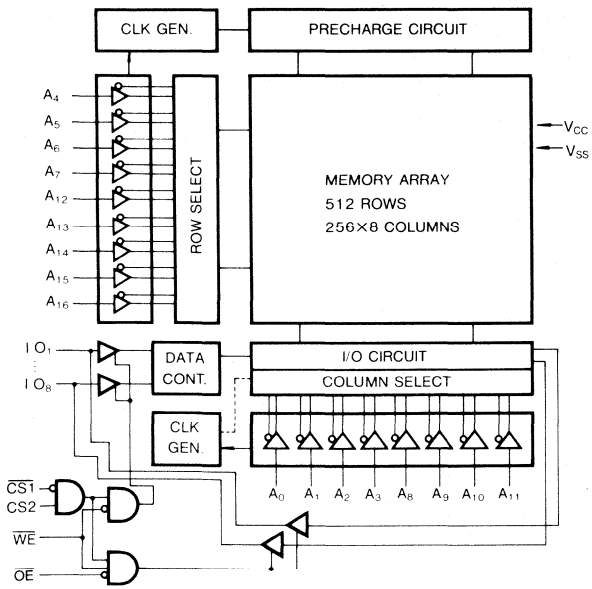
- **Industrial Temperature Range : -40 to 85° C**
- **Fast Access Time: 70, 100ns(max.)**
- **Low Power Dissipation**
  Standby (CMOS) : 550μW(max.)
  : 275μW(max.)
  Operating : 110mW(max.)
- **Single 5V±10% power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - No clock or refresh required
- **Three State Output**
- **Low Data Retention Voltage: 2V(Min)**
- **JedecStandard pin coniguration**
  KM681000BLGI/BLG-L : 32-SOP-525
  KM681000BLTI/BLTI-L : 32-TSOP1-0820F
  KM681000BLRI/BLRI-L : 32-TSOP1-0820R

GENERAL DESCRIPTION

The KM681000BLI/BLI-L is a 1,048,576-bit high speed Static Random Access Memory organized as 131,072 words by 8 bits.
The device is fabricated using Samsung's advanced CMOS technology.
The KM681000BLI/BLI-L has an output enable input for precise control of the data outputs. It also has chip enable inputs for the minimum current power down mode.
The KM681000BLI/BLI-L has been designed for high speed and low power applications. It is particularly well suited for battery back-up memory application.
And -40 to 85° C operating temperature range makes it ideal for industrial use.

2

FUNCTIONAL BLOCK DIAGRAM

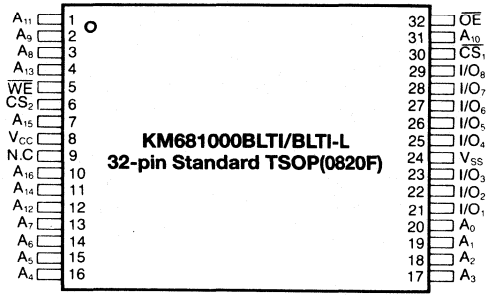


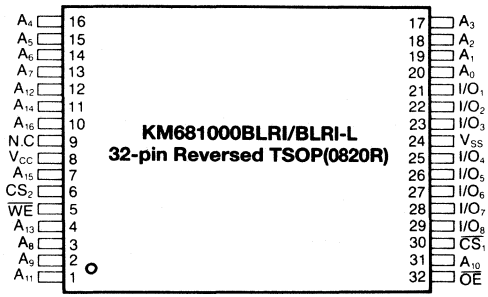
PIN CONFIGURATION

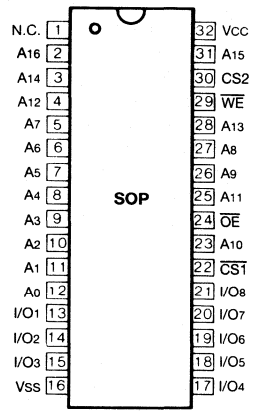
Pin Name	Pin Function
A0-A16	Address Inputs
$\overline{WE}$	Write Enable input
$\overline{CS1}$, CS2	Chip Select Input
$\overline{OE}$	Output Enable input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power(+5V)
Vss	Ground
N.C.	No Connection

SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top Views)







ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-40 to 85	°C
Soldering Temperature and Time	T_{SOLDER}	260°C, 10sec(Lead only)	—

* Stresses greater than those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED OPERATING CONDITIONS (T_A=-40 to 85°C)

item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.5	—	0.8	V

* V_{IL}(min.)=-3.0V for $\leq$50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=-40 to 85°C, V_{CC}=5$\pm$10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-1		1	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}		-1		1	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, CS2=V_{IH} V_{IN}=V_{IL} or V_{IH}, $V_{I/O}$=0mA			7	20	mA
Average Operating Current	I_{CC1}	Cycle Time=1μs, 100% Duty $\overline{CS1}\leq$0.2V, CS2$\geq$ V_{CC}-0.2V $I_{I/O}$=0mA, $V_{IL}\leq$0.2V, $V_{IH}\geq V_{CC}$-0.2V				15	mA
	I_{CC2}	Min Cycle,100% Duty $\overline{CS1}$=V_{IL}, CS2=V_{IH}, $I_{I/O}$=0mA				70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}				3	mA
	I_{SB1}	$\overline{CS1}\geq V_{CC}$-0.2V,	L		2	100	μA
		CS2$\geq V_{CC}$-0.2V or CS2$\leq$0.2V	LL		1	50	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA				0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1.0mA		2.4			V

* Typ : V_{CC}=5V, T_A=25°C

CAPACITANCE (f=1MHz, T_A=25°C)

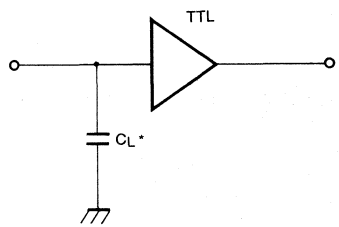
Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note : Capacitance is sampled and not 100% tested.

TEST CONDITIONS (T_A=-40 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	C_L=100pF+1TTL

TEST CIRCUIT



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM681000BLPI-7/7L KM681000BLGI-7/7L		KM681000BLPI-10/10L KM681000BLGI-10/10L		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		100		ns
Address Access Time	t_{AA}		70		100	ns
Chip Select to Output	t_{CO1}, t_{CO2}		70		100	ns
Output Enable to Valid Output	t_{OE}		35		50	ns
Chip Select to Low-Z Output	t_{LZ1}, t_{LZ2}	10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Chip Disable to High-Z Output	t_{HZ1}, t_{HZ2}	0	25	0	30	ns
Output Disable to High-Z Output	t_{OHZ}	0	25	0	30	ns
Output Hold from Address Change	t_{OH}	10		10		ns

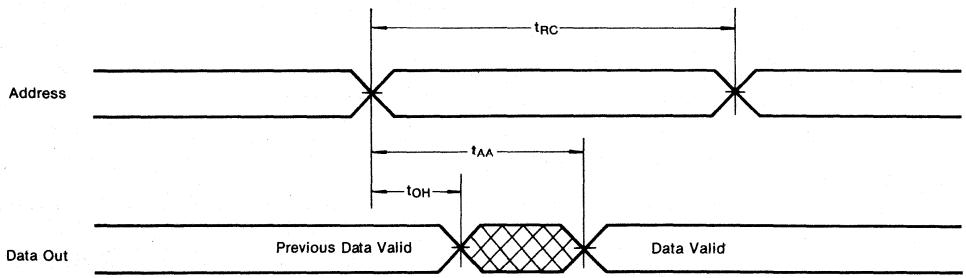
WRITE CYCLE

Parameter	Symbol	KM62256BLI-7 KM62256BLGI-7		KM62256BLI-10 KM62256BLGI-10		Units
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		100		ns
Chip Select to End of Write	t_{CW}	60		80		ns
Address Set-up Time	t_{AS}	0		0		ns
Address Valid to End of Write	t_{AW}	60		80		ns
Write Pulse Width	t_{WP}	50		60		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to Output High-Z	t_{WHZ}	0	25	0	30	ns
Data to Write Time Overlap	t_{DW}	30		40		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Output Low-Z	t_{OW}	5		10		ns

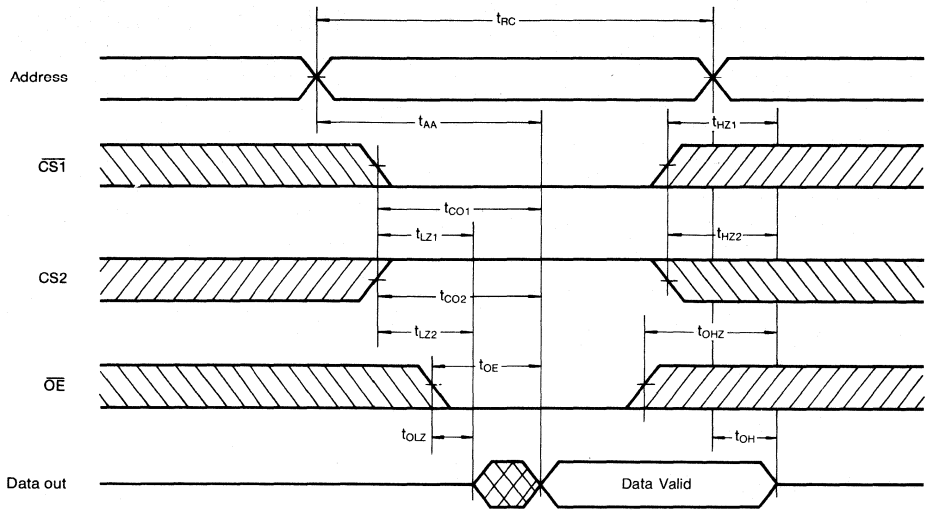
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

(CS=OE, V_{IL}, WE=V_{IH})



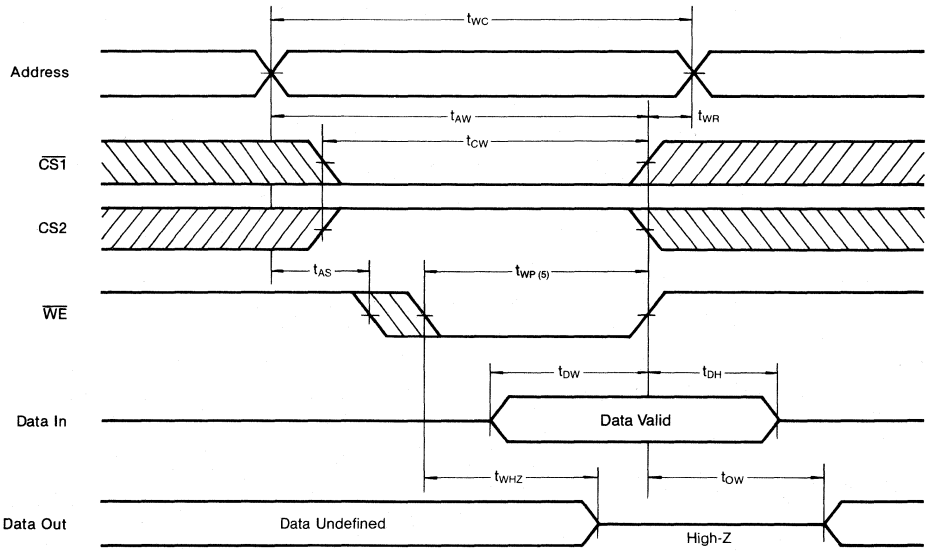
TIMING WAVEFORM OF READ CYCLE (2) ($\overline{WE}$ = V_{IH})



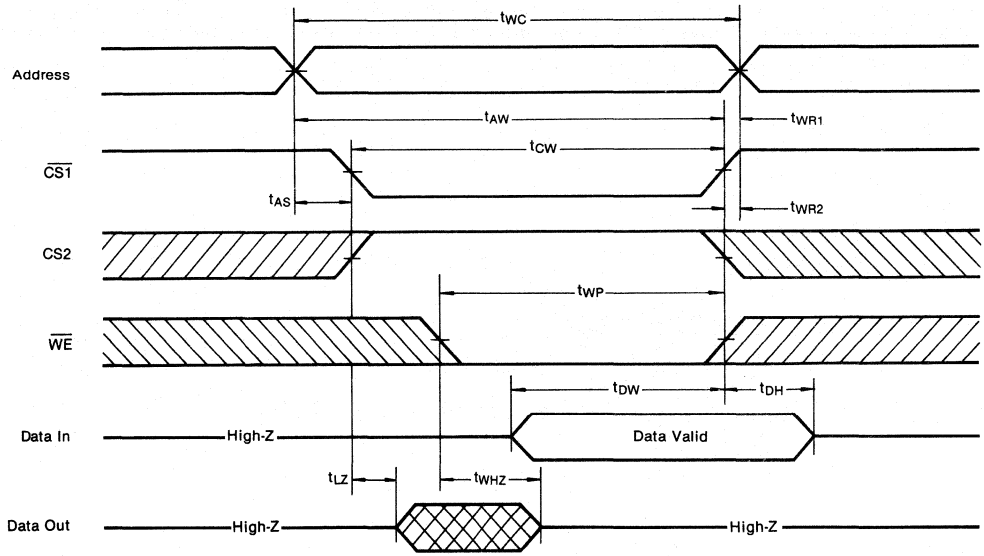
Notes (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
2. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.

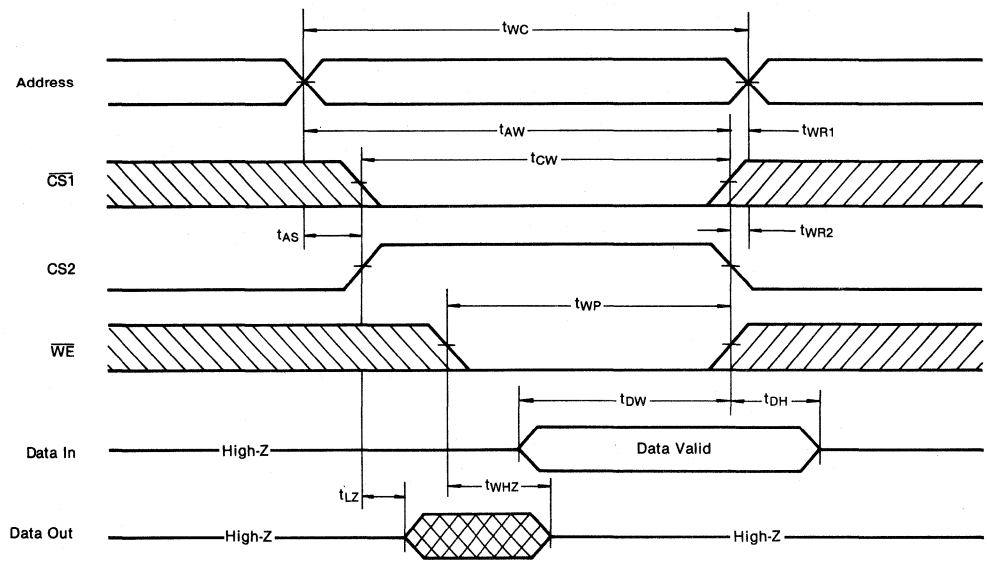
TIMING WAVEFORM OF WRITE CYCLE (1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (3) ($\overline{CS2}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends at $\overline{CS1}$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS2 going low
5. If $\overline{OE}$, CS2 and $\overline{WE}$ are in the read mode during this period, the I/O pins are in the output low-Z state, inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the read data of next address.
8. When $\overline{CS1}$ is low and CS2 is high: I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Vcc Current
H	X*	X	X	Power down	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Power down	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

* X means Don't Care

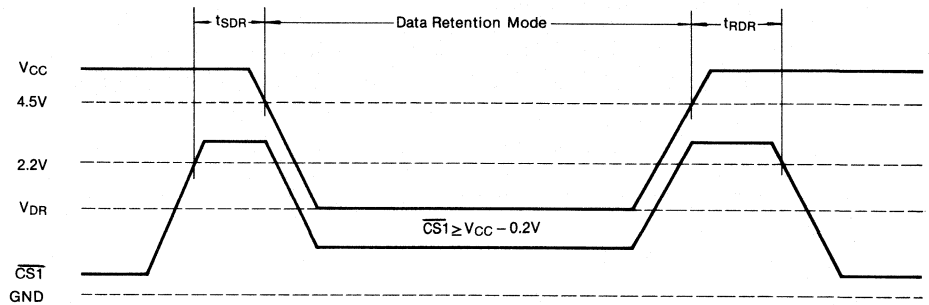
DATA RETENTION CHARACTERISTICS (T_A=-40 to 70°C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1}$(1) ≥ V_{CC}-0.2V		2.0		5.5	V
Data Retention Current	I_{DR}	V_{CC}=3.0V	L-VER		1	50	μA
		$\overline{CS1}$* ≥ V_{CC}-0.2V	LL-VER		0.5	20	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention		0			ns
Recovery Time	t_{RDR}	Waveforms(below)		t_{RC}**			ns

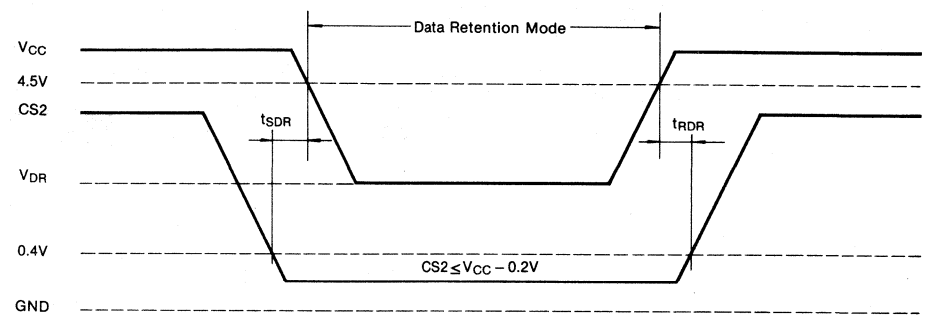
* $\overline{CS1}$ ≥ V_{CC}-0.2, CS2 ≥ V_{CC}-0.2(CS1 Controlled) or CS2 ≤ 0.2(CS2 Controlled)
** Read Cycle Time

2

DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM (2) (CS2 Controlled)



524, 288 WORD X 8 Bit High Speed CMOS Static RAM

FEATURES

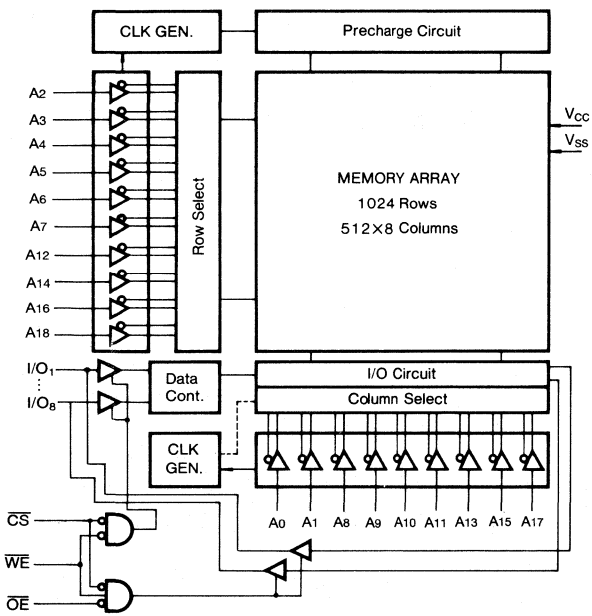
- **Fast Access Time : 55, 70, 85, 100ns(Max.)**
- **Low Power Dissipation**
  Standby (CMOS) : 2.57mW(Max)
  550μW(Max.) L-Version
  110μW(Max.) L-L-Version
  Operating : 385mW/MHz(Max.)
- **Single 5V±10% power supply**
- **TTL Compatible inputs and outputs**
- **Three State Output**
- **Battery back-up operation**
- **Data retention : 2V(Min.) : L/L-L Version**
  2.4V(Min.) : Standard Version

KM684000LP/LP-L : 32-DIP-600
KM684000G/LG/LG-L : 32-SOP-525
KM684000T/LT/LT-L : 32-TSOP2-400F
KM684000R/LR/LR-L : 32-TSOP2-400R

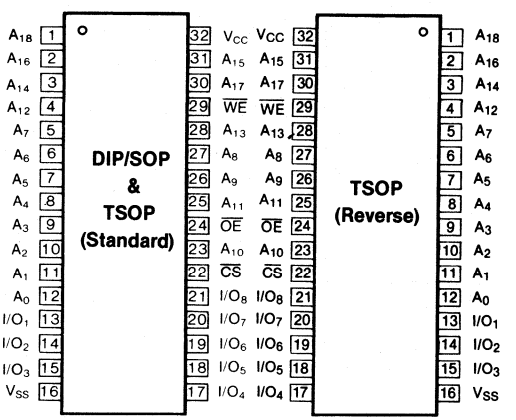
GENERAL DESCRIPTION

The KM684000/L/L-L is a 4,194,304-bit high speed Static Random Access Memory organized as 524, 288 words by 8 bits.
The device is fabricated using Samsung's advanced CMOS process.
The KM684000/L/L-L has an output enable input for precise control of the data outputs.
It also has chip enable inputs for the minimum current power down mode
The KM684000/L/L-L has been designed for high speed and low power applications.
It is particularly well suited for battery back-up nonvolatile memory application.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A18	Address Inputs
$\overline{WE}$	Write Enable input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable input
I/O1~I/O8	Data Inputs/Outputs
VCC	Power(+5V)
VSS	Ground

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	$V_{IN, OUT}$	-0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-55 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

* V_{IL}(min.)=-3.0V for $\leq$50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V$\pm$10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-1	+1	μA
Output Leakage Current	I_{IO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL} $\overline{OE}$=V_{IH}, $V_{I/O}$=V_{SS} to V_{CC}		-1	+1	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}, $I_{I/O}$=0mA			25	mA
Average Operating Current	I_{CC1}	Cycle Time=1μs, 100% Duty $\overline{CS}\leq$0.2V, $V_{IH}\geq V_{CC}$-0.2V $V_{IL}\leq$ 0.2V, $I_{I/O}$=0mA			20	mA
	I_{CC2}	Min Cycle, 100% Duty, CS=V_{IL} V_{IN}=V_{IL} or V_{IH} I_{IO}=0mA			70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}			3	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}$-0.2V			500	μA
		$V_{IN}\geq V_{CC}$-0.2 or $V_{IN}\leq$0.2V	L		100	μA
			L-L		20	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA			0.4	V
Output High Voltage	V_{OH}	I_{OH}=1mA		2.4		

* Typ. : V_{CC}=5V, T_A=25°C

CAPACITANCE (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	10	pF

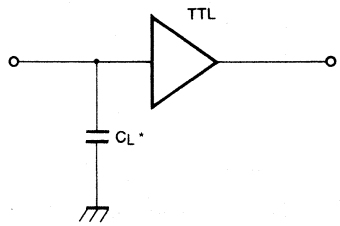
* Note : Capacitance is sampled and not 100% tested.

TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	C_L=100pF+1TTL

*C_L=30pF for KM68512L-5/5L

TEST CIRCUIT



* Including Scope and Jig Capacitances

READ CYCLE

Parameter	Symbol	KM684000-5 KM684000L-5 KM684000L-5L		KM684000-7 KM684000L-7 KM684000L-7L		aKM684000-8 KM684000L-8 KM684000L-8L		KM684000-10 KM684000L-10 KM684000L-10L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	55	-	70	-	85	-	100	-	ns
Address Access Time	t_{AA}	-	55	-	70	-	85	-	100	ns
Chip Select to Output	t_{CO}	-	55	-	70	-	85	-	100	ns
Output enable to valid Output	t_{OE}	-	25	-	35	-	40	-	50	ns
Chip enable to Low-Z Output	t_{LZ}	10	-	10	-	10	-	10	-	ns
Output enable to Low-Z Output	t_{OLZ}	5	-	5	-	5	-	5	-	ns
Output Disable to High-Z Output	t_{HZ}	0	20	0	25	0	30	0	30	ns
Chip Disable to High-Z Output	t_{OHZ}	0	20	0	25	0	30	0	30	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	10	-	ns

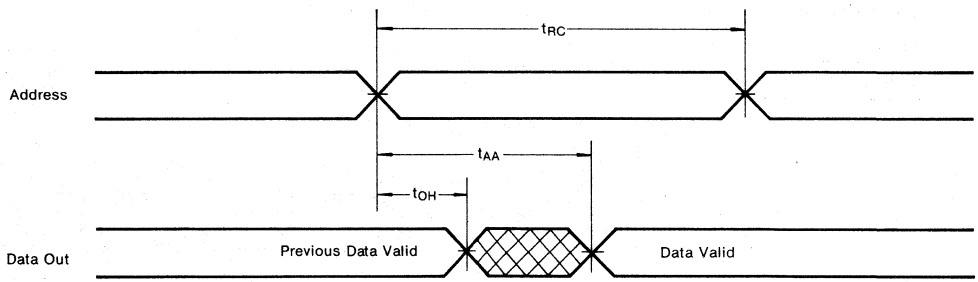
WRITE CYCLE

Parameter	Symbol	KM684000-5 KM684000L-5 KM684000L-5L		KM684000-7 KM684000L-7 KM684000L-7L		KM684000-8 KM684000L-8 KM684000L-8L		KM684000-10 KM684000L-10 KM684000L-10L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	55		70		85		100		ns
Chip Select to End of Write	t_{CW}	45		60		70		80		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AW}	45		60		70		80		ns
Write Pulse Width	t_{WP}	40		50		55		60		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WHZ}	0	25	0	30	0	30	0	30	ns
Data to Write Time Overlap	t_{DW}	25		30		35		40		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End of Write to Output Low-Z	t_{OW}	5		5		5		5		ns

TIMING DIAGRAMS

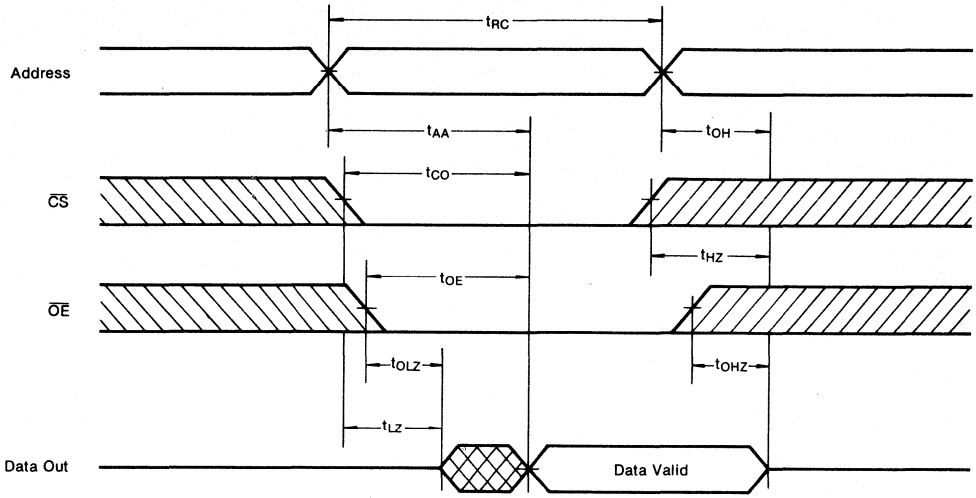
TIMING WAVEFORM OF READ CYCLE(1)(Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



SAMSUNG ELECTRONICS

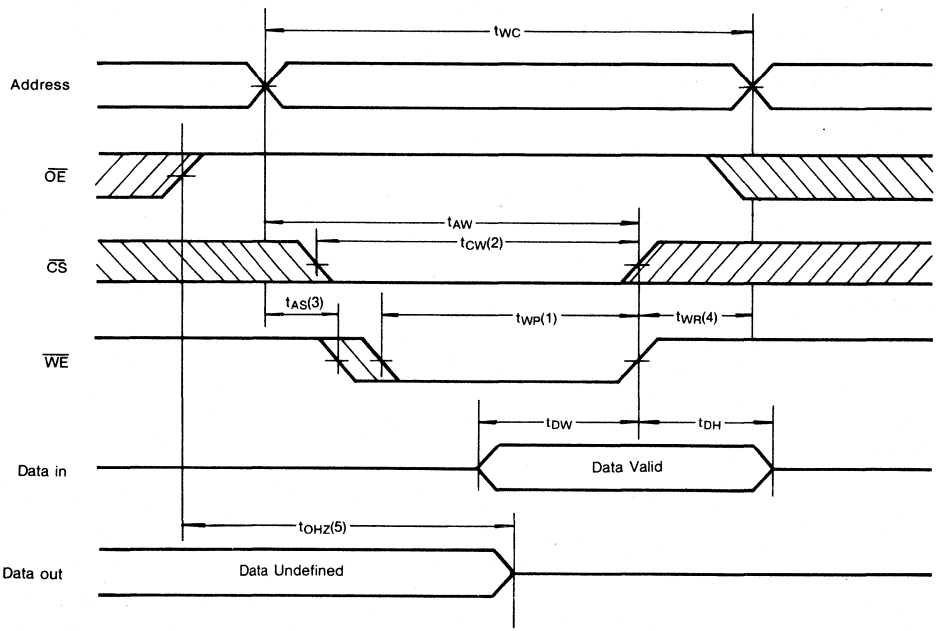
TIMING WAVEFORM OF READ CYCLE (2) ($\overline{WE}$ = V_{IH})



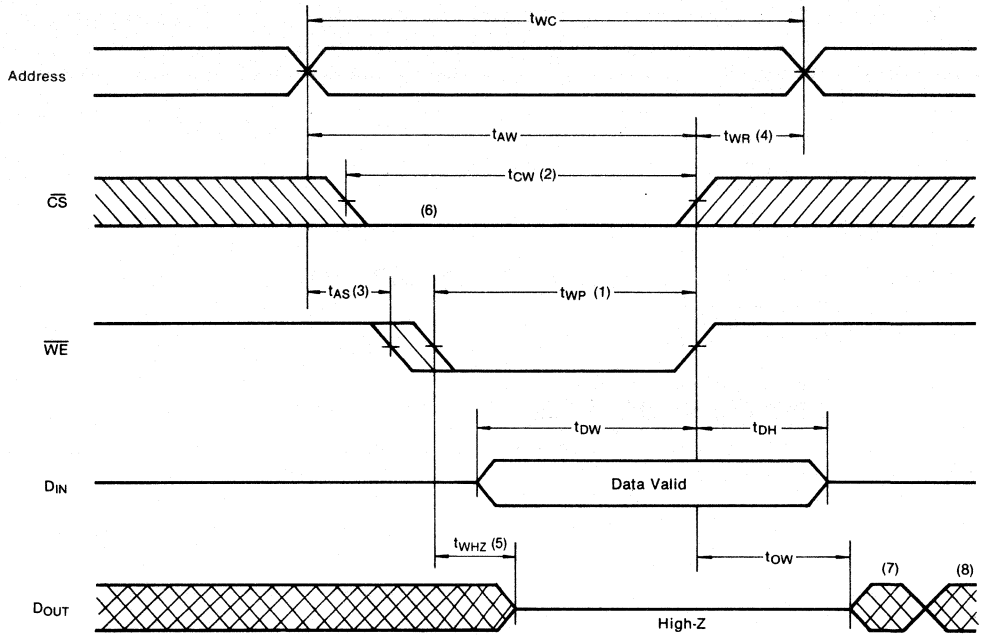
Notes (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
2. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (1) ($\overline{OE}$ = Clock)



TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{OE}$ = Low Fixed)



Notes (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earlist transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
5. During this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
7. D_{OUT} is the some phase of latest written data in this write cycle.
8. D_{OUT} is the read data of the new address.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

DATA RETENTION CHARACTERISTICS* (T_A=40 to 85°C)

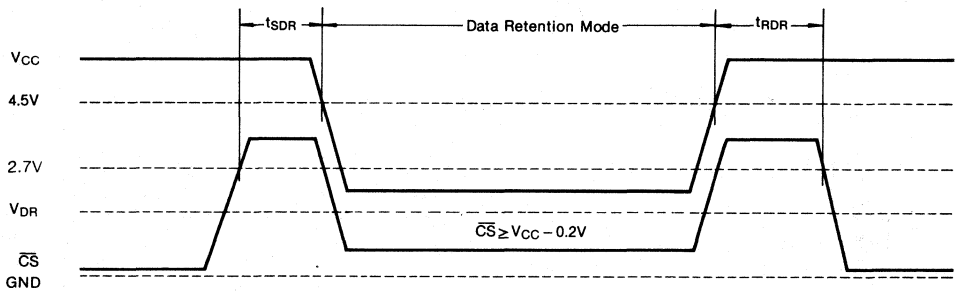
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	CS≥V_{CC}-0.2V	Standard	2.4		5.5	V
			L/L-L	2.0		5.5	V
Data Retention Current	I_{DR}	V_{CC}=3V CS≥V_{CC}-0.2V	Standard			250	μA
			L			50*	μA
			L-L			20**	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms(below)		0			ns
Recovery Time	t_{RDR}			5			ns

* 20μA(max.) at 0°C~40°C

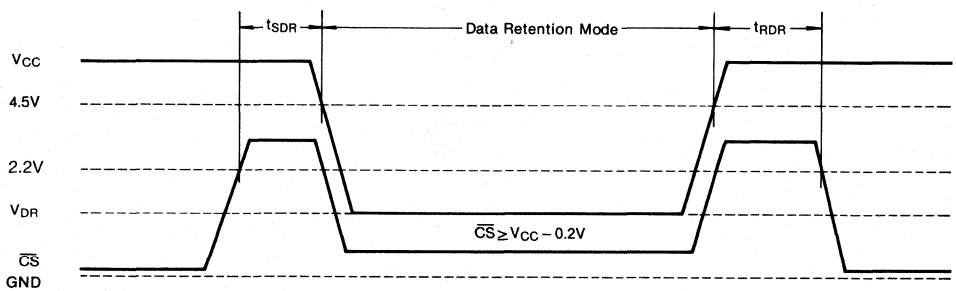
** 5μA(max.) at 0°C~40°C

DATA RETENTION WAVEFORM

Standard Power Version



L/L-L Power Version



524,288K WORD x 8 Bit High Speed CMOS Static RAM

FEATURES

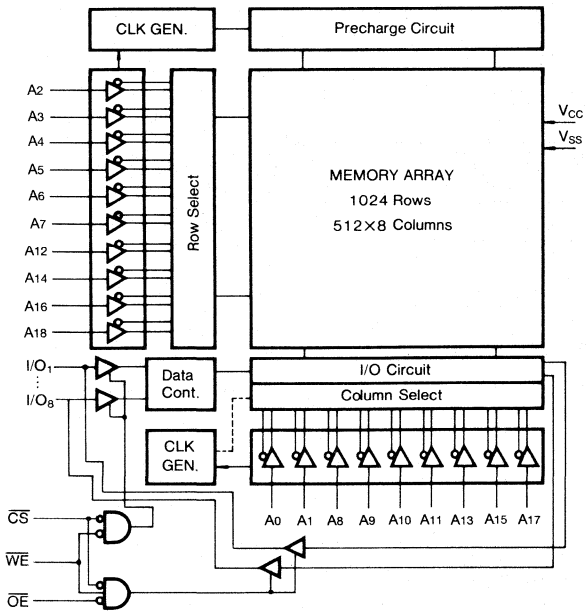
- **Fast Access Time : 70,85,100ns(Max.)**
- **Low Power Dissipation**
  Standby (CMOS) : 11mW(Typ.)
  1.1μW(Typ.) L-Version
  275μW(Typ.) LL-Version
  Operating : 137.5mW(Max.)
- **Single 5V$\pm$10% power supply**
- **Wide temperature operatint: -40°C~85°C**
- **TTL Compatible inputs and outputs**
- **Three State Output**
- **Low Data Retention Voltage:2V(Min)**
- **Standard Pin Configuration**
  KM684000LGI/LGI-L : 32-SOP-525
  KM684000LTI/LTI-L : 32-TSOP2-400F
  KM684000LRI/LRI-L : 32-TSOP2-400R

GENERAL DESCRIPTION

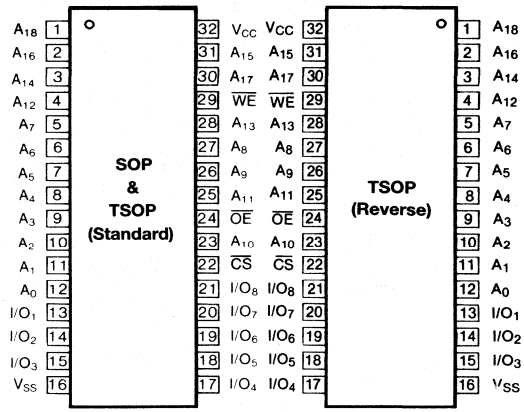
The KM684000LI/LI-L is a 4,194,304-bit high-speed Static Random Access Memory organized as 524, 288 words by 8 bits.
The device is fabricated using Samsung's advanced CMOS process.
The KM684000LI/LI-L has an output enable input for precise control of the data outputs.
It also has chip enable inputs for the minimum current power down mode
The KM684000LI/LI-L has been designed for high speed and low power applications.
It is particularly well suited for battery back-up nonvolatile memory application.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A18	Address Inputs
$\overline{WE}$	Write Enable input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power(+5V)
Vss	Ground

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-55 to 150	°C
Operating Temperature	T_A	-40 to 85	°C

* Stresses greater than those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=40 to 85°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.3*	—	0.8	V

* V_{IL}(min.)=-3.0V for $\leq$50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=-40 to 85°C, V_{CC}=5V$\pm$10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-1	+1	μA
Output Leakage Current	I_{IO}	$\overline{CS}$=V_{IN} or $\overline{WE}$=V_{IL} $\overline{OE}$=V_{IH}, $V_{I/O}$=V_{SS} to V_{CC}		-1	+1	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}, $I_{I/O}$=0mA			25	mA
Average Operating Current	I_{CC1}	Cycle Time=1μs, 100% Duty $\overline{CS}\leq$0.2V, $V_{IH}\geq V_{CC}$-0.2V $V_{IL}\leq$ 0.2V, $I_{I/O}$=0mA			20	mA
	I_{CC2}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL} V_{IN}=V_{IL} or V_{IH} I_{IO}=0mA			70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}			3	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}$-0.2V	L		100	μA
		$V_{IN}\geq V_{CC}$-0.2 or $V_{IN}\leq$0.2V	L-L		50	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA			0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1.0mA		2.4		V

CAPACITANCE (f=1MHz, T_A=25°C)

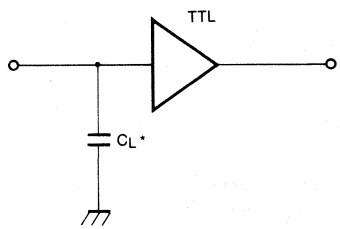
Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	10	pF

* Note : Capacitance is sampled and not 100% tested.

TEST CONDITIONS (T_A=-40 to 85°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	C_L=100pF+1TTL

TEST CIRCUIT



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM684000LI-7 KM684000LI-7L		KM684000LI-8 KM684000LI-8L		KM684000LI-10 KM684000LI-10L		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		ns
Address Access Time	t_{AA}		70		85		100	ns
Chip Select to Output	t_{CO}		70		85		100	ns
Output Enable to Valid Output	t_{OE}		35		40		50	ns
Chip Enable to Low-Z Output	t_{LZ}	10		10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5		ns
Output Disable to High-Z Output	t_{HZ}	0	25	0	30	0	30	ns
Output Disable to High-Z Output	t_{OHZ}	0	25	0	30	0	30	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

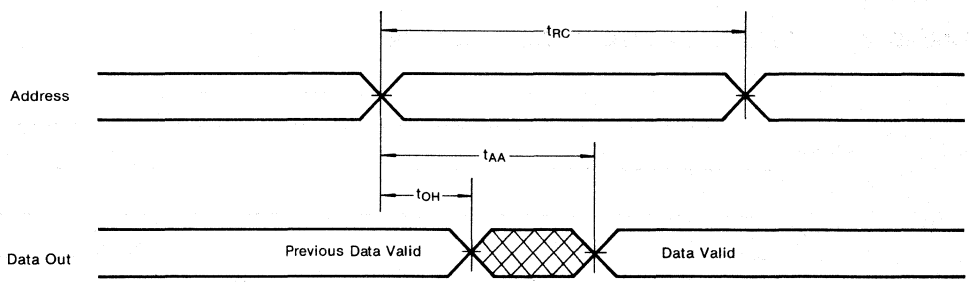
WRITE CYCLE

Parameter	Symbol	KM684000LI-7 KM684000LI-7L		KM684000LI-8 KM684000LI-8L		KM684000LI-10 KM684000LI-10L		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		ns
Chip Select to End of Write	t_{CW}	60		70		80		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	60		70		80		ns
Write Pulse Width	t_{WP}	50		55		60		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WHZ}	0	30	0	30	0	30	ns
Data to Write Time Overlap	t_{DW}	30		35		40		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End of Write to Output Low-Z	t_{OW}	5		5		5		ns

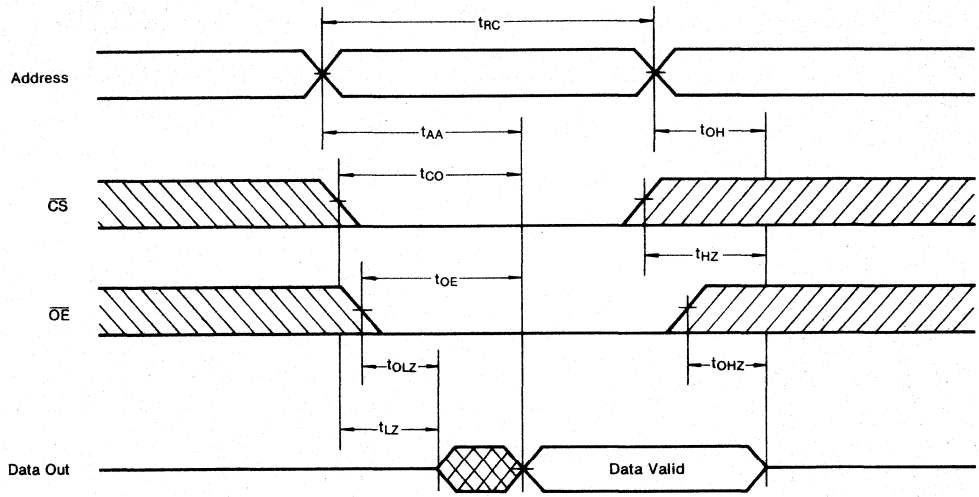
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)



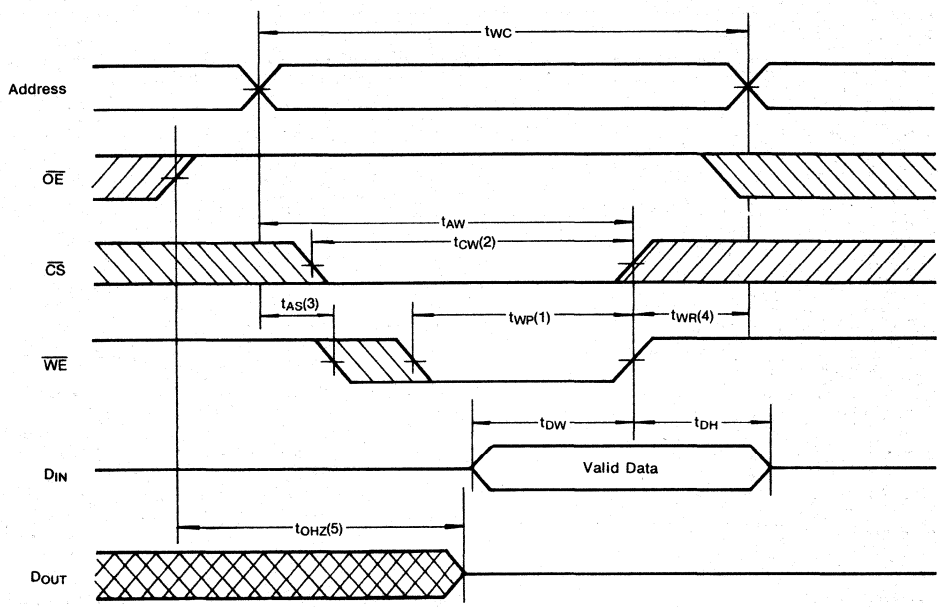
TIMING WAVEFORM OF READ CYCLE (2) ($\overline{WE}$ = V_{IH})



Notes (READ CYCLE)

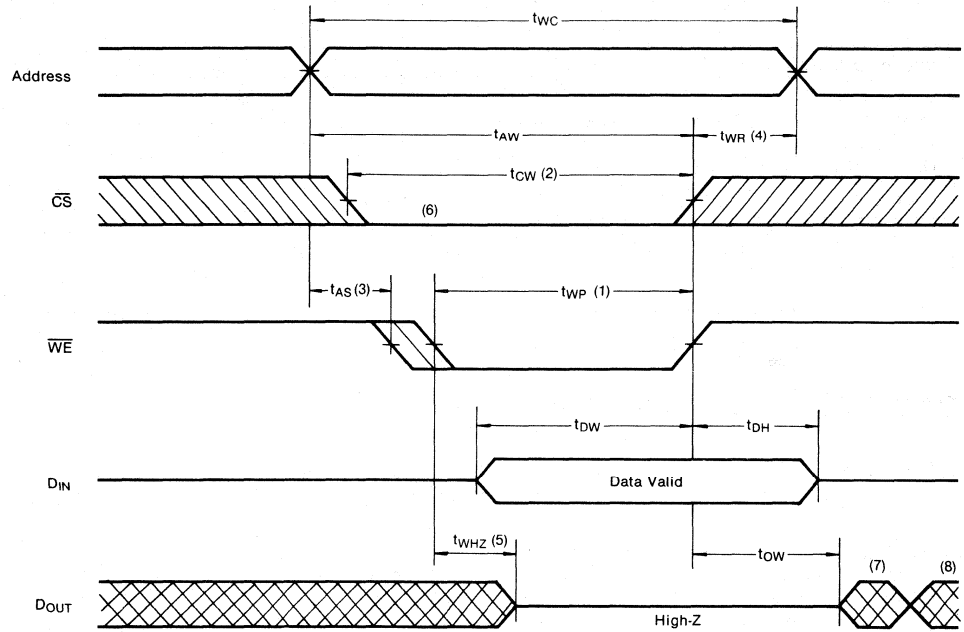
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
2. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (1) ($\overline{OE}$ = Clock)



SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{OE}$ = Low Fixed)



Notes (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earlist transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or WE going high.
5. During this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
7. D_{OUT} is the some phase of latest written data in this write cycle.
8. D_{OUT} is the read data of the new address.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

DATA RETENTION CHARACTERISTICS* (TA=40 to 85°C)

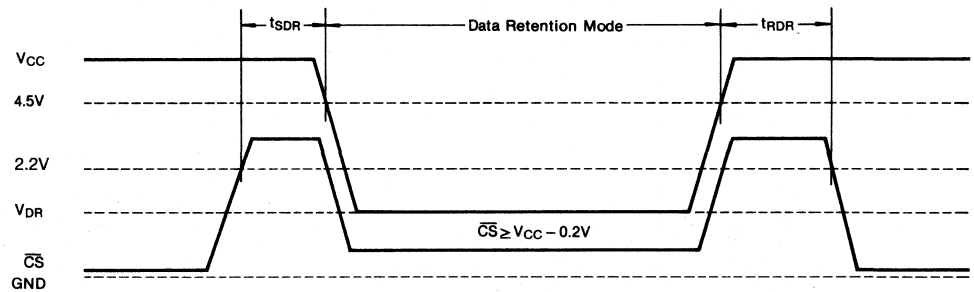
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Vcc for Data Retention	Vdr	$\overline{CS} \geq$ Vcc-0.2V		2.0		5.5	V
Data Retention Current	Idr	Vcc=3V	L			50*	μA
		$\overline{CS} \geq$ Vcc-0.2V	L-L			20**	μA
Data Retention Set-up Time	tSDR	See Data Retention		0			ns
Recovery Time	tRDR	Wave forms (below)		5			ns

* 20μA (max) at 0° C~40C°
** 5μA (max) at 0° C~40C°

2

DATA RETENTION WAVEFORM

L/L-L Power Version



256K x16 Bit CMOS Static RAM

FEATURES

- **Fast Access Time : 55, 70, 85ns(Max.)**
- **Low Power Dissipation**
  Standby (CMOS) : 500μW(Typ.) L-Version
  5μW(Typ.) LL-Version
  Operating : 165mW(max.)
- **Single 5$\pm$10%V power supply**
- **TTL Compatible inputs and outputs**
- **Fully Static Operation**
  - No clock or refresh required
- **Three State Output**
- **Data Byte Control : LB : I/O$_1$~I/O$_8$**
  : UB : I/O$_9$~I/O$_{16}$
- **Low Data Retention Voltage: 2V(Min)**
- **Standard Pin Configuration**
  KM6164000ALT/LT-L : 44-TSOP2-400F

GENERAL DESCRIPTION

The KM6164000AL/L-L is a 4,194,304-bit high speed Static Random Access Memory organized as 262,144 words by 16 bits.

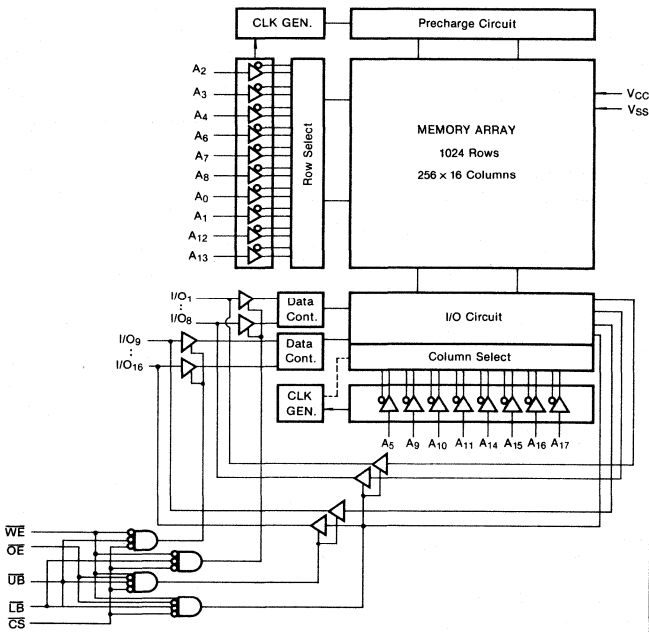
The device is fabricated using Samsung's advanced CMOS process.

The KM6164000AL/L-L has an output enable input for precise control of the data outputs.

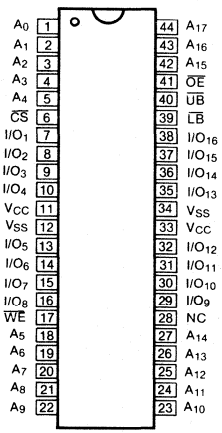
It also has a chip enable input for the minimum current power down mode.

The KM6164000AL/L-L has been designed for high speed and low power applications. It is particularly well suited for low battery back-up nonvolatile memory application.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Low-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1~I/O16	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C.	No Connection

32,768 WORD x 8 Bit Extended Voltage OperationCMOS Static RAM

FEATURES

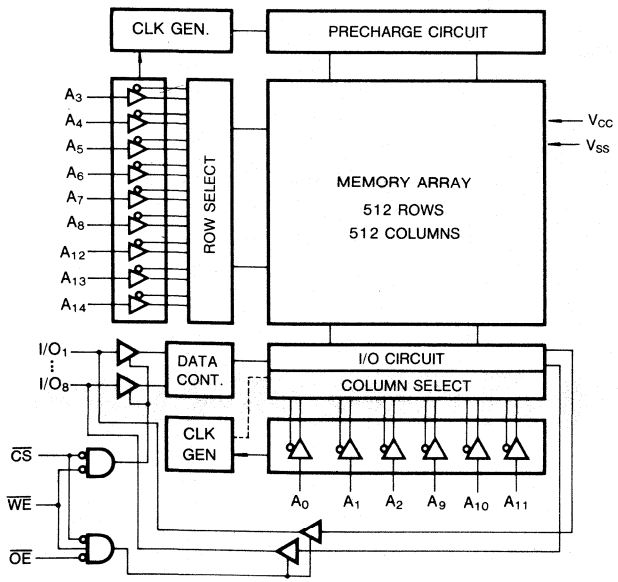
- **Extended Operating Voltage : 3.0~5.5V**
- **Fast Access Time**
  -3.3V Operation : 100ns(Max.)
  -5V Operation : 70ns(Max.)
- **Low Power Dissipation Standby operating**
  -3.3V Operation : 2.4mW/1.2mW(Typ.)
  -5V Operation : 5.0mW/35mW(Typ.)
- **TTL Compatible inputs and outputs**
- **Fully Static Operation**
  -No clock or refresh required
- **Three State Outputs**
- **Standard Pin Configuration**
  KM62256CLG-LV : 28-SOP-450
  KM62256CLTG-LV : 28-TSOP1-0813.4F
  KM62256CLRG-LV : 28-TSOP1-0813.4R

GENERAL DESCRIPTION

The KM62256CL-LV is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.
The device is fabricated using Samsung's advanced CMOS processand high-speed circuit technology.
The KM62256CL-LV has an output enable input for precise control of the data outputs.
It also has a chip enable input for the minimum current power down mode.
The KM62256CL-LV is particularly well suited for use in low voltage(3.0~5.5V) operation and battery back-up applications.

2

FUNCTIONAL BLOCK DIAGRAM

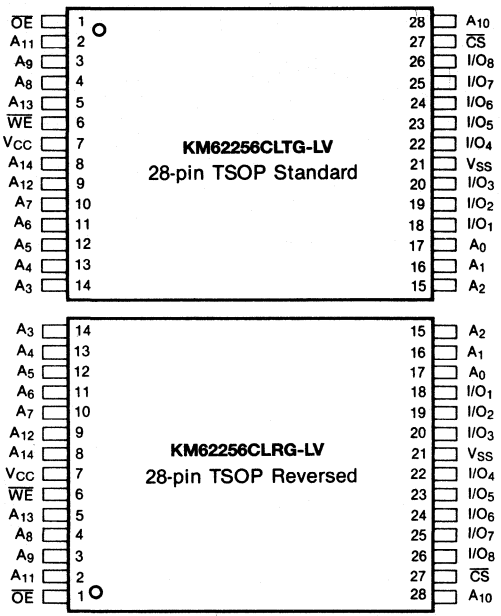


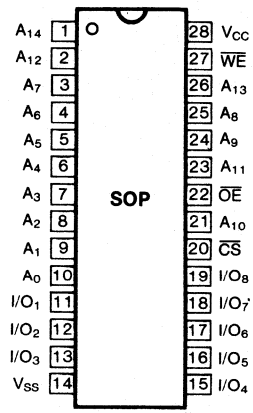
PIN NAMES

Pin Name	Pin Function
A0-A14	Address Inputs
$\overline{WE}$	Write Enable input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable input
I/O1~I/O8	Data Inputs/Outputs
VCC	Power(3.0~5.5V)
VSS	Ground

PIN CONFIGURATIONS (Top View)

28-pin TSOP (0813.4)





ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to V_{CC} + 0.5	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{SOLDER}	260° C, 10sec (Lead only)	-

* Stresses greater than those listed under "ABSOLYT MATINGS RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.3*	-	0.4	V

* V_{IL}(min.)=-3.0V for$\leq$50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, unless otherwise specified)

Item	Symbol	Test Condition	V_{CC}=3.3V$\pm$10%			V_{CC}=5V$\pm$10%			Unit
			Min	Typ*	Max	Min	Typ**	Max	
Input Leakage Current	I_{LI}	V_{IN}=Vssto V_{CC}	-1		1	-1		1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IL}or $\overline{WE}$=V_{IL}, $V_{I/O}$=Vss to V_{CC}	-1		1	-1		1	μA
DC Operating Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL} $I_{I/O}$=0mA		1.0	2.0		7	15	mA
Average Operating Current	I_{CC1}	Cycle Time=1μs, 100% Duty, $\overline{CS}\leq$0.2V, $V_{IL}\leq$0.2V, $V_{IH}\geq V_{CC}$-0.2V, $I_{I/O}$=0mA		2.5	5			7	mA
	I_{CC2}	Min Cycle,100% Duty CS=V_{IL} $I_{I/O}$=0mA			30			70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}			0.3			1	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}$-0.2V, $V_{IN}\geq V_{CC}$-0.2 or $V_{IN}\leq$0.2V			10			20	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA			0.4			0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1.0mA	2.2			2.4			V

* Typ: V_{CC}=3.3V, T_A=25°C

* * Typ: V_{CC}=5.0V, T_A=25°C

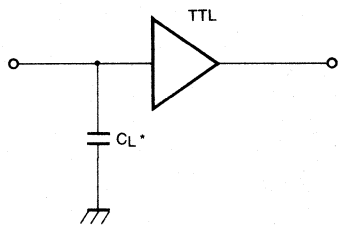
CAPACITANCE (f=MHz, T_A=25°C)

Item	Symbol	Test	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note : Capacitance is sampled and not 100% tested.

TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=3V±10%, unless otherwise specified)

Parameter	Value	
	V_{CC}=3.3V	V_{CC}=5.0V
Input Pulse Level	2.2V/0.4V	2.4V/0.8V
Input Rise and Fall Time	5 ns	5 ns
Input and Output Timing Reference Levels	1.5 V	1.5 V
Output Load	C_L=100pF+1TTL	C_L=100pF+1TTL



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	Vcc=5.0V± 10%		Vcc=3.3V± 10%		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		100		ns
Address Access Time	t_{AA}		70		100	ns
Chip Select to Output	t_{CO}		70		100	ns
Output Enable to Valid Output	t_{OE}		35		50	ns
Chip Select to Low-Z Output	t_{LZ}	10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Chip Disable to High-Z Output	t_{HZ}		30		35	ns
Output Disable to High-Z Output	t_{OHZ}		30		35	ns
Output Hold from Address Change	t_{OH}	5		15		ns

WRITE CYCLE

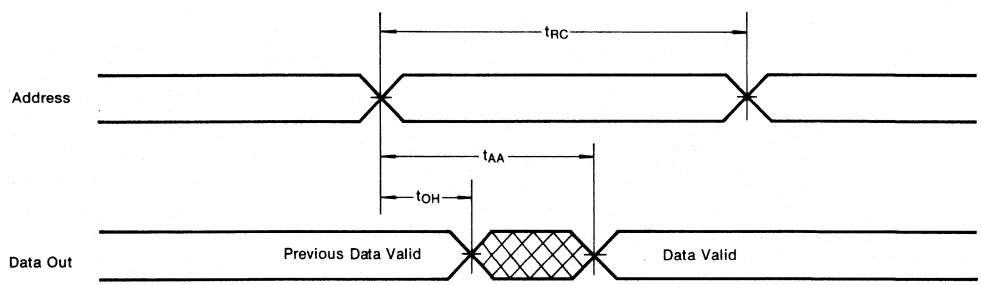
Parameter	Symbol	Vcc=5.0V± 10%		Vcc=3.3V± 10%		UNIT
		Min	Max	Min	Max	
Write Cycle Time	tWC	70		100		ns
Chip Select to End of Write	tCW	60		70		ns
Address Valid to End of Write	tAS	60		70		ns
Address Set-up Time	tAW	0		0		ns
Write Pulse Width	tWP	50		70		ns
Write Recovery Time	tWR	0		0		ns
Write to Output High-Z	tWHZ		25	0	30	ns
Data to Write Time Overlap	tDW	30		50		ns
Data Hold from Write Time	tDH	0		0		ns
End of Write to Output Low-Z	tOW	5		10		ns

2

TIMING DIAGRAMS

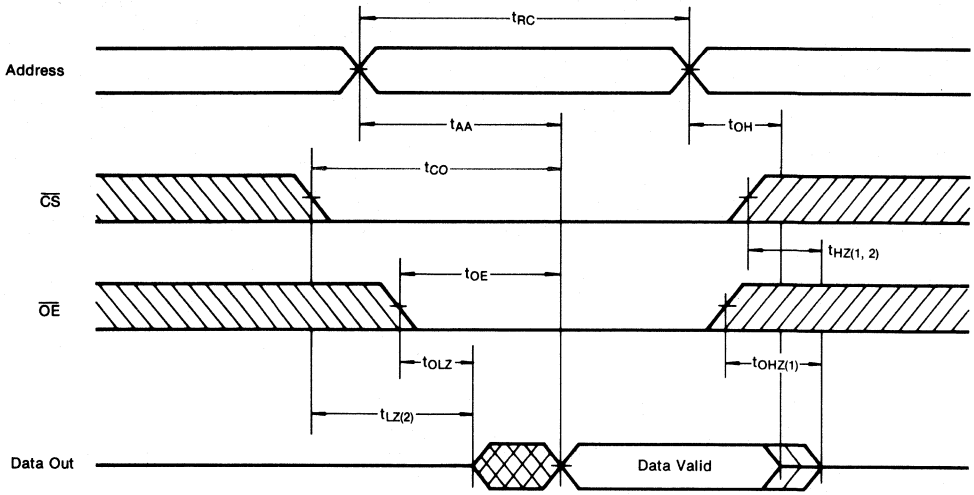
TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



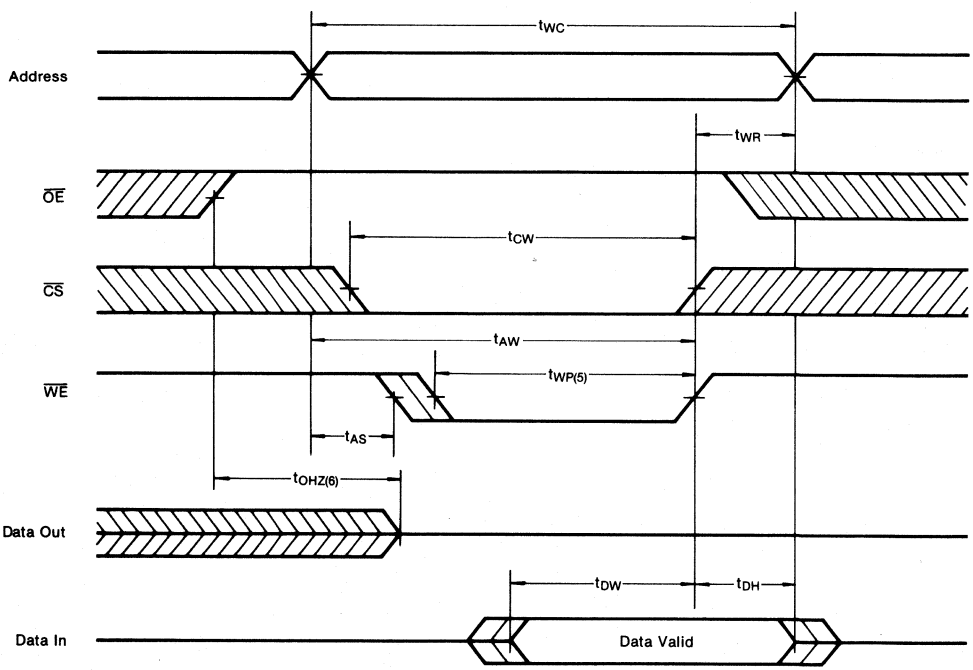
TIMING WAVEFORM OF READ CYCLE (2)

($\overline{WE}$ = V_{IH}) (Note 1, 2, 3, 4)



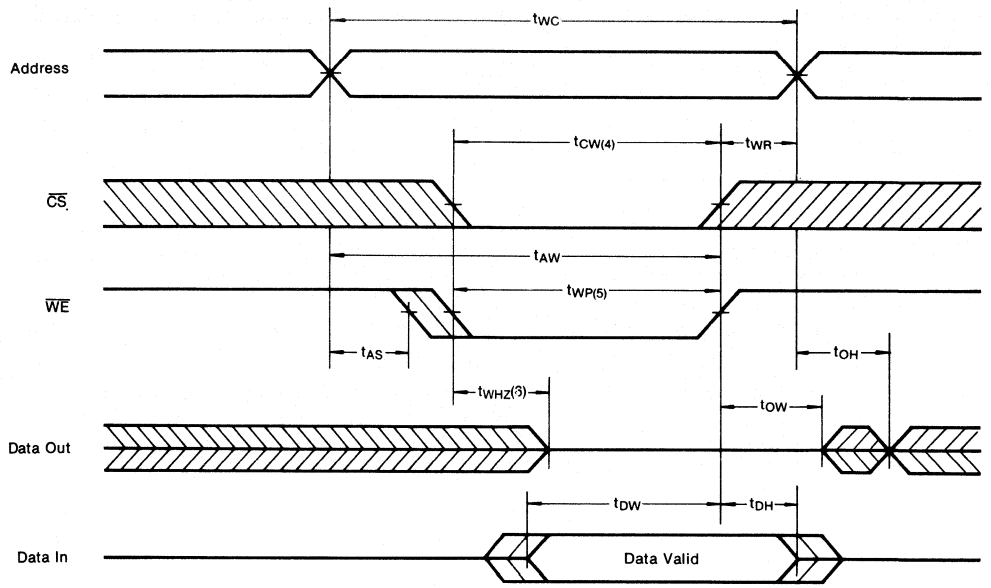
TIMING WAVEFORM OF WRITE CYCLE (3)

($\overline{OE}$ Clocked) (Note 5, 6, 7, 8)



TIMING WAVEFORM OF WRITE CYCLE (4)

($\overline{OE}$ Low Fixed) (Note 5, 6, 7, 8, 9)



Notes

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to the V_{OH} or V_{OL} level.
2. At any given temperature and voltage condition t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ transition Low.
5. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and $\overline{WE}$.
6. During this period, I/O pins are in the output state. The input signals out of phase must not applied.
7. $\overline{CS}$ or $\overline{WE}$ must be high during address transition state.
8. If $\overline{OE}$ is high, I/O pins remain in a high-impedance state.
9. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

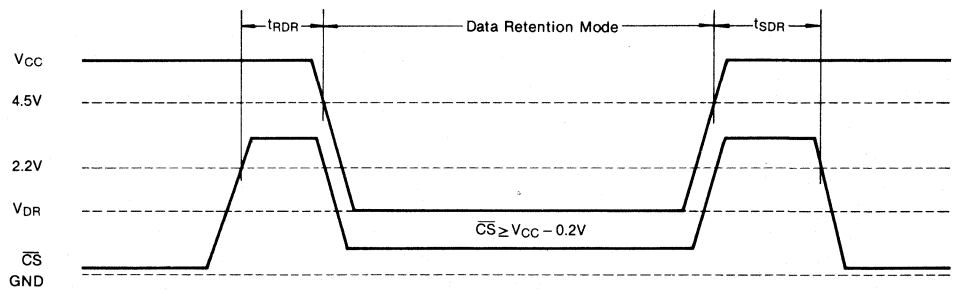
* X means Don't Care.

DATA RETENTION CHARACTERISTICS (T_A=0 to 70°C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V		2.0		5.5	V
Data Retention Current	I_{DR}	V_{CC}=3.3V	0~70° C			10	μA
		$\overline{CS} \geq V_{CC}$-0.2V	0~40° C			5	μA
			25° C		0	3	μA
		V_{CC}=3.0~5.5V			3.0*	10	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention		0			ns
Recovery Time	t_{RDR}	Waveforms(below)		t_{RC}**			ns

* V_{CC}=5.0V, TA=25°C
** t_{RC} : Read Cycle Time

DATA RETENTION WAVEFORM ($\overline{CS}$ Controlled)



131,072 WORD x 8 Bit CMOS Static RAM Low Voltage Operation

FEATURES

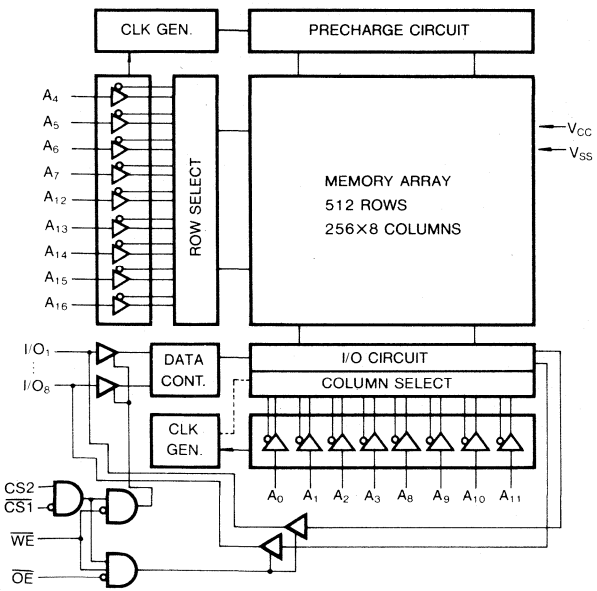
- **Fast Access Time : 70, 100ns(Max.)**
- **Low Power Dissipation**
  Standby (CMOS) : 3μW(Typ.) L-Version
  1.5μW(Typ.) LL-Version
  Operating : 15mW(Typ.)
- **Single 3.0V~3.6V power supply**
- **TTL Compatible inputs and outputs**
- **Fully Static Operation**
  -No clock or refresh required
- **Three State Output**
- **Battery Back-up Operation**
  -2V(min.) Data Retention
- **Standard Pin Configuration**
  KM68V1000BLG/BLG-L:32-SOP-525
  KM68V1000BLT/BLT-L :32-TSOP StandardType
  KM68V1000BLR/BLR-L:32-TSOP StandardType

GENERAL DESCRIPTION

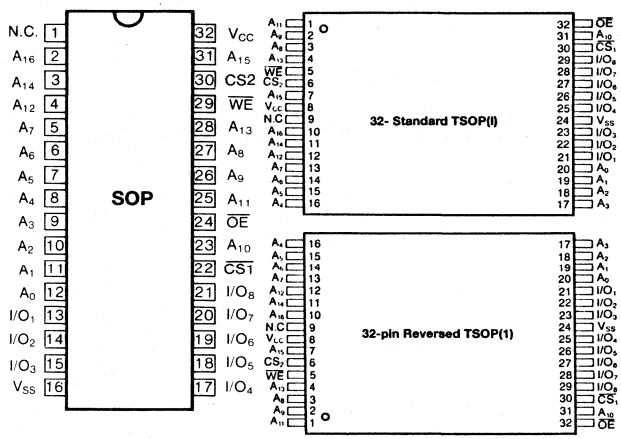
The KM68V1000BL/BL-L is a 1,048,576-bit high speed Static Random Access Memory organized as 131,072 words by 8 bits.
The device is fabricated using Samsung's advanced CMOS process.
The KM68V1000BL/BL-L has an output enable input for precise control of the data outputs.
It also has a chip enable inputs for the minimum current power down mode.
The KM68V1000BL/BL-L has been designed for high speed and low power applications.
It is particularly well suited for low voltage (3.0~3.6V) operation and battery back-up application.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A16	Address Inputs
$\overline{WE}$	Write Enable input
$\overline{CS1}$, CS2	Chip Select Input
$\overline{OE}$	Output Enable input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power(+3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	$V_{in, OUT}$	-0.5 to V_{CC} + 0.5	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 4.6	V
Power Dissipation	P_D	0.7	W
Storage Temperature	T_{STG}	-55 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

* V_{IL}(min.)=-3.0V for $\leq$50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=3.0~3.6V, unless otherwise specified)

Item	Symbol	Test Condition		Min	Typ*	Max	Unit
Input Leakage Current	I_{IL}	V_{IN}=V_{SS} to V_{CC}		-1		+1	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} $\overline{WE}$=V_{IL} $V_{I/O}$ V_{SS} to V_{CC}		-1		+1	μA
DC Operating Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, CS2=V_{IH} V_{IN}=V_{IL} V_{IH}, $I_{I/O}$=0mA				1.5	mA
Average Operating Current	I_{CC1}	Cycle Time=1μs, 100% Duty $\overline{CS1}$ $\leq$0.2V, CS2 $\geq$ V_{CC}-0.2V, $I_{I/O}$=0mA				5	mA
	I_{CC2}	Min. Cycle,100% Duty $I_{I/O}$=0mA $\overline{CS1}$=V_{IL}, CS2=V_{IH}				40	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}				0.3	mA
	I_{SB1}	$\overline{CS1}$ $\geq$ V_{CC}-0.2V	L		1	50	μA
		CS2 $\geq$ V_{CC}-0.2V or CS2 $\leq$ 0.2V	L-L		0.5	10	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA				0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1mA		2.2			V

* Typ. : V_{CC}=3.3V, T_A=25°C

CAPACITANCE (f=1MHz, T_A=25°C)

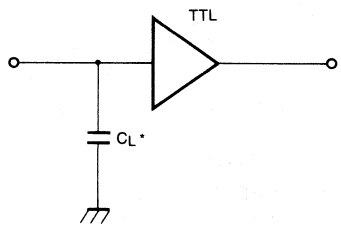
Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note : Capacitance is sampled and not 100% tested.

TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=3.0~3.6V, unless otherwise specified)

Parameter	VALUE
Input Pulse Level	0.8 to 2.2V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	C_L=100*pF+1TTL

TEST CIRCUIT



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68V1000BL-7 KM68V1000BL-7L		KM68V1000BL-10 KM68V1000BL-10L		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		100		ns
Address Access Time	t_{AA}		70		100	ns
Chip Select to Output	t_{CO}		70		100	ns
Output Enable to Valid Output	t_{OE}		35		50	ns
Chip Enable to Low-Z Output	t_{LZ}	10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Chip Disable to High-Z Output	t_{HZ}	0	25	0	30	ns
Output Disable to High-Z Output	t_{OHZ}	0	25	0	30	ns
Output Hold from Address Change	t_{OH}	10		15		ns

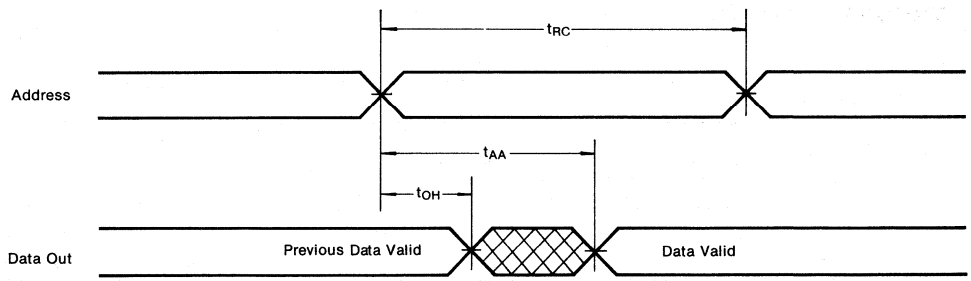
WRITE CYCLE

Parameter	Symbol	KM68V1000BL-7 KM68V1000BL-7L		KM68V1000BL-10 KM68V1000BL-10L		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		100		ns
Chip Select to End of Write	t_{CW}	60		80		ns
Address Set-up Time	t_{AS}	0		0		ns
Address Valid to End of Write	t_{AW}	60		80		ns
Write Pluse Width	t_{WP}	55		70		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to Output High-Z	t_{WHZ}	0	25	0	35	ns
Data to Write Time Overlap	t_{DW}	30		40		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End of Wirte to Output Low-Z	t_{OW}	5		5		ns

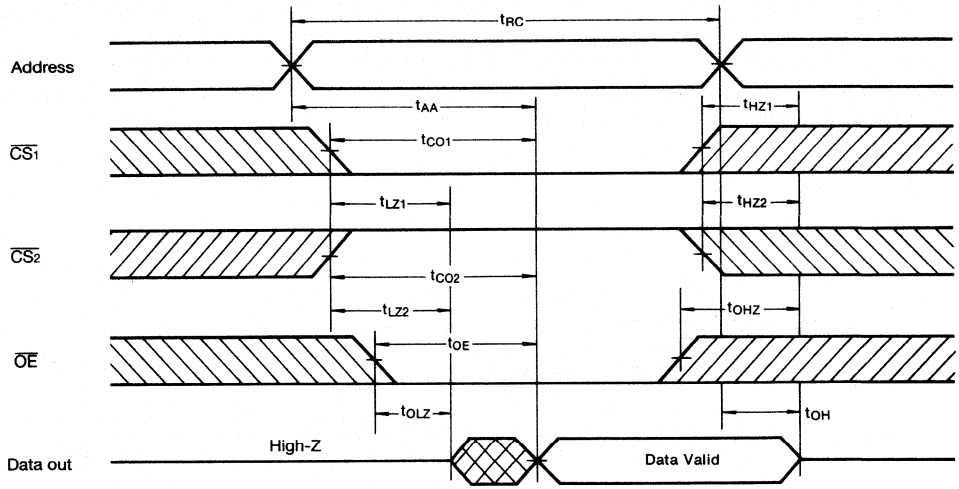
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, CS2=V_{IH}, $\overline{WE}$=V_{IH})



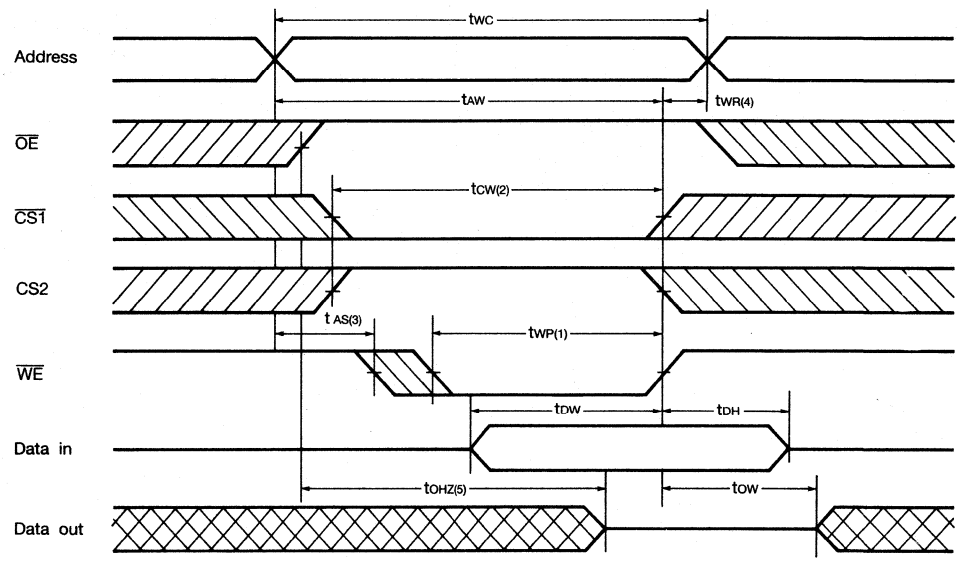
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



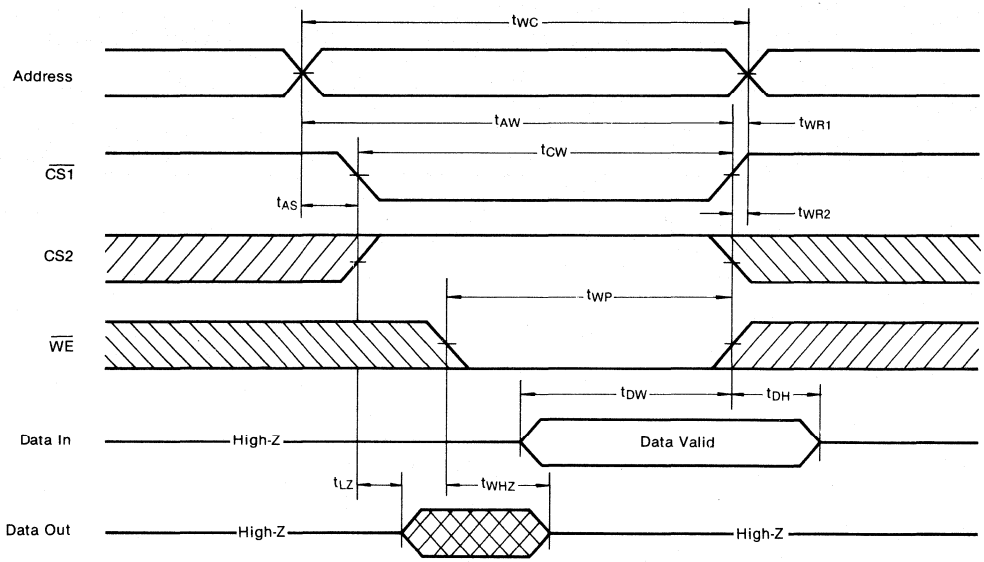
Notes(READ CYCLE)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition tHZ(max.) is less than tLZ(min.).both for a given device and from device to device.

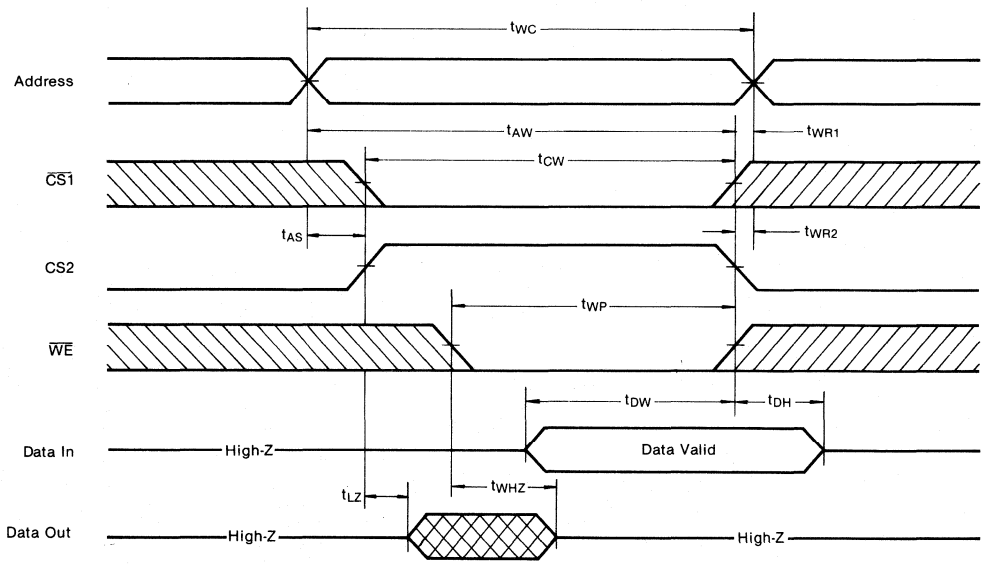
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (3) ($\overline{CS2}$ Controlled)



Notes(WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends at $\overline{CS1}$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS2 going low
5. If $\overline{OE}$, CS2 and $\overline{WE}$ are in the read mode during this period, the I/O pins are in the output low-Z state, inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the read data of next address.
8. When $\overline{CS1}$ is low and CS2 is high: 1/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

2

FUNCTIONAL DESCRIPTION

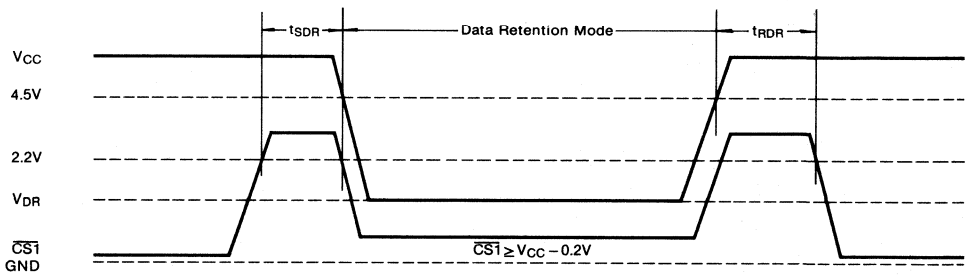
$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Vcc Current
H	X*	X	X	Power down	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Power down	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

DATA RETENTION CHARACTERISTICS (T_A=0 to 70°C)

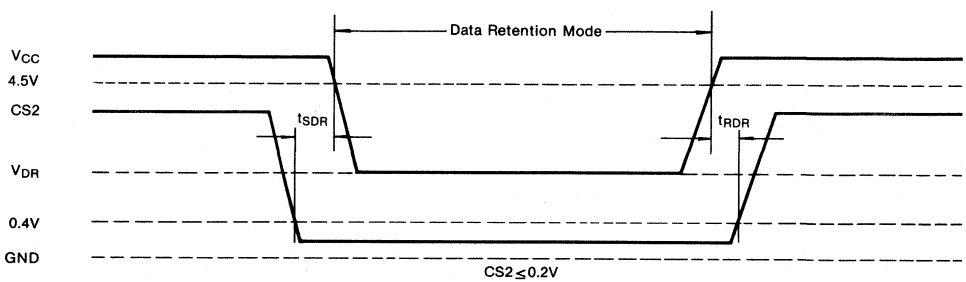
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1}$(1) ≥ V_{CC}-0.2V		2.0		5.5	V
Data Retention Current	I_{DR}	V_{CC}=3.0V	L		1	20(2)	μA
		$\overline{CS1}$ ≥ V_{CC}-0.2V	LL		0.5	5(3)	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention		0			ns
Recovery Time	t_{RDR}	Waveforms(below)		t_{RC}(4)			ns

(1) $\overline{CS1}$ ≥ V_{CC}-0.2, CS2 ≥ V_{CC}-0.2($\overline{CS1}$ Controlled) or CS2 ≤ 0.2(CS2 Controlled)
(2) 20μA(max.) at 0°C to 40°C(Guaranteed only for L-version)
(3) 3μA(max.) at 0°C to 40°C(Guaranteed only for LL-version)
(4) t_{RC}=Read Cycle Time

DATA RETENTION WAVEFORM 1 ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM 2 (CS2 Controlled)



524,288 WORD x 8 Bit CMOS Static RAM Low Voltage Operation

FEATURES

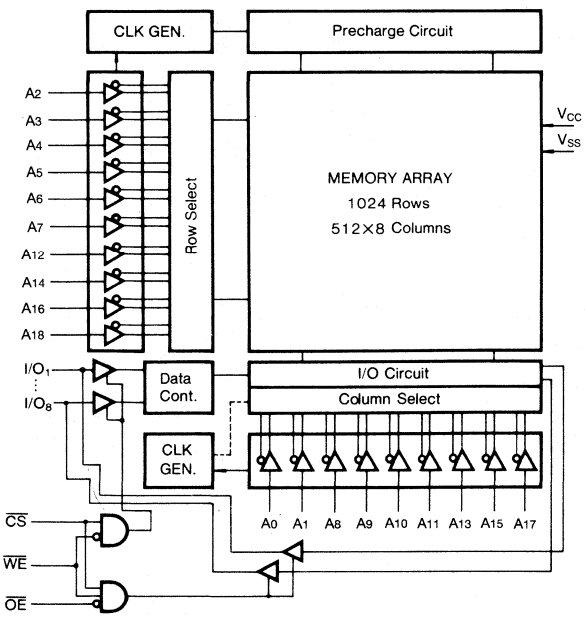
- **Fast Access Time : 70, 100, 120ns(Max.)**
- **Low Power Dissipation**
  Standby (CMOS) : 3μW(Typ.) L-Version
  1.5μW(Typ.) LL-Version
  Operating : 18mW/1MHz
- **Single 3.0~3.6V power supply**
- **TTL compatible inputs and outputs**
- **Three State Output**
- **Low Data Retention Voltage: 2V(Min)**
- **Standard Pin Configuration**
  KM68V4000ALG/ALG-L : 32-SOP-525
  KM68V4000ALT/ALT-L : 32-TSOP2-400F
  KM68V4000ALR/ALR-L : 32-TSOP2-400R

GENERAL DESCRIPTION

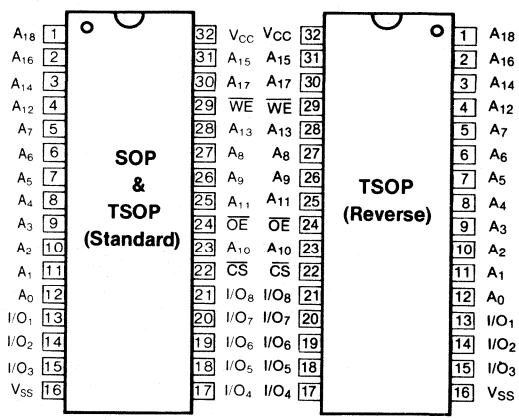
The KM68V4000AL/AL-L is a 14,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits.
The device is fabricated using Samsung's advanced CMOS process.
The KM68V4000AL/AL-L has an output enable input for precise control of the data outputs.
It also has a chip enable input for the minimum current power down mode.
The KM68V4000AL/AL-L has been designed for high speed and low power application.
It is particularly well suited for low voltage (3.0~3.6V) operation and battery back-up application.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A18	Address Inputs
$\overline{WE}$	Write Enable input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power(+3V)
Vss	Ground

256KX16 Bit CMOS Static RAM Low Voltage Operation

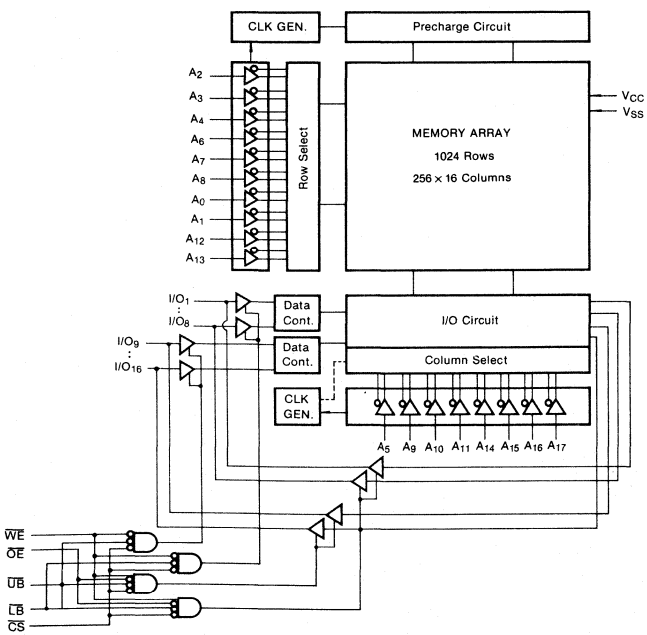
FEATURES

- **Fast Access Time : 70, 100, 120ns(Max.)**
- **Low Power Dissipation**
  Standby (CMOS) : 3μW(Typ.) L-Version
  1.5μW(Typ.) LL-Version
  Operating : 12mW(Typ.)
- **Single 3.0~3.6V power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - No clock or refresh required
- **Three State Output**
- **Data Byte Control : LB:I/O1~I/O8**
  : LB:I/O9~I/O16
- **Low Data Retention Voltage : 2V(Min.)**
- **Standard Pin Configuration**
  KM616V4000ALT/ALT-L : 44-pin TSOP(II)
  (Standard Type)

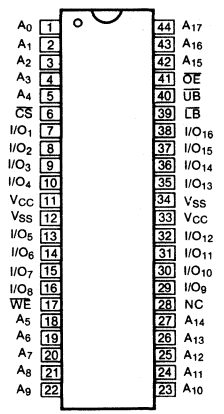
GENERAL DESCRIPTION

The KM616V4000AL/L-L is a 4,194,304 bit-high speed Static Random Access Memory organized as 262,144 words by 16 bits.
The device is fabricated using Samsung's advanced CMOS process.
The KM616V4000AL/L-L has an output enable input for precise control of the data outputs.
It also has a chip enable inputs for the minimum current power down mode.
The KM616V4000AL/L-L has been designed for high speed and low power applications. It is particularly well suited for low voltage (2.7~3.6V) operation and battery back-up application.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Upper-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1~I/O16	Data Inputs/Outputs
VCC	Power(+3.3V)
VSS	Ground
N.C	No Connection

128K X 8 Bit CMOS Pseudo Static RAM

FEATURES

- **Fast Access Time:**
  - **—$\overline{CE}$ Access Time ... 80,100,120ns (Max.)**
  - **—Cycle Time ... Random Read/Write Cycle Time ... 130,160,190ns (Max.)**
- **Low Power Dissipation ... 200mW typ. (Active)**
  0.5mW typ. (Standby)
- **Single 5V±10% Power Supply**
- **TTL compatible inputs and outputs**
- **Non multiplexed Address**
- **Three state Output**
- **512 Refresh Cycles/8ms**
- **Self Refresh Current: 1mA (max. Standard)**
  200μA (max. L-Version)
  100μA (max, LL-Version)
- **Data Retention Supply Voltage; 3.0V to 5.5V**
  - **—Battery Back-up Capability with KM658128LD/LD-L**
- **CS Mode Standby Cycle**
- **32-Pin JEDEC Standard Plastic Package**
  - **—DIP (600mil)**
  - **—SOP (525mil), SOP (450mil)**

GENERAL DESCRIPTION

The KM658128A/AL/AL-L is a 1,048,576 bit high-speed Pseudo Static Random Access Memory organized as 131,072 words by 8 bits, fabricated using 1.1μm advanced CMOS technology.

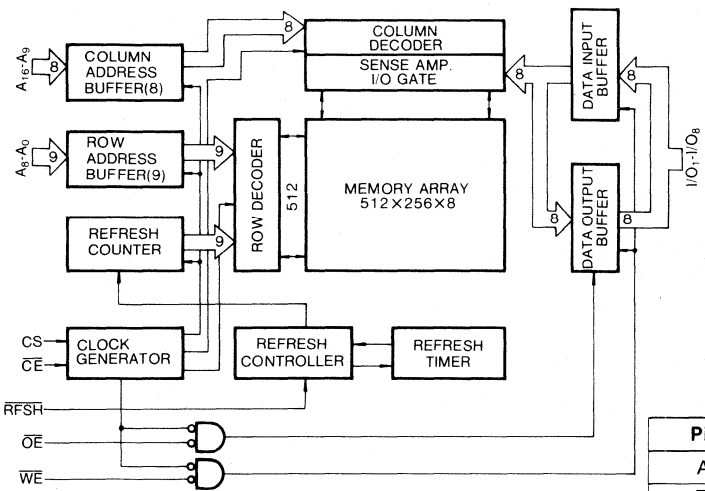
The device, utilizing one transistor DRAM cell with on-chip refresh timer, provides the advantages of DRAM (Low cost, High density) and Static RAM (Low standby power and ease of use).

The pin-out of KM658128A/AL/AL-L follow the JEDEC standard for Static RAM with the addition of $\overline{RFSH}$ input. The $\overline{RFSH}$ input allows two types of refresh operation ; Auto Refresh and Self Refresh.

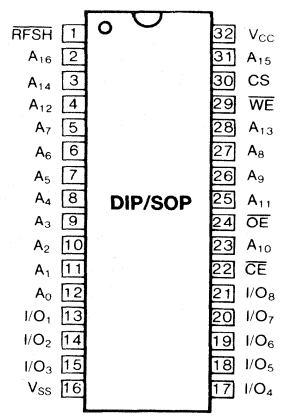
The $\overline{CE}$ only Refresh is also supported.

The KM658128A/AL/AL-L supports a write function similiar to static RAM in that the input data is written into the memory cell at the rising edge of $\overline{WE}$, thus simplifying the interface to standard microprocessors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Pin Name	Pin Function
A0-A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{RFSH}$	Refresh
$\overline{CE}$	Chip Enable
CS	Chip Select
I/O1-I/O8	Data Inputs/Outputs
VCC	Power Supply
VSS	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1.0 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Soldering Temperature Time	T_{solder}	260·10 (Lead only)	°C·sec

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating. Section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Ta=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1.0	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.)=−3.0V for pulse width≤10ns

DC AND OPERATING CHARACTERISTICS

(Ta=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	All Inputs, V_{IN}=0 to V_{CC}		−10	—	+10	μA
Output Leakage Current	I_{LO}	$\overline{OE}$=V_{IH}, $V_{I/O}$=0 to V_{CC}		−10	—	+10	μA
Operating Power Supply Current	I_{CC1}	$\overline{CE}$, CS, Address Cycling I/O=0mA, t_{CYC}=t_{RC}min.	130ns	—	50	70	mA
			160ns	—	40	60	
			190ns	—	35	50	
Standby Power Supply Current	I_{SB1}	$\overline{CE}$=V_{IH}, $\overline{RFSH}$=V_{IH}		—	1	2	mA
	I_{SB2}	$\overline{CE}$≥V_{CC}−0.2V $\overline{RFSH}$≥V_{CC}−0.2V	KM658128A	—	—	1	mA
			KM658128AL	—	100	200	μA
			KM658128AL-L	—	70	100	μA
Self Refresh Current	I_{CC2}	$\overline{CE}$=V_{IH} $\overline{RFSH}$=V_{IL}		—	1	2	mA
	I_{CC3}	$\overline{CE}$≥V_{CC}−0.2V $\overline{RFSH}$≤0.2V	KM658128A	—	—	1	mA
			KM658128AL	—	100	200	μA
			KM658128AL-L	—	70	100	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1.0mA		2.4	—	—	V

CAPACITANCE (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	10	pF

* Note: Capacitance is sampled and not 100% tested.

FUNCTIONAL DESCRIPTION

$\overline{CE}$	CS at $\overline{CE}$ going Low	$\overline{RFSH}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode
L	H	X*	L	H	OUT	READ
L	H	X	X	L	IN	WRITE
L	H	X	H	H	High-Z	$\overline{CE}$ Refresh
L	L	X	X	X	High-Z	CS Standby
H	X	L	X	X	High-Z	Refresh
H	X	H	X	X	High-Z	Standby

* Note: X=Don't care

AC CHARACTERISTICS

TEST CONDITIONS (Ta=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified.)

Input Pulse Level ..... 0.6 to 2.6V
Input Rise and Fall Time 5ns
Input Timing Reference Level ..... V_{IH}=2.4V, V_{IL}=0.8V
Output Timing Reference Level ..... V_{OH}=2.2V, V_{OL}=0.8V
Output Load ..... C_L=100pF+1TTL

Item	Symbol	KM658128A-8		KM658128A-10		KM658128A-12		Unit
		Min	Max	Min	Max	Min	Max	
Random Read or Write Cycle Time	t_{RC}	130	—	160	—	190	—	ns
Random read Modify write Cycle Time	t_{RWC}	190	—	220	—	260	—	ns
Chip Enable Access Time	t_{CEA}	—	80	—	100	—	120	ns
Output Enable Access Time	t_{OEA}	—	30	—	30	—	40	ns
Chip Disable to Output in High-Z	t_{CHZ}	0	30	0	30	0	35	ns
Chip Enable to Output in Low-Z	t_{CLZ}	20		20	—	20	—	ns
Output Disable to Output High-Z	t_{OHZ}	—	25	—	25	—	30	ns
Output Disable Set-Up Time	t_{ODS}	0	—	0	—	0	—	ns
Output Disable Hold Time	t_{ODH}	10	—	10	—	10	—	ns
Output Enable to Output In Low-Z	t_{OLZ}	0	—	0	—	0	—	ns
Chip Enable Pulse Width	t_{CE}	80n	10μ	100n	10μ	120n	10μ	s
Chip Enable Precharge Time	t_P	40	—	50	—	60	—	ns
Address Set-up Time	t_{AS}	0	—	0	—	0	—	ns
Address Hold Time	t_{AH}	30	—	30	—	35	—	ns
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns

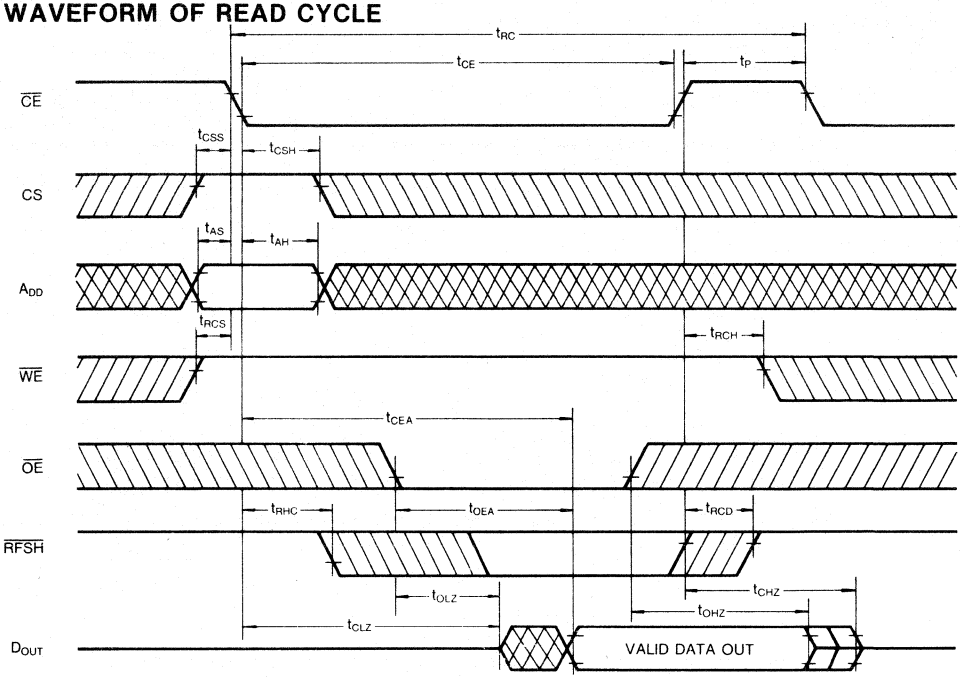
AC CHARACTERISTICS (Continued)

Item	Symbol	KM658128A-8		KM658128A-10		KM658128A-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns
$\overline{RFSH}$ Hold Time	t_{RHC}	15	—	15	—	15	—	ns
Refresh Command Delay Time (Standby Mode)	t_{RCD}	—	5	—	5	—	5	ns
Chip Select Set-up Time	t_{CSS}	0	—	0	—	0	—	ns
Chip Select Hold Time	t_{CSH}	30	—	30	—	35	—	ns
Write Command Pulse Width	t_{WP}	50	—	60	—	65	—	ns
Chip Enable to End of Write	t_{CW}	80	—	100	—	120	—	ns
Data In to End of Write	t_{DW}	25	—	30	—	30	—	ns
Data In Hold Time for Write	t_{DH}	0	—	0	—	0	—	ns
Output Active from End of Write	t_{OW}	5	—	5	—	5	—	ns
Write to Output in High-Z	t_{WHZ}	—	20	—	25	—	30	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	40	—	50	—	60	—	ns
Refresh Precharge Time	t_{FP}	40	—	40	—	40	—	ns
Refresh Reset Time (Automatic Refresh)	t_{RFA}	0	—	0	—	0	—	ns
Refresh Command Pulse Width (Automatic Refresh)	t_{FAP}	80n	8μ	80n	8μ	80n	8μ	s
Automatic Refresh Cycle Time	t_{FC}	130	—	160	—	190	—	ns
Refresh Command Pulse Width (Self Refresh)	t_{FAS}	8	—	8	—	8	—	μs
Refresh Reset Time (Self Refresh)	t_{RFS}	130	—	160	—	190	—	ns
Refresh Periods (512 cycles)	t_{REF}	—	8	—	8	—	8	ms

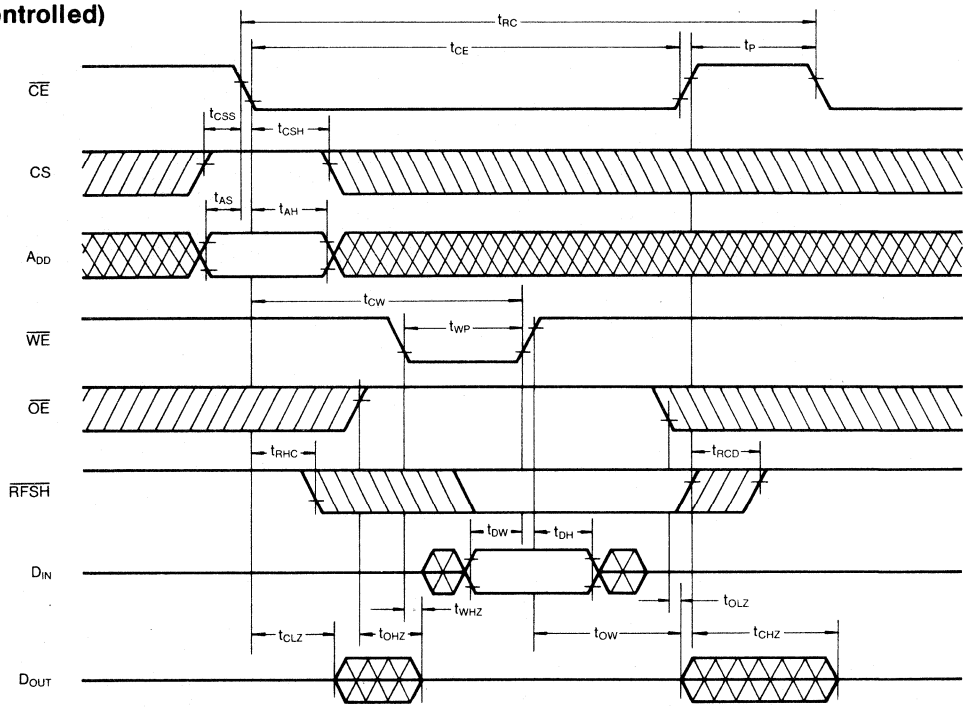
NOTES

1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions under condition of t_T=5ns and are not 100% tested.
2. t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} and t_{OW} are sampled under condition of t_T=5ns and not 100% tested.
3. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. Write ends at the earlier of $\overline{WE}$ going high or $\overline{CE}$ going high.
4. In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
5. Transition time t_T is measured between V_{IH}(min), and V_{IL}(max).
6. After power-up, pause more than 100μs and execute at least 8 initialization cycle.
7. 512 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15μs after self refresh, in order to meet the refresh specification of 8ms and 512 cycles.

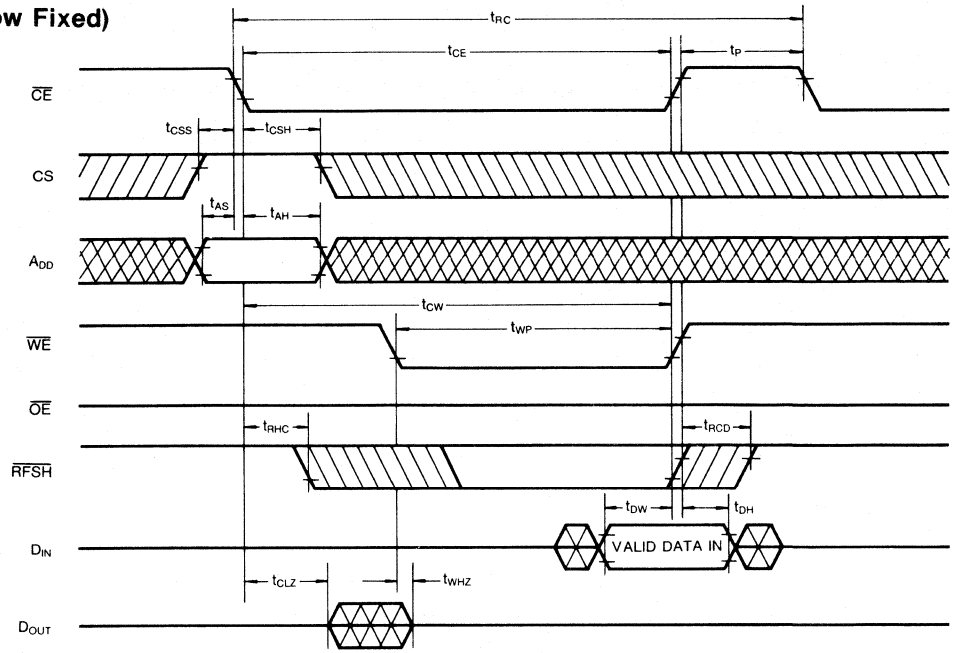
TIMING WAVEFORM OF READ CYCLE



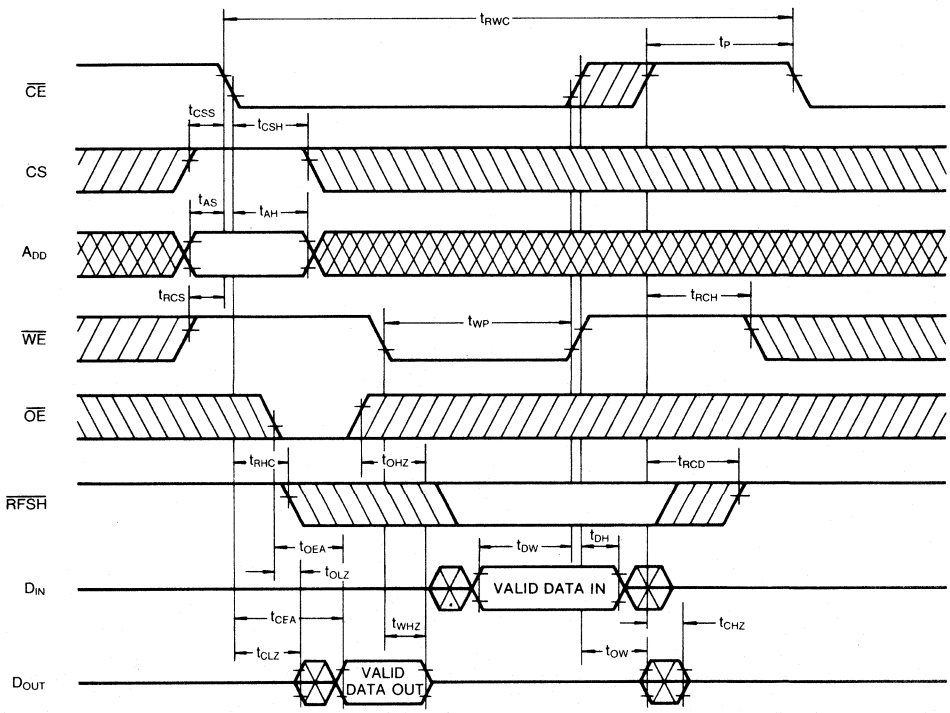
TIMING WAVEFORM OF WRITE CYCLE No. 1 (OE Controlled)



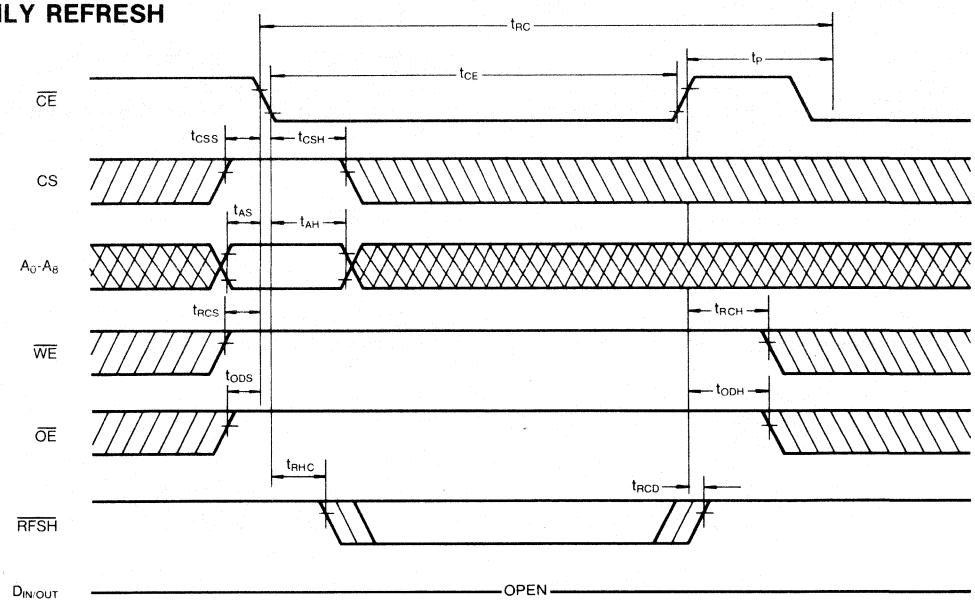
TIMING WAVEFORM OF WRITE CYCLE No. 2 ($\overline{OE}$ Low Fixed)



TIMING WAVEFORM OF READ MODIFY WRITE CYCLE

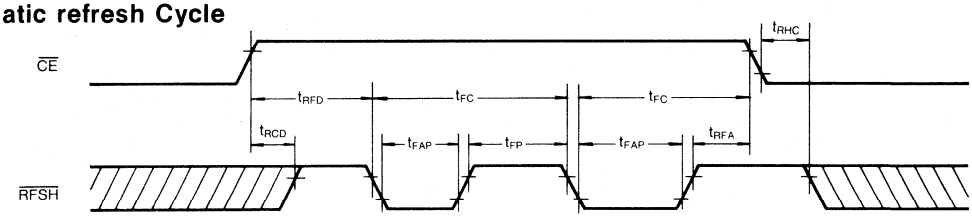


$\overline{CE}$ ONLY REFRESH

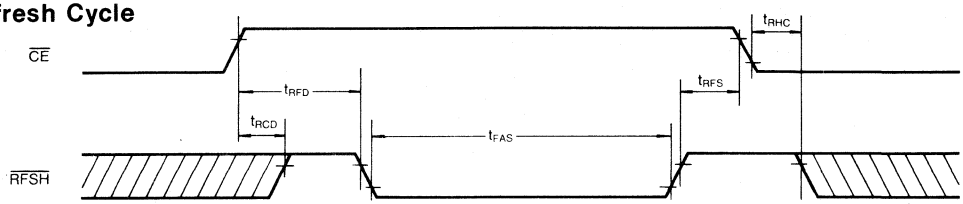


Note: A_{DD9-16} Don't care

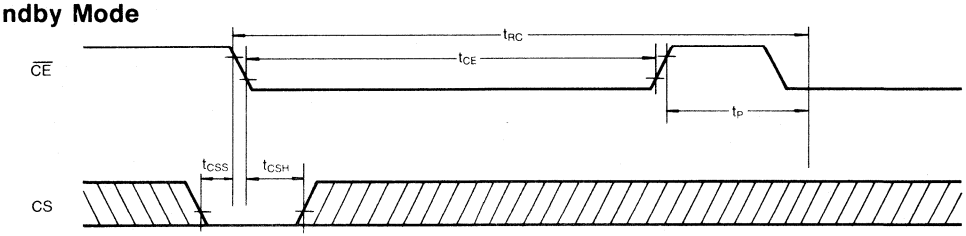
Automatic refresh Cycle



Self refresh Cycle



CS Standby Mode



16,384 WORD×4 Bit CMOS Static RAM

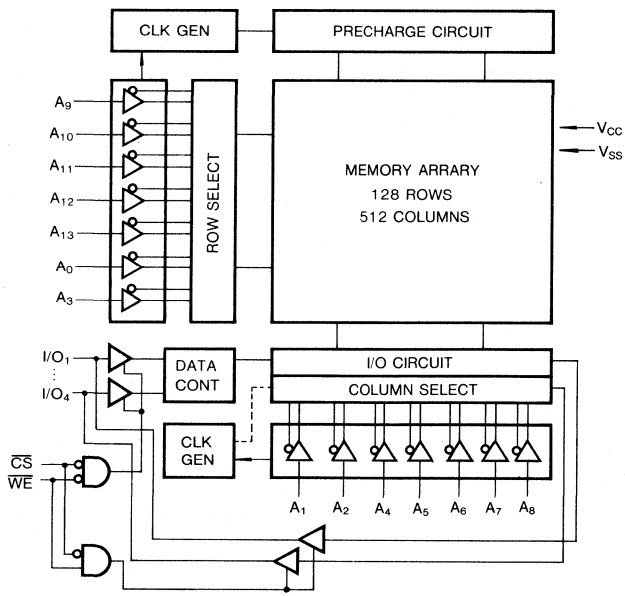
FEATURES

- **Fast Access Time: 12, 15, 20, 25ns (max.)**
- **Low Power Dissipation**
  Standby (TTL) : 35mA (max.)
  (CMOS): 1mA (max.)
- **Operating KM6465B-12 : 140mA (max.)**
  KM6465B-15 : 130mA (max.)
  KM6465B-20 : 120mA (max.)
  KM6465B-25 : 110mA (max.)
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  No clock or refresh required
- **Three State Outputs**
- **Standard Pin Configuration**
  - KM6465BP : 22-DIP-300B

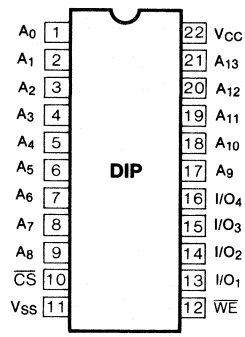
GENERAL DESCRIPTION

The KM6465B is a 65,536-bit high-speed Static Random Access Memory organized as 16,384 words by 4 bits.
The device is fabricated using Samsung's advanced CMOS process.
The KM6465B has a chip select input for the minimum current power down mode.
The KM6465B has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which batery back-up for nonvolatility is required.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Pin Name	Pin Function
A_0-A_{13}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.) = −3.0V for ≤20ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-	-	1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH}, $\overline{WE}$=V_{IL}, $V_{I/O}$=Vss to Vcc, Vcc=Max		-	-	1	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty, $\overline{CS}$=V_{IL}, I_{OUT}=0mA	12ns	-	110	140	mA
			15ns	-	95	130	mA
			20ns	-	85	120	mA
			25ns	-	75	110	mA
Standby Power SupplyCurrent	I_{SB}	$\overline{CS}$=V_{IH}, Min Cycle		-	15	35	mA
	I_{SB1}	$\overline{CS}$ ≥ Vcc-0.2V, f=0 V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	-	1	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4.0mA		2.4	-	-	V

* Typ: V_{CC} = 5V, T_A = 25°C

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	7	pF

Note: Capacitance is sampled and not 100% tested.

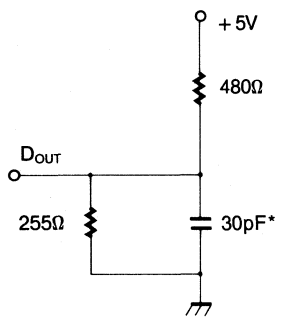
AC CHARACTERISTICS

TEST CONDITIONS

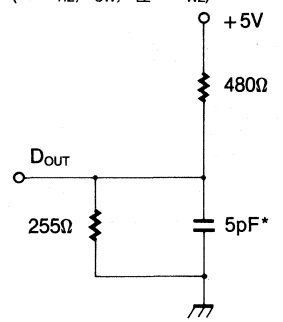
($T_A = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Loads	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{OW}, t_{LZ} & t_{WZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	-12		-15		-20		-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	12		15		20		25		ns
Address Access Time	t_{AA}		12		15		20		25	ns
Chip Select to Output	t_{CO}		12		15		20		25	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		3		ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	0	9	0	10	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns
Chip selection to Power Up Time	t_{PU}	0		0		0		0		ns
Chip Selection to Power Down Time	t_{PD}		12		15		20		25	ns

WRITE CYCLE

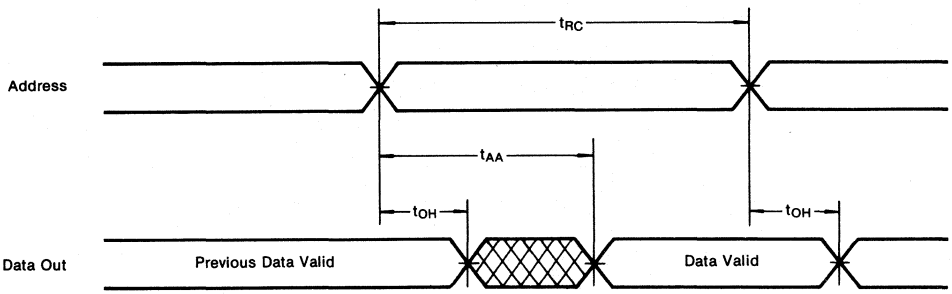
Parameter	Symbol	-12		-15		-20		-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	12		15		20		25		ns
Chip Select to End of Write	t_{CW}	10		12		13		15		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AW}	10		12		13		15		ns
Write Pulse Width	t_{WP}	10		12		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WZ}	0	7	0	8	0	9	0	10	ns
Data to Write Time Overlap	t_{DW}	8		9		10		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		0		ns

2

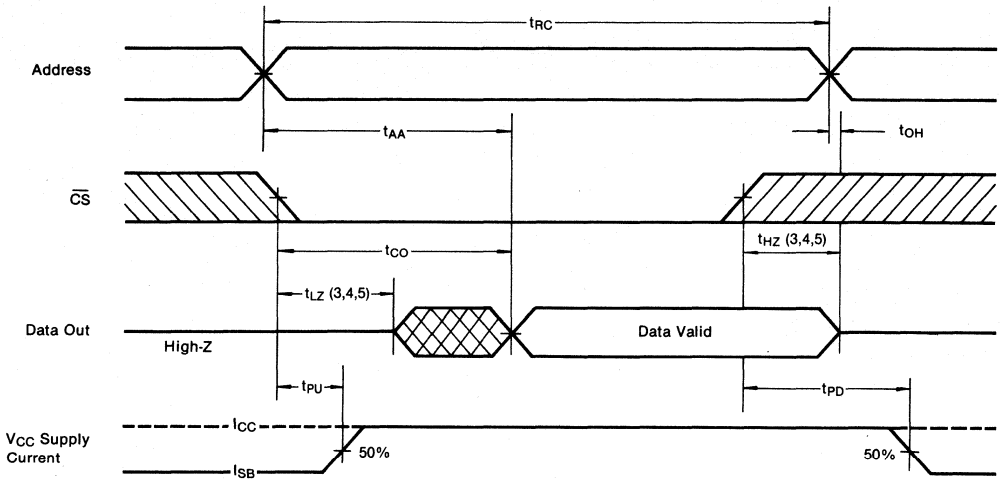
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=V_{IL}, $\overline{WE}$=V_{IH})



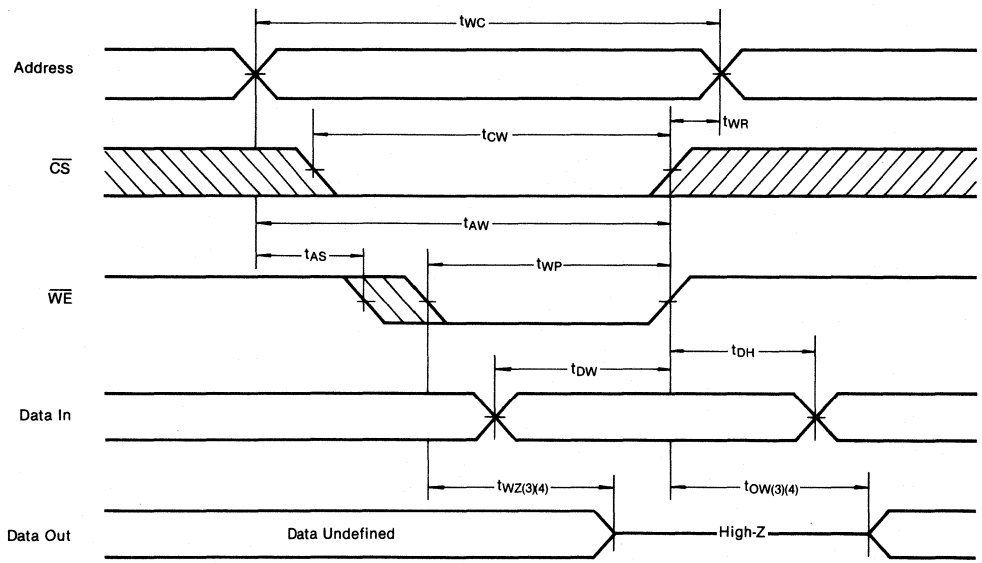
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



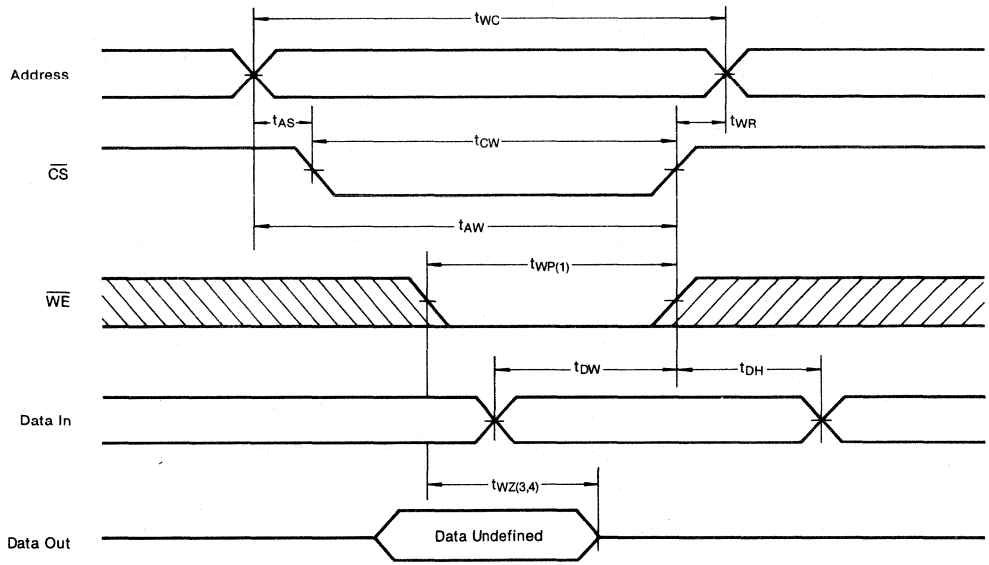
Notes (Read Cycle):

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max) is less than t_{LZ} (min) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B).
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=V_{IL}.
7. Address valid prior to coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ} (max.) is less than t_{OW} (min.) both for a given device and from device to device.
6. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	I/O Pin	Supply Current	Mode
H	X*	High-Z	I_{SB}, I_{SB1}	Not Select
L	H	D_{OUT}	I_{CC}	Read
L	L	D_{IN}	I_{CC}	Write

* Note: X means Don't Care.

16,384 WORD x 4 Bit CMOS Static RAM (With $\overline{OE}$)

FEATURES

- **Fast Access Time: 12, 15, 20, 25ns (max.)**
- **Low Power Dissipation**
  Standby (TTL) : 35mA (max.)
  (CMOS): 1mA (max.)
- **Operating KM6466B-12 : 140mA (max.)**
  KM6466B-15 : 130mA (max.)
  KM6466B-20 : 120mA (max.)
  KM6466B-25 : 110mA (max.)
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  No clock or refresh required
- **Three State Outputs**
- **Standard Pin Configuration**
  - KM6466BP : 24-DIP-300
  - KM6466BJ : 24-SOJ-300

GENERAL DESCRIPTION

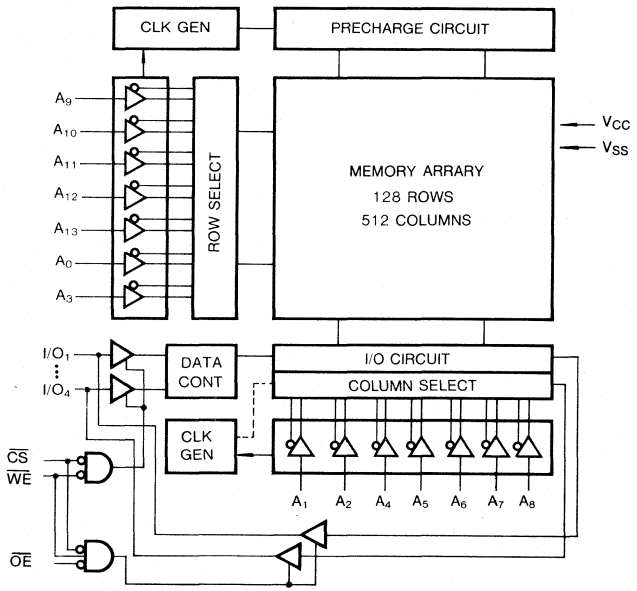
The KM6466B is a 65,536-bit high-speed Static Random Access Memory organized as 16,384 words by 4 bits.

The device is fabricated using Samsung's advanced CMOS process.

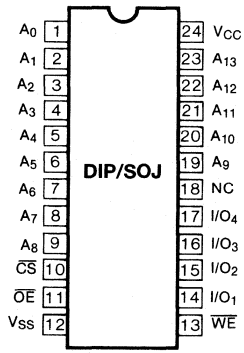
The KM6466B has a chip select input for the minimum current power down mode.

The KM6466B has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which batery back-up for nonvolatility is required.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Pin Name	Pin Function
A_0-A_{13}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_4	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.) = −3.0V for ≤20ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-	-	1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH}, $\overline{WE}$=V_{IL}, $V_{I/O}$=Vss to Vcc, Vcc=Max		-	-	1	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{OUT}=0mA	12ns	-	110	140	mA
			15ns	-	95	130	mA
			20ns	-	85	120	mA
			25ns	-	75	110	mA
Standby Power SupplyCurrent	I_{SB}	$\overline{CS}$=V_{IH}, Min Cycle		-	15	35	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0 V_{IN}≥Vcc-0.2V or V_{IN} ≤0.2V		-	-	1	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4.0mA		2.4	-	-	V

* Typ: V_{CC} = 5V, T_A = 25°C

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

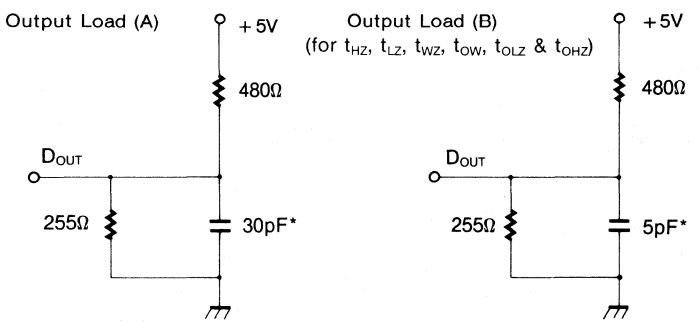
Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	7	pF

Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Loads	See below



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	-12		-15		-20		-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	12		15		20		25		ns
Address Access Time	t_{AA}		12		15		20		25	ns
Chip Select to Output	t_{CO}		12		15		20		25	ns
Output Enable to Valid Output	t_{OE}		7		8		9		10	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	0	9	0	10	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns
Chip selection to Power Up Time	t_{PU}	0		0		0		0		ns
Chip Selection to Power Down Time	t_{PD}		12		15		20		25	ns

WRITE CYCLE

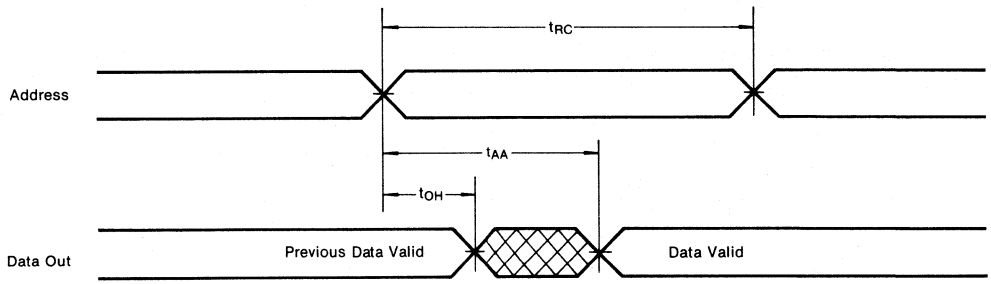
Parameter	Symbol	-12		-15		-20		-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	12		15		20		25		ns
Chip Select to End of Write	t_{CW}	10		12		13		15		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AW}	10		12		13		15		ns
Write Pulse Width	t_{WP}	10		12		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WZ}	0	7	0	8	0	9	0	10	ns
Data to Write Time Overlap	t_{DW}	8		9		10		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		0		ns

2

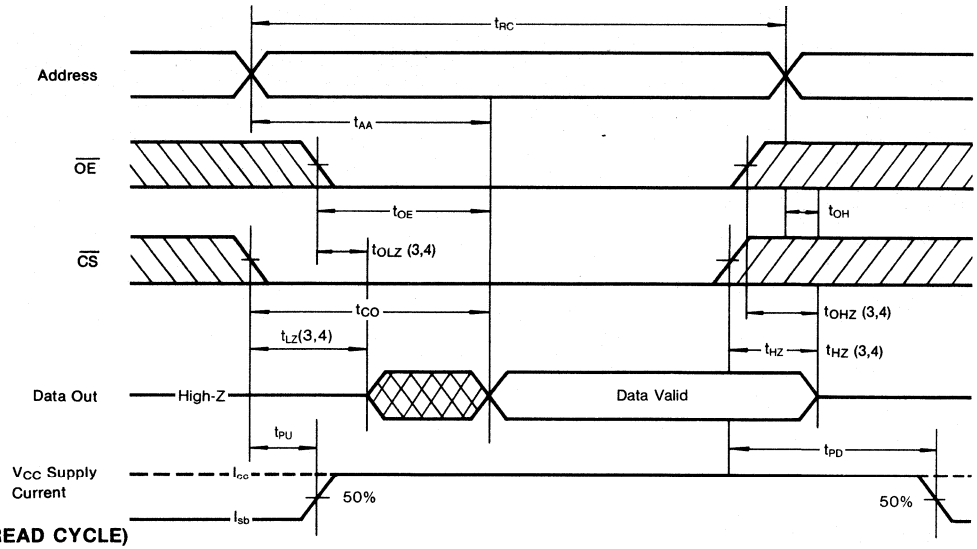
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS} = V_{IL}$, $\overline{WE} = V_{IH}$, $\overline{OE} = V_{IL}$)



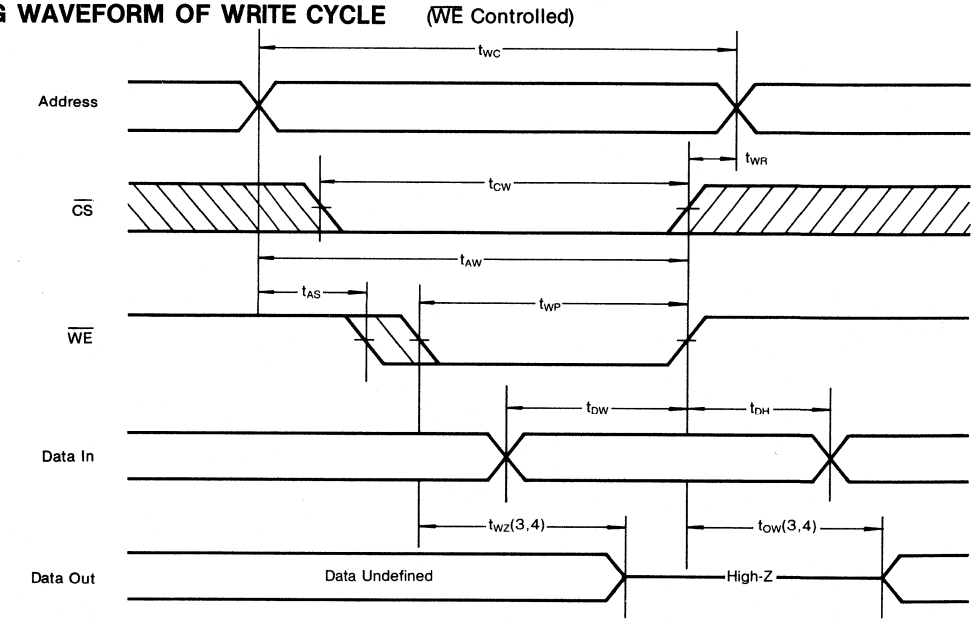
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



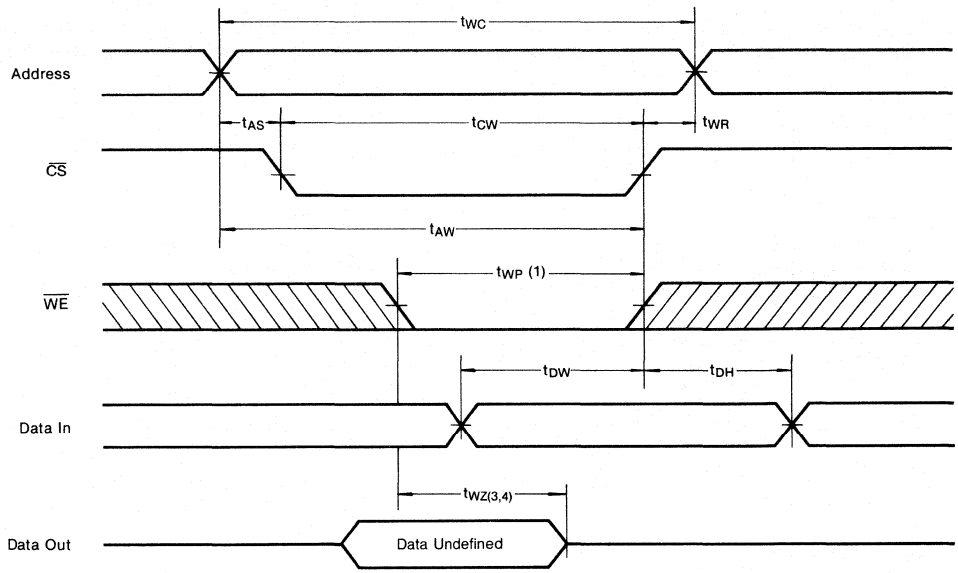
Notes (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Device is continuously selected with $\overline{CS}$=V_{IL}.
6. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ} (max.) is less than t_{OW} (min.) both for a given device and from device to device.
6. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.
7. $\overline{OE}$ is high for write cycle.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current	Mode
H	X	X	High-Z	I_{SB}, I_{SB1}	Not Select
L	H	L	D_{OUT}	I_{CC}	Read
L	L	X	D_{IN}	I_{CC}	Write

* Note: X means Don't Care.

8,192 WORD×8 Bit High Speed CMOS Static RAM

FEATURES

- **Fast Access Time: 12, 15, 20, 25ns (max.)**
- **Low Power Dissipation**
  Standby (TTL) : 35mA (max.)
  (CMOS): 1mA (max.)
- **Operating KM6865B-12 : 140mA (max.)**
  KM6865B-15 : 130mA (max.)
  KM6865B-20 : 120mA (max.)
  KM6865B-25 : 110mA (max.)
- **Single 5V±10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  No clock or refresh required
- **Three State Outputs**
- **Standard Pin Configuration**
  —KM6865BP : 28-DIP-300
  —KM6865BJ : 28-SOJ-300

GENERAL DESCRIPTION

The KM6865B is a 65,536-bit high-speed Static Random Access Memory organized as 8,192 words by 8 bits.

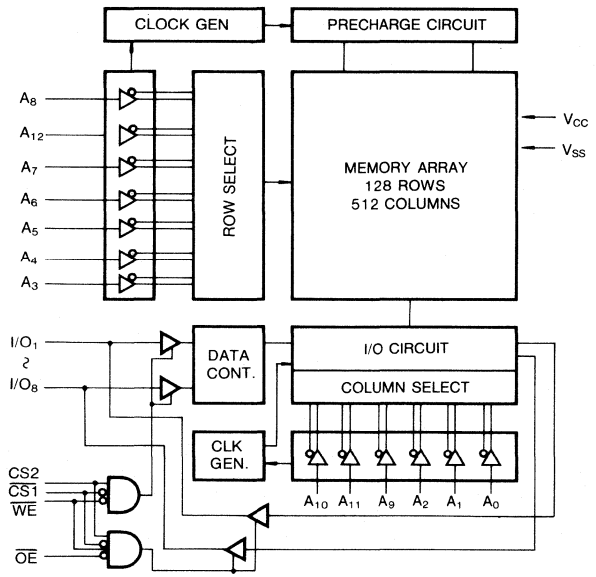
The KM6865B uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.

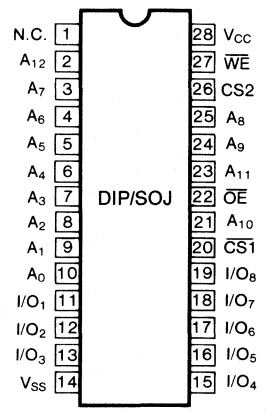
It is particularly well suited for use in high-density high-speed system applications.

The KM6865B is packaged in a 300 mil. 28-pin plastic DIP or SOJ

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Pin Name	Pin Function
A_0-A_{12}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS1}$, CS2	Chip Selects
$\overline{OE}$	Output Enable
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.) = −3.0V for ≤10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-	-	1	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH}, or CS2=V_{IL}, $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}, V_{CC}=Max		-	-	1	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty, $\overline{CS1}$=V_{IL}, CS2=V_{IH}, I_{OUT}=0mA	12ns	-	110	140	mA
			15ns	-	95	130	mA
			20ns	-	85	120	mA
			25ns	-	75	110	mA
Standby Power SupplyCurrent	I_{SB}	$\overline{CS1}$=V_{IH}, or CS2=V_{IL}, Min Cycle		-	15	35	mA
	I_{SB1}	$\overline{CS1}$ ≥ V_{CC}-0.2V, CS2 ≤ 0.2V, f=0 V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V		-	-	1	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4.0mA		2.4	-	-	V

*Typ : V_{CC}=5V, T_A=25° C

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	7	pF

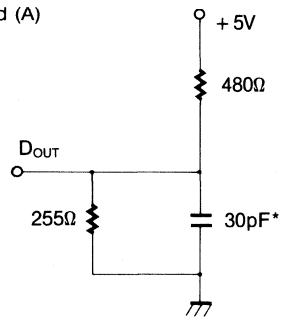
Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

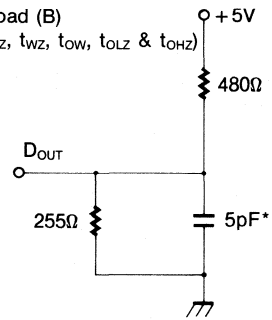
TEST CONDITIONS ($T_A = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Loads	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	-12		-15		-20		-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	12		15		20		25		ns
Address Access Time	t_{AA}		12		15		20		25	ns
Chip Select to Output	t_{CO}		12		15		20		25	ns
Output Enable to Valid Output	t_{OE}		8		8		10		12	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	0	9	0	10	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns
Chip selection to Power Up Time	t_{PU}	0		0		0		0		ns
Chip Selection to Power Down Time	t_{PD}		12		15		20		25	ns

WRITE CYCLE

Parameter	Symbol	-12		-15		-20		-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	12		15		20		25		ns
Chip Select to End of Write	t_{CW}	10		12		13		15		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AW}	10		12		13		15		ns
Write Pulse Width	t_{WP}	10		12		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WZ}	0	7	0	8	0	9	0	10	ns
Data to Write Time Overlap	t_{DW}	8		9		10		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		0		ns

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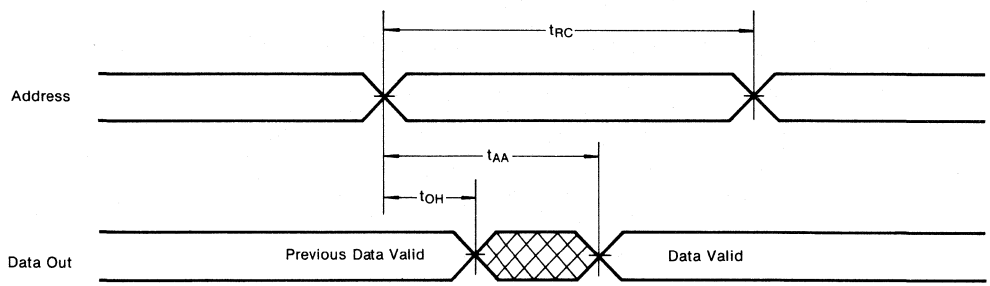
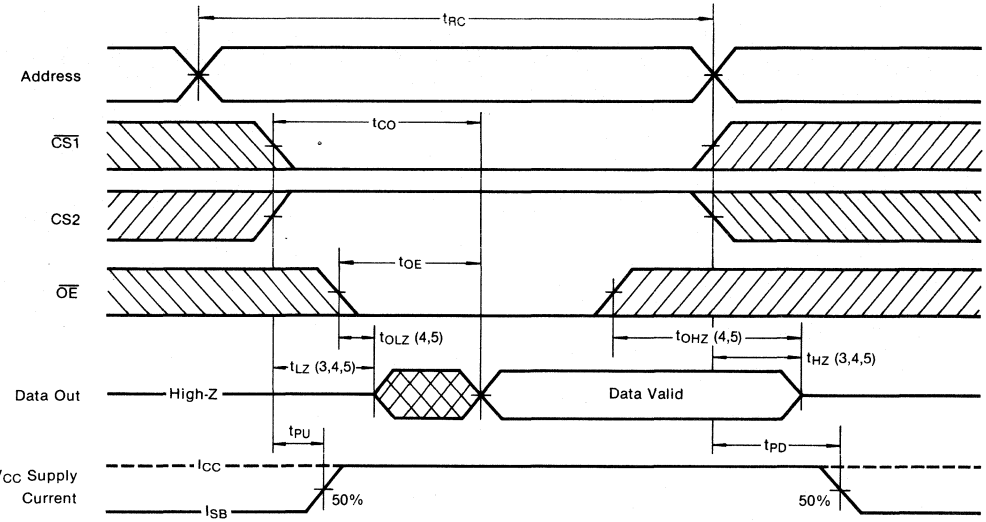
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS1} = \overline{OE} = V_{IL}$, $CS2 = \overline{WE} = V_{IH}$)



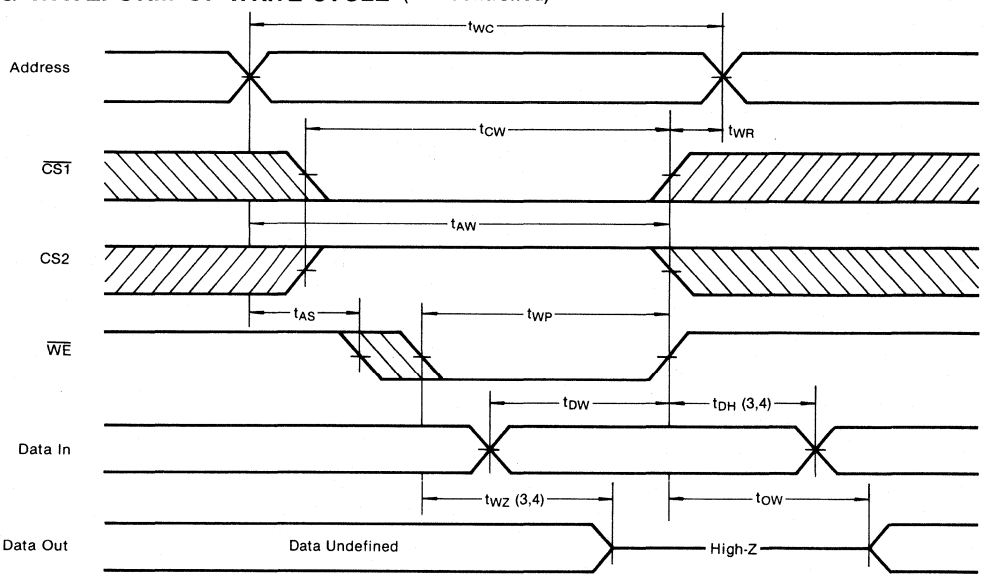
TIMING WAVEFORM OF READ CYCLE



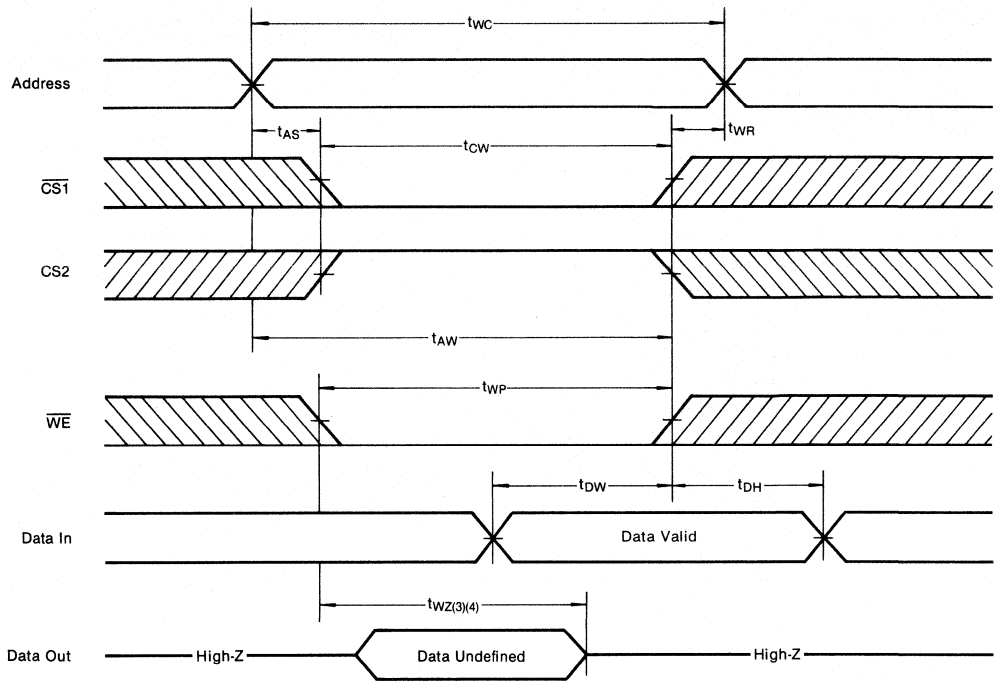
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max) is less than t_{LZ} (min) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B).
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS_1}=V_{IL}$, $CS_2=V_{IH}$.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS1}$, CS2 and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ} (max.) is less than t_{OW} (min.) both for a given device and from device to device.
6. $\overline{CS1}$ or $\overline{WE}$ must be high or CS2 must be low during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

65,536 WORDx4 Bit High Speed CMOS Static RAM

FEATURES

- **Fast Access Time : 12, 15, 20ns(Max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 40mA (max.)**
  - **(CMOS) : 2mA(max.)**
  - **Operating : KM64258C-12 : 150mA (max.)**
  - **KM64258C-15 : 140mA (max.)**
  - **KM64258C-20 : 130mA (max.)**
- **Single 5V±10% power supply**
- **TTL compatible inputs and outputs**
- **I/O tolerence & compatible with 3.3V Device**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three state Output**
- **Standard Pin Configuration**
  - **KM64258CJ : 28-SOJ-300**

GENERAL DESCRIPTION

The KM64258C is a 262,144 bit high speed Static Random Access Memory organized as 65, 536 words by 4 bits.

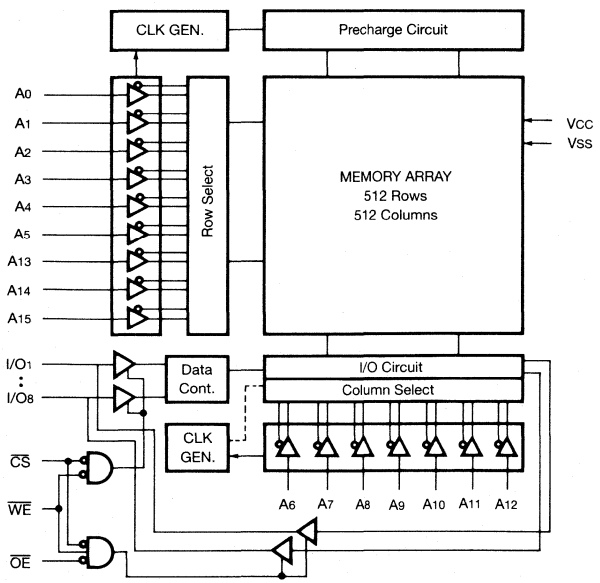
The KM64258C uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology.

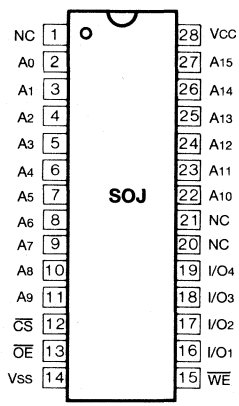
It is particulay well suited for use in high-density high-speed system applications.

The KM64258C is packaged in a 300mil 28-pin plastic SOJ

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A15	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
VCC	Power(+5V)
VSS	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	-65 to 150	°C
Operating Temperature	T_a	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260° C, 10sec(Lead only)	-

* Stresses greater than those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.5*	—	0.8	V

* V_{IL}(min)=-3.0V for $\leq$ 10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V$\pm$10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CC}		-	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IN} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} or $V_{I/O}$=Vss to V_{CC}		-	2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{out}=0mA	12ns	-	150	mA
			15ns	-	140	mA
			20ns	-	130	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min Cycle.		-	40	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}$-0.2V f= o $V_{IN}\geq V_{CC}$-0.2 or $V_{IN}\leq$0.2V		-	2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	V

Note : * Temp=25° C, V_{CC}=5V$\pm$5%

CAPACITANCE (f=1MHz T_A=25°C)*

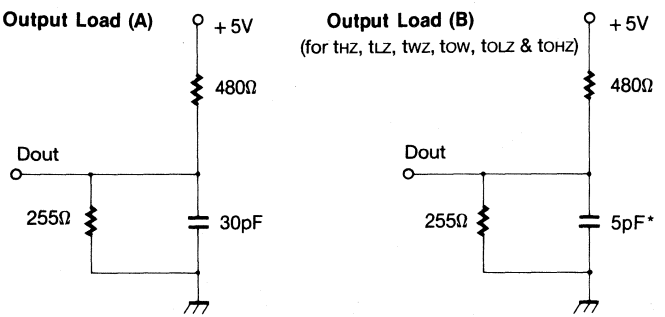
Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	7	pF

* Note : Capacitance is sampled and not 100% tested.

AC CHARACTERISCS

TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	See below



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	12		15		20		ns
Address Access Time	t_{AA}		12		15		20	ns
Chip Select to Output	t_{CO}		12		15		20	ns
Output Enable to Valid Output	t_{OE}		6		7		9	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	8	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Chip selection to Power Up time	t_{PU}	0		0		0		ns
Chip selection to Power Down Time	t_{PD}		12		15		20	ns

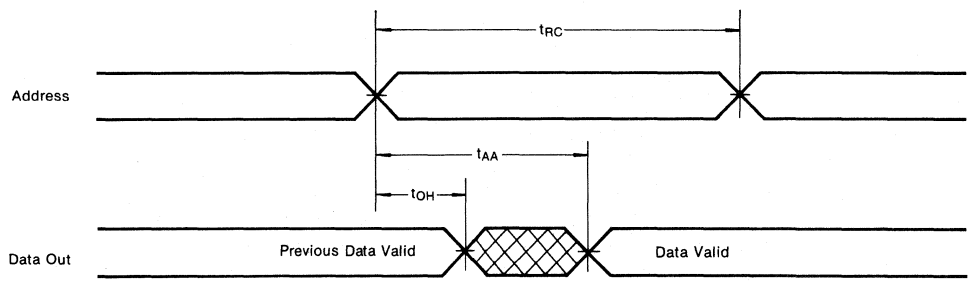
WRITE CYCLE

Parameter	Symbol	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	12		15		20		ns
Chip Select to End of Write	t_{CW}	9		11		13		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	9		12		13		ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	9		12		13		ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP}	12		15		20		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	6	0	8	0	8	ns
Data to Write Time Overlap	t_{DW}	7		8		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		ns

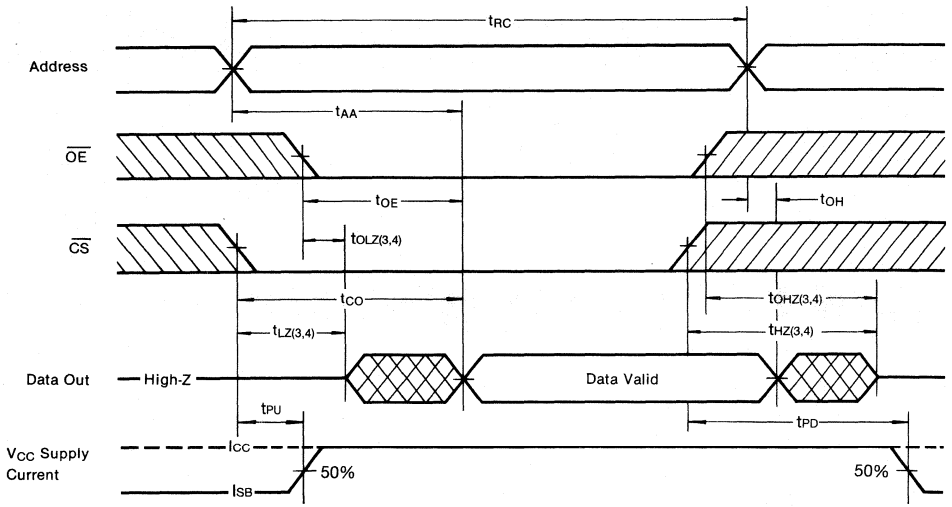
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



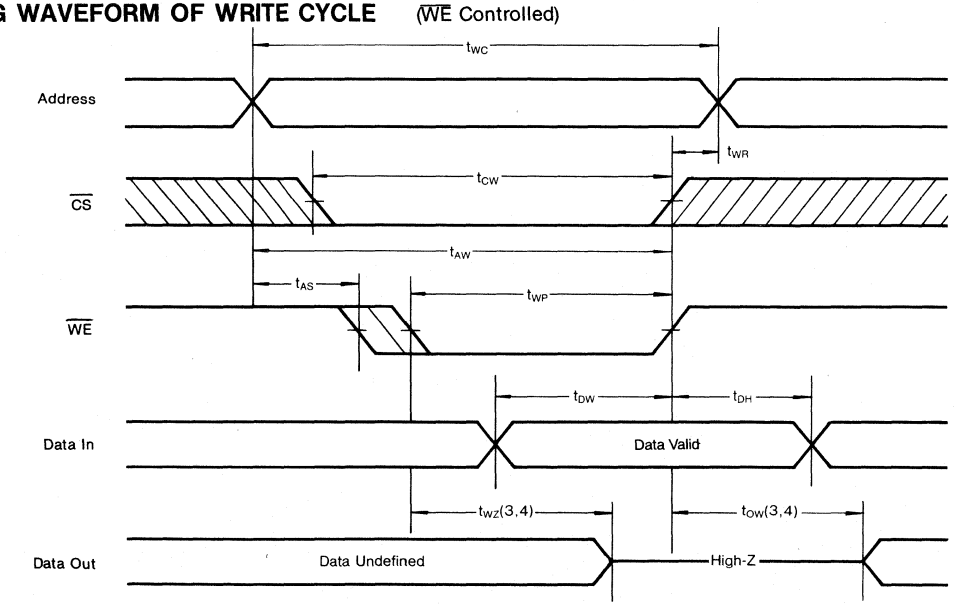
TIMING WAVEFORM OF READ CYCLE



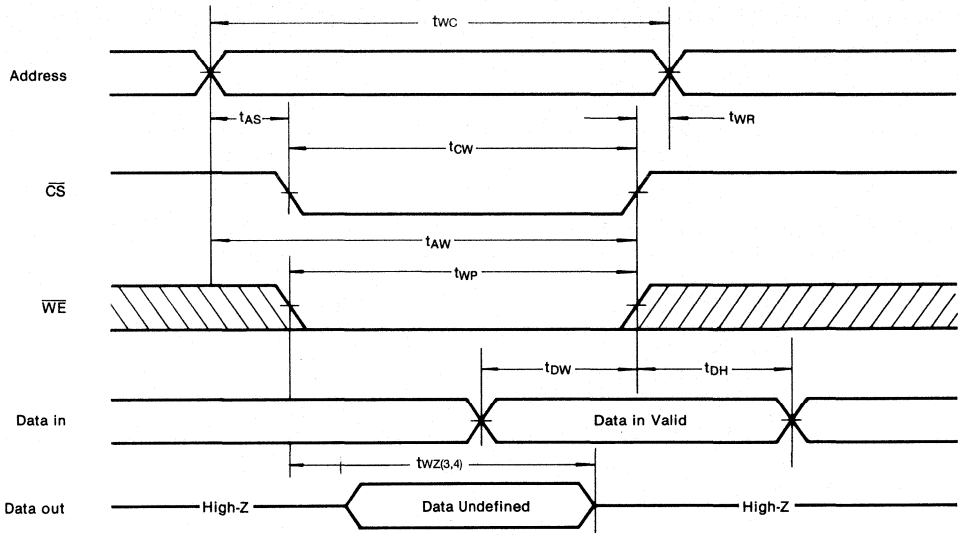
Note (Read cycle)

1. $\overline{WE}$ is high for read cycle
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less the than t_{LZ}(min.) both for a given device and from device to device
4. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
5. Address valid prior to or coincident with $\overline{CS}$ transition low.
6. Device is continuously selected with $\overline{CS}$=V_{IL}

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (Write cycle)

1. A write occurs during the overlap(tWP) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing i sreferenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B) This parameter is sampled and not 100% tested.
4. At any given temperaturd and voltage condition, twz(max.) is less than tow(min.) both for a given device and fiom device to device.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address teansition.

FUNCTION DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	ISB, ISB1
L	H	H	Output disable	High-Z	ICC
L	H	L	Read	DOUT	ICC
L	L	X	Write	DIN	ICC

Note : X means Don't Care

32,768 WORD x 8 Bit High Speed CMOS Static RAM

FEATURES

- **Fast Access Time : 12, 15, 20ns(Max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 40mA (max.)**
  - **(CMOS) : 2mA (max)**
  - **Operating : KM68257C-12 : 165mA (max.)**
  - **KM68257C-15 : 150mA (max.)**
  - **KM68257C-20 : 140mA (max.)**
- **Single 5V±10% power supply**
- **TTL compatible inputs and outputs**
- **I/O Tolerence & compatible with 3.3V Device**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three state Output**
- **Standard Pin Configuration**
  - **KM68257CP : 28-DIP-300**
  - **KM68257CJ : 28-SOJ-300**

GENERAL DESCRIPTION

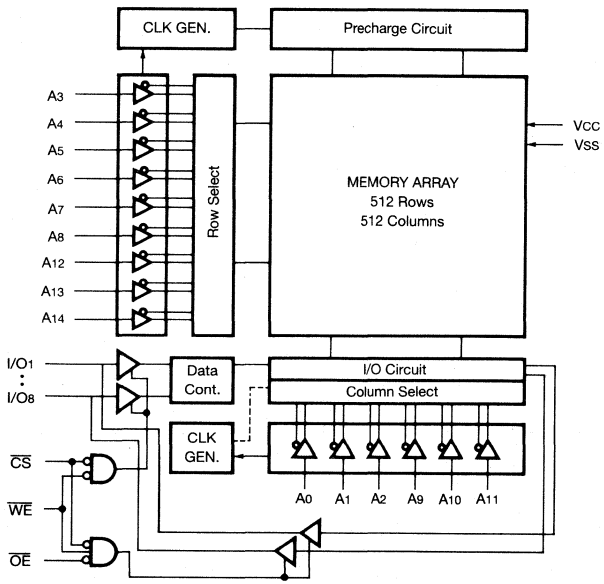
The KM68257C is a 262,144 bit high speed Static Random Access Memory organized as 32,768 words by 8 bits.

The KM68257C uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.

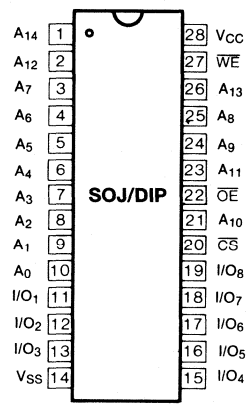
It is particularly well suited for use in high-density high-speed system applications.

The KM68257C is packaged in a 300mil 28-pin plastic SOJ and DIP

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A14	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O8	Data Inputs/Outputs
VCC	Power(+5V)
VSS	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	-65 to 150	°C
Operating Temperature	T_a	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260° C, 10sec(Lead only)	-

* Stresses greater than those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(min)=-3.0V for $\leq$ 10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CC}		-	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IN} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=Vss to V_{CC}		-	2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{out}=0mA	12ns	-	165	mA
			15ns	-	150	mA
			20ns	-	140	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min Cycle.		-	40	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, f= o V_{IN}≥V_{CC}-0.2 or V_{IN}≤0.2V		-	2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	V

Note : * Temp=25° C, V_{CC}=5V±5%

CAPACITANCE (f=1MHz T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

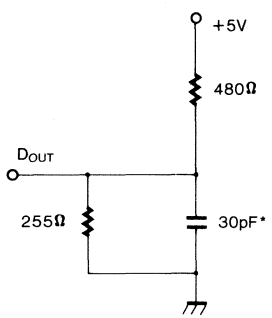
* Note : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

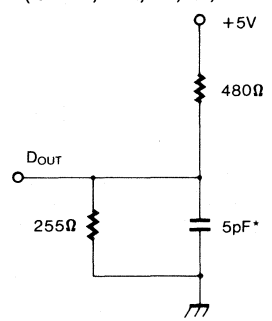
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{OLZ}, t_{OHZ}, t_{HZ}, t_{LZ}, t_{WO} & t_{WZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	12		15		20		ns
Address Access Time	t_{AA}		12		15		20	ns
Chip Select to Output	t_{CO}		12		15		20	ns
Output Enable to Valid Output	t_{OE}		6		7		9	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	8	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Chip selection to Power Up time	t_{PU}	0		0		0		ns
Chip selection to Power Down Time	t_{PD}		12		15		20	ns

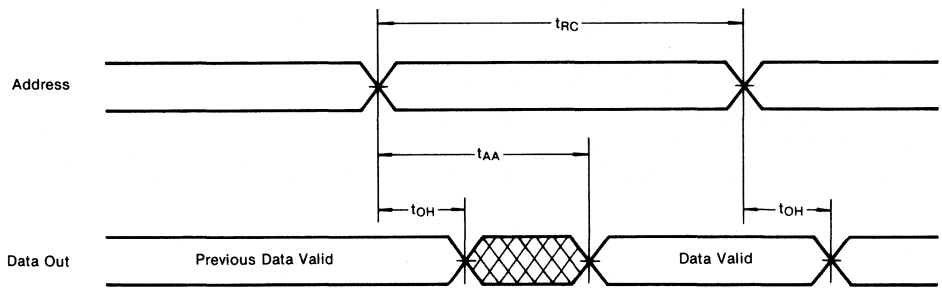
WRITE CYCLE

Parameter	Symbol	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	12		15		20		ns
Chip Select to End of Write	tCW	9		11		13		ns
Address Set-up Time	tAS	0		0		0		ns
Address Valid to End of Write	tAW	9		12		13		ns
Write Pulse Width($\overline{OE}$ High)	tWP	9		12		13		ns
Write Pulse Width($\overline{OE}$ Low)	tWP	12		15		20		ns
Write Recovery Time	tWR	0		0		0		ns
Write to Output High-Z	tWZ	0	6	0	8	0	8	ns
Data to Write Time Overlap	tDW	7		8		10		ns
Data Hold from Write Time	tDH	0		0		0		ns
End Write to Output Low-Z	tOW	0		0		0		ns

TIMING DIAGRAMS

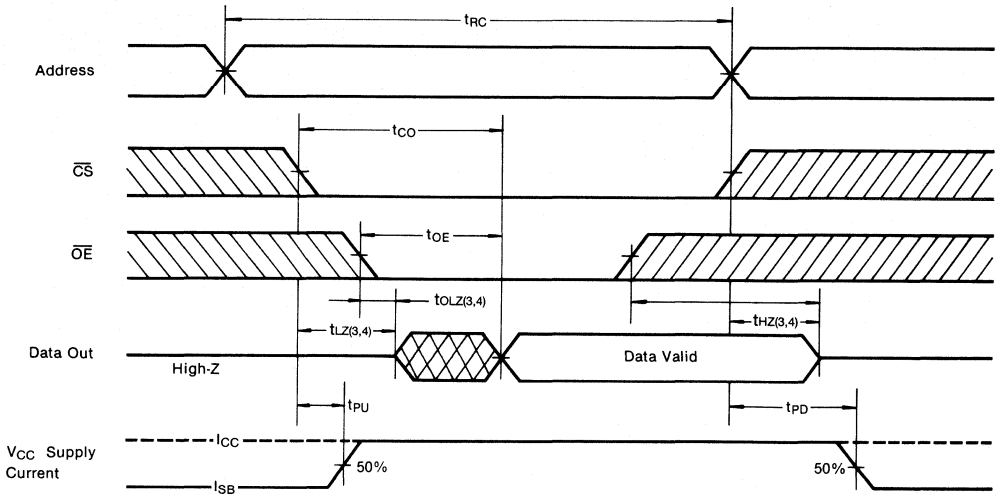
TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



SAMSUNG ELECTRONICS

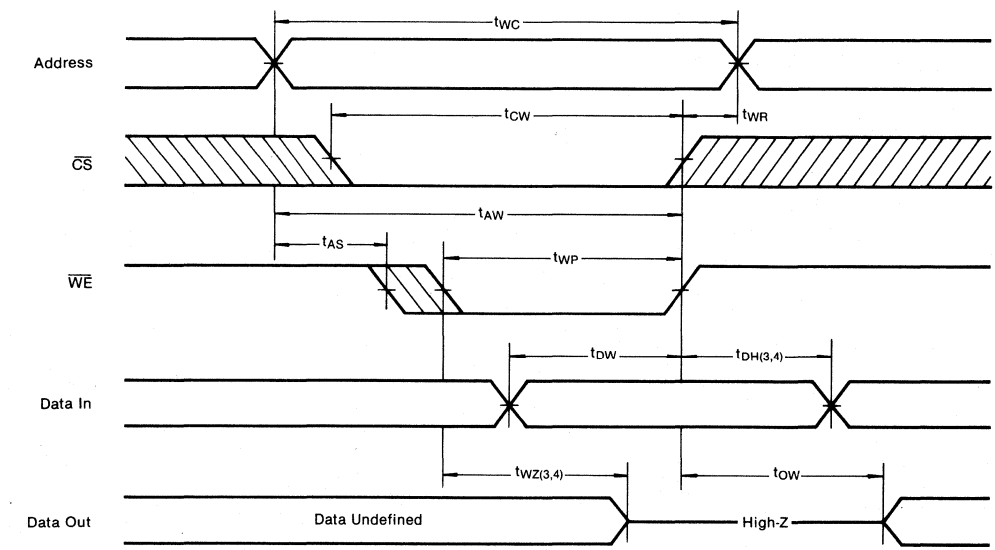
TIMING WAVEFORM OF READ CYCLE



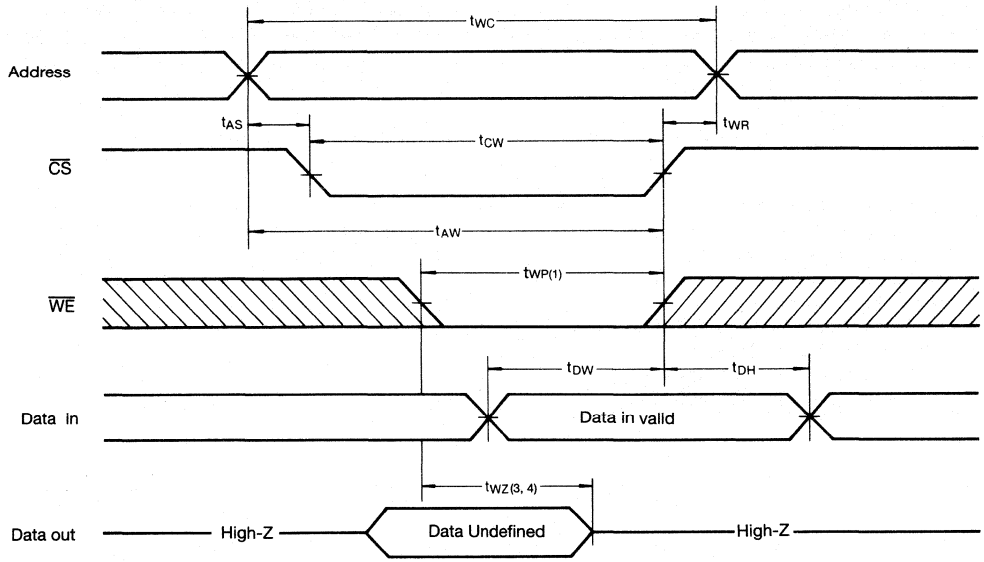
Notes(Read Cycle)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ± 200mV from steady state voltage with Load (B)
   This parameter is sampled and not 100% tested.
5. Address valid prior to or coincident with $\overline{CS}$ transition low.
6. Device is continuously Selected with $\overline{CS}$=V_{IL}.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes(Write cycle)

1. A write occurs during the overlap(tWP) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B)
   This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, twz(max.) is less than tow(min.) both for a given device and fiom device to device.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTION DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	ISB, ISB1
L	H	H	Output Disable	High-Z	ICC
L	H	L	Read	DOUT	ICC
L	L	X	Write	DIN	ICC

Note : X means Don't Care

262,144 WORD x 4 Bit High-Speed CMOS Static RAM

FEATURES

- **Fast Access Time : 20, 25, 35ns(max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 40mA (max.)**
  - **(CMOS) : 2mA (max)**
  - **Operating : KM641001-20 : 150mA (max.)**
  - **KM641001-25 : 130mA (max.)**
  - **KM641001-35 : 110mA (max.)**
- **Single 5V±10% power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three state Output**
- **Low Data Retention Voltage : 2V(min.)**
- **Standard Pin Configuration**
  - **KM641001P : 28-DIP-400**
  - **KM641001J : 28-SOJ-400**

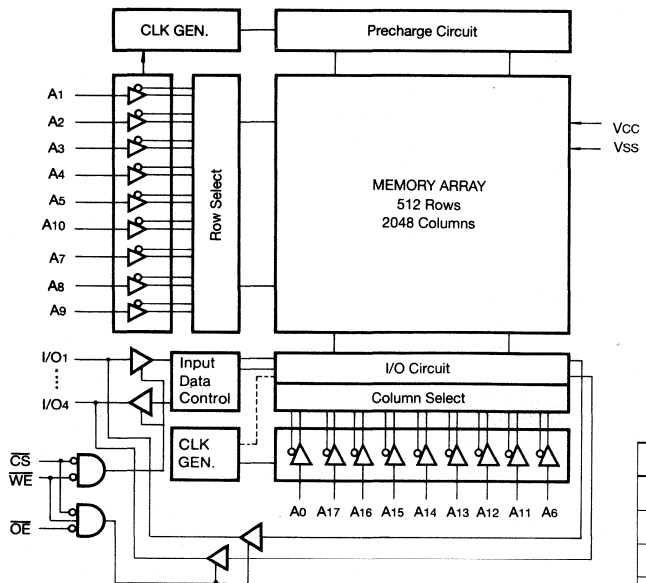
GENERAL DESCRIPTION

The KM641001 is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits.

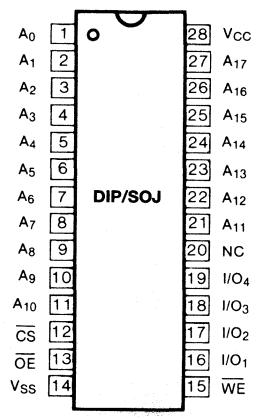
The KM641001 uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM641001 is packaged in a 400mil 28-pin plastic DIP or SOJ with the conventionnal power-supply pinout.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Pin Name	Pin Function
A0-A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Inputs/Outputs
VCC	Power(+5V)
VSS	Ground
NC	NO Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	-65 to +150	°C
Operating Temperature	T_a	0 to 70	°C

* Stresses greater than those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.5*	—	0.8	V

* V_{IL}(min.)=-3.0V for ≤ 10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IN} or $\overline{WE}$=V_{IL}, V_{OUT}=V_{SS} to V_{CC}		-	2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{out}=0mA	20ns	-	150	mA
			25ns	-	130	
			35ns	-	110	
Standby Power	I_{SB}	$\overline{CS}$=V_{IH}, Min Cycle.		-	40	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, f= o V_{IN}≤0.2 or V_{IN}≥V_{CC}-0.2V		-	2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE* (f=1MHz, T_A=25°C)

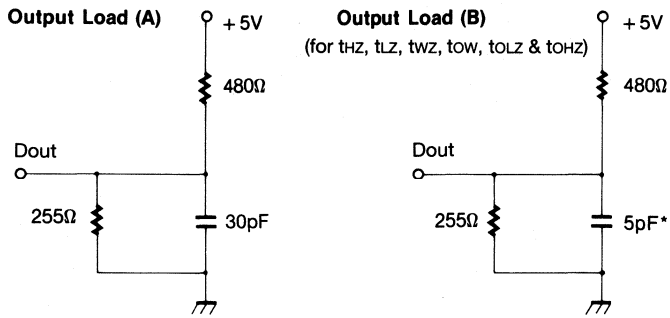
Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	7	pF

* Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	See below



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20		25		35		ns
Address Access Time	t_{AA}		20		25		35	ns
Chip Select to Output	t_{CO}		20		25		35	ns
Output Enable to Output	t_{OE}		10		13		15	ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Enable to Low-Z Output	t_{LZ}	0		0		0		ns
Output Disable to High-Z Output	t_{OHZ}	0	8	0	10	0	15	ns
Chip Disable to High-Z Output	t_{HZ}	0	12	0	15	0	15	ns
Output Hold from Address Change	t_{OH}	3		5		5		ns
Chip select to Power Up time	t_{PU}	0		0		0		ns
Chip Disable to Power Down Time	t_{PD}		20		25		35	ns

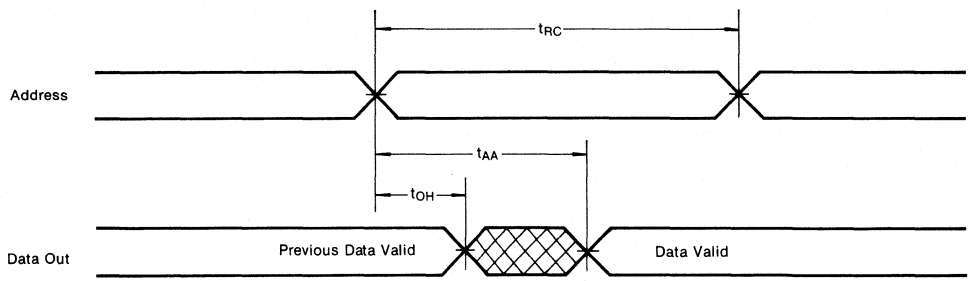
WRITE CYCLE

Parameter	Symbol	-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	20		25		35		ns
Chip Select to End of Write	t_{CW}	17		20		30		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	17		20		30		ns
Write Pulse Width	t_{WP}	15		20		25		ns
Write Recovery Time	t_{WR}	2		3		3		ns
Write to Output High-Z	t_{WZ}	0	8	0	10	0	12	ns
Data to Write Time Overlap	t_{DW}	12		15		20		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		ns

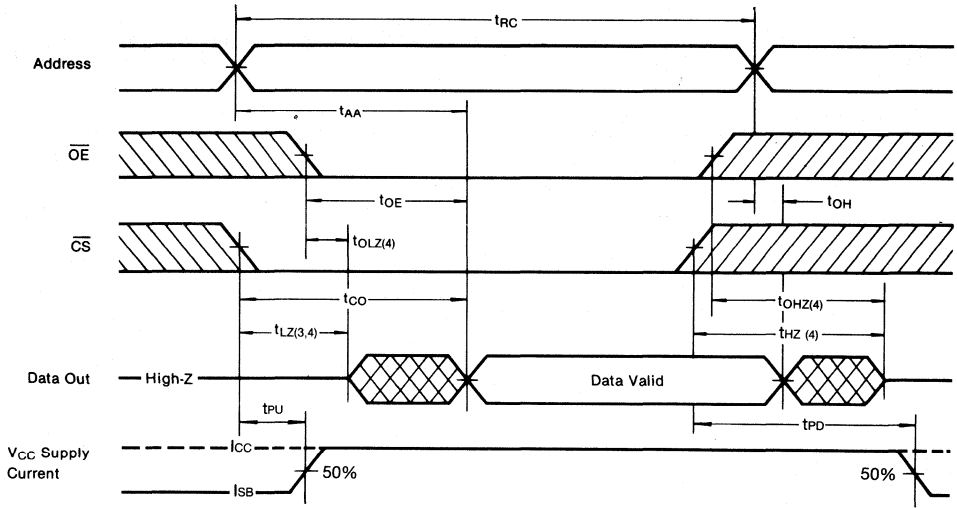
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



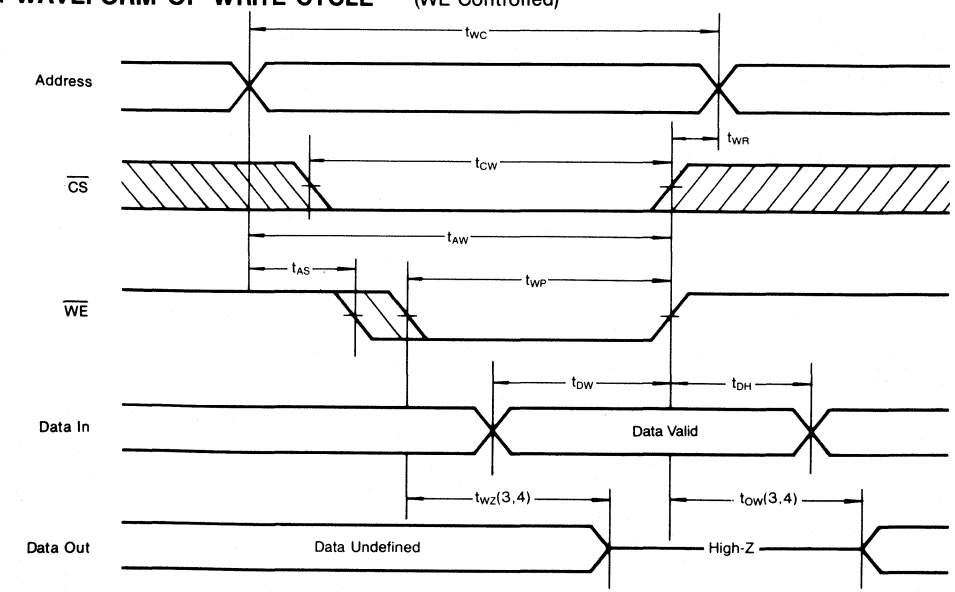
TIMING WAVEFORM OF READ CYCLE



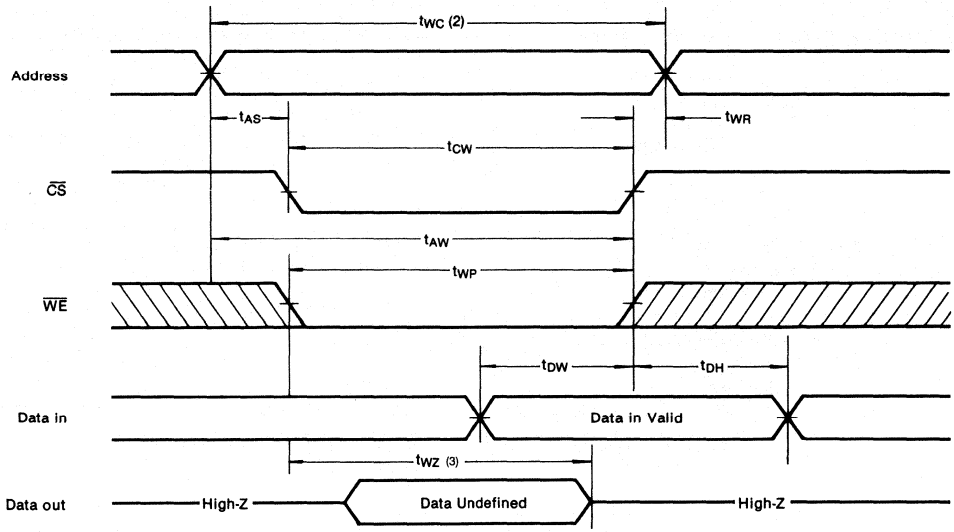
Note (Read cycle)

1. $\overline{WE}$ is high for read cycle
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less the than t_{LZ}(min.) both for a given device and from device to device
4. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
5. Device is continuously selected with $\overline{CS}$=V_{IL}
6. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Note (Write cycle)
1. A write occurs during the overlap(tWP) of a low $\overline{WE}$.
2. All write cycle timing i sreferenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B) This paramitoc is sampled and not 100% tested.
4. At any given temperaturd and voltage condition, twz(max) is less than tow(min) both for a given device and fiom device to device.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address teansition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current	Mode
H	X	X	High-Z	I_{SB}, I_{SB1}	Not Select
L	L	H	D_{OUT}	I_{CC}	Read
L	L	L	D_{IN}	I_{CC}	Write
L	H	L	D_{IN}	I_{CC}	Write

Note : X means Don't Care

262,144 WORD x 4 Bit High-Speed CMOS Static RAM

FEATURES

- **Fast Access Time: 15, 17, 20ns (Max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 40mA (Max.)**
  - **(CMOS): 10mA (Max.)**
  - **Operating : KM641003-15 : 170mA (Max.)**
  - **KM641003-17 : 160mA (Max.)**
  - **KM641003-20 : 150mA (Max.)**
- **Single 5V ± 10% Power Supply**
- **TTL compatible inputs and outputs**
- **I/O tolerence & compatible with 3.3V Dvice**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three state Output**
- **Center Power/Ground Pin Configuration**
- **Standard Pin Configuration**
  KM641003J : 32-SOJ-400

GENERAL DESCRIPTION

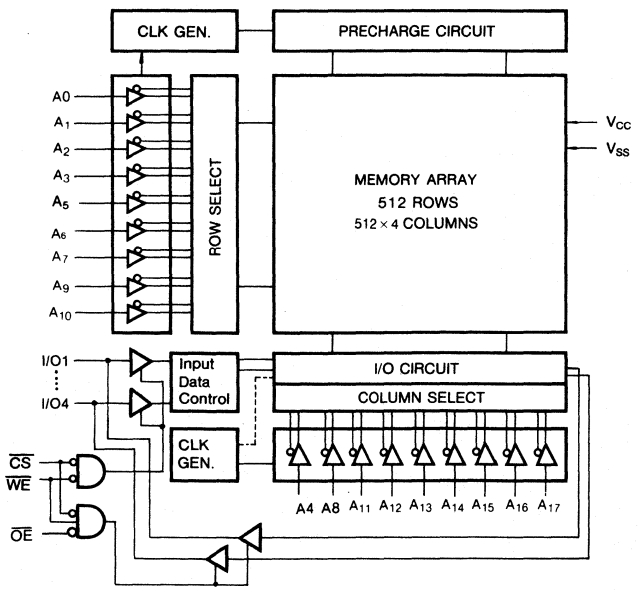
The KM641003 is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits.

The KM641003 uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

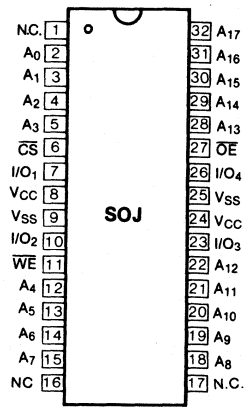
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM641003 is packaged in a 400mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Pin Name	Pin Function
A0-A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output enable
I/O1-I/O4	Data Inputs/Outputs
VCC	Power (+5V)
VSS	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	-65 to 150	°C
Operating Temperature	T_a	0 to 70	°C

* Stresses greater than those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.5*	—	0.8	V

* V_{IL}(min.)=-3.0V for ≤ 10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CC}		-2	+2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=Vss to V_{CC}		-2	+2	μA
Average Operating Current	I_{CC1}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{OUT}=0mA	15ns	-	170	mA
			17ns	-	160	
			20ns	-	150	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, V_{IN}=V_{IH}/V_{IL}, Min Cycle.		-	40	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V f= o V_{IN}≥V_{CC}-0.2 V or V_{IN}≤0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4.0mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	V

Note : V_{CC}=5V±5%, Temp=25° C

CAPACITANCE (f=1MHz, T_A=25°C)*

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	8	pF

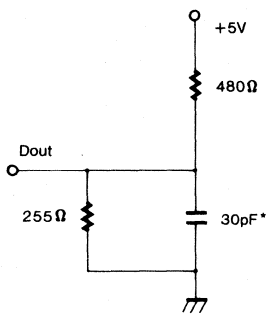
* Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

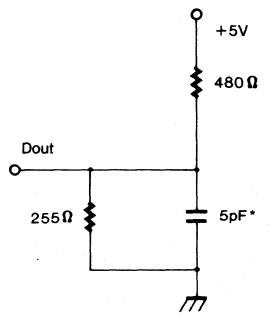
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(t_{OLZ},t_{OHZ}, t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



*Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	-15		-17		-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		ns
Address Access Time	t_{AA}		15		17		20	ns
Chip Select to Output	t_{CO}		15		17		20	ns
Output Enable to Output	t_{OE}		8		9		10	ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Enable to Low-Z Output	t_{LZ}	3		3		3		ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	8	ns
Output Hold from Address Change	t_{OH}	3		3		5		ns
Chip Select to Power Up Time	t_{PU}	0		0		0		ns
Chip Disable to Power Down Time	t_{PD}		15		17		20	ns

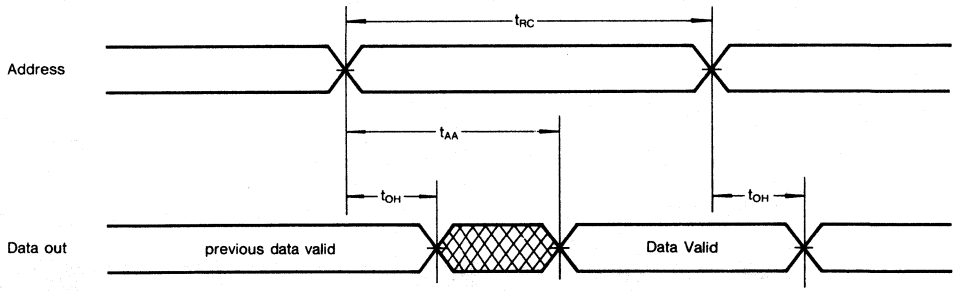
WRITE CYCLE

Parameter	Symbol	-15		-17		-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		ns
Chip Select to End of Write	t_{CW}	12		12		13		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	12		12		13		ns
Write Pulse Width	t_{WP}	12		12		13		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	8	0	8	0	10	ns
Data to Write Time Overlap	t_{DW}	8		9		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End of Write to Output Low-Z	t_{OW}	3		4		5		ns

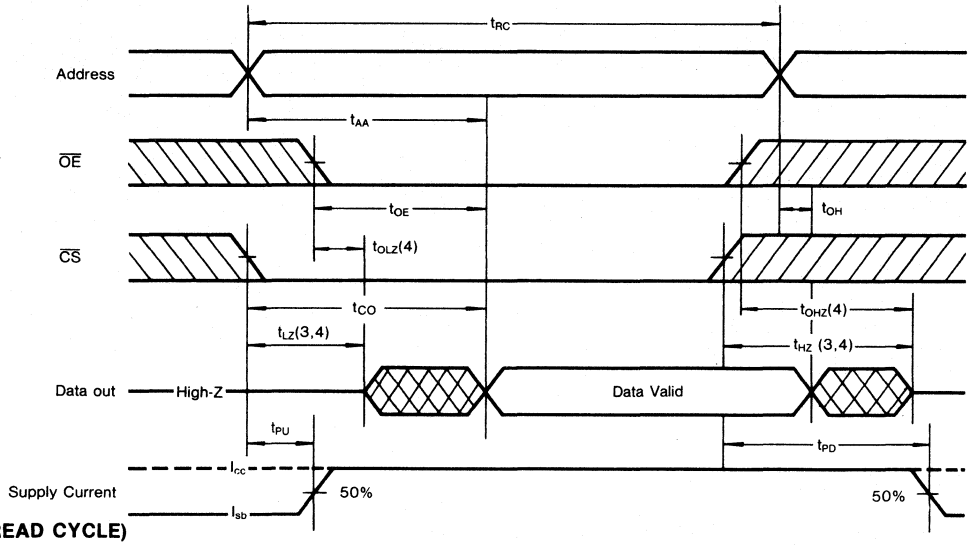
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



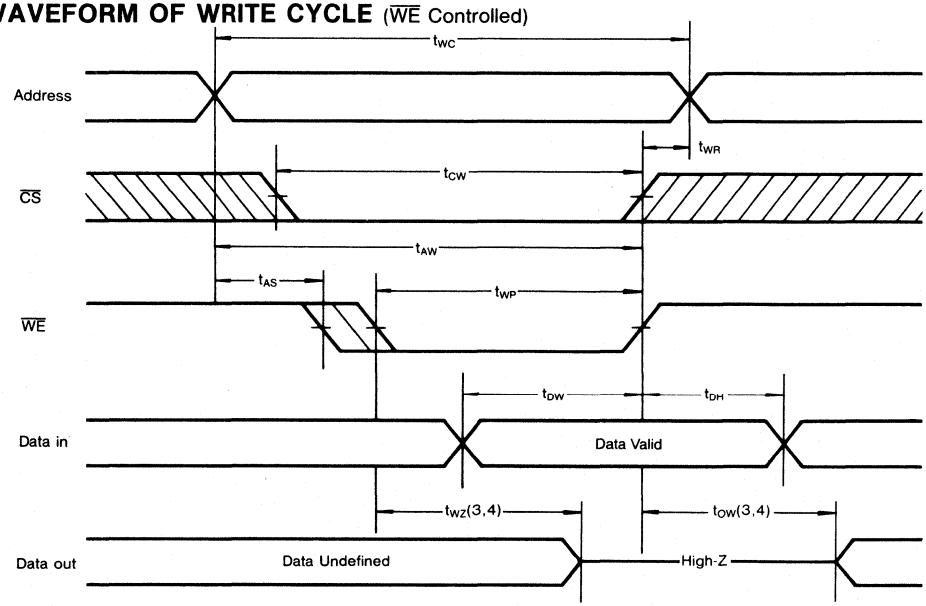
TIMING WAVEFORM OF READ CYCLE



Notes (READ CYCLE)

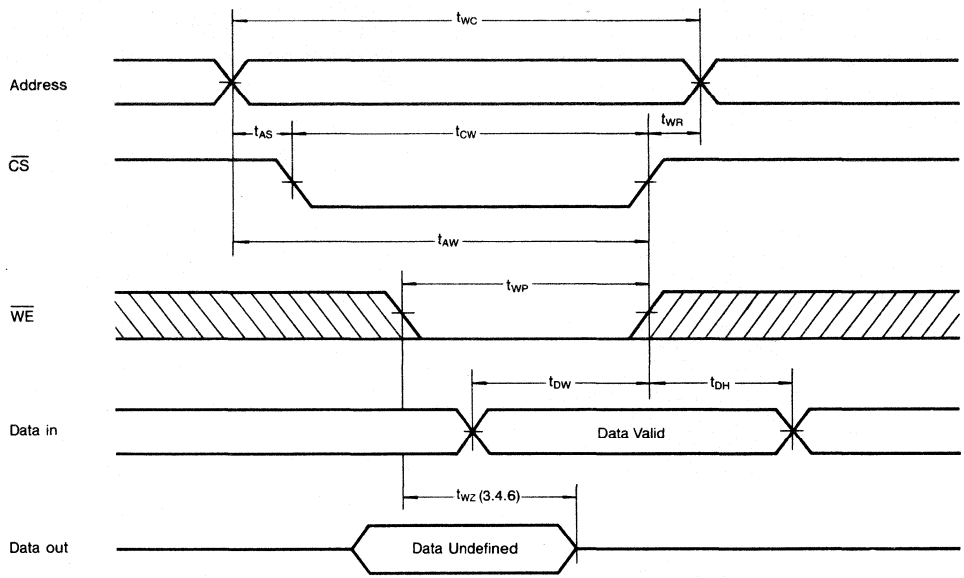
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Device is continuously selected with $\overline{CS}$=V_{IL}.
6. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.
6. When $\overline{CS}$ is low, I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note: X means Don't Care

262,144 WORDx4 Bit High-Speed CMOS Static RAM

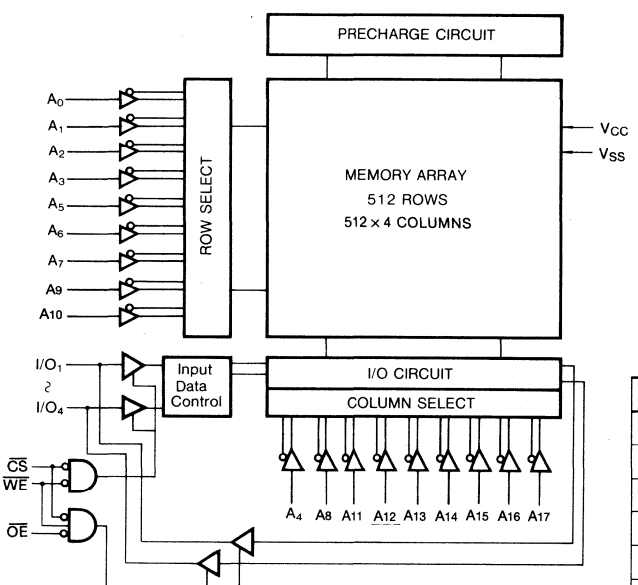
FEATURES

- **Fast Access Time : 12, 15, 17, 20ns(Max.)**
- **Low Power Dissipation**
  Standby (TTL) : 20mA(Max.)
  (CMOS) : 3mA(Max.)
  Operating KM641003A-12 : 185mA(Max.)
  KM641003A-15 : 165mA(Max.)
  KM641003A-17 : 145mA(Max.)
  KM641003A-20 : 125mA(Max.)
- **Single 5V±10% power supply**
- **TTL compatible inputs and outputs**
- **I/O compatible with 3.3V Device**
- **Fully Static Operation**
  - No clock or refresh required
- **Three state Output**
- **Center Power / Ground Pin configuration**
- **Standard Pin Configuration**
  - KM641003AJ : 32-SOJ-400
  - KM641003AT : 32-TSOP(II)-400F

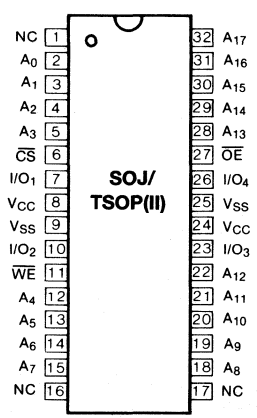
GENERAL DESCRIPTION

The KM641003A is a 1,048,576-bit high-speed Static Random Access Memory organization as 262,144 words by 4-bits.
The KM641003A uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system application.
The KM641003A is packaged in a 400mil 32-pin plastic SOJ and TSOP(II).

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A17	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1~I/O4	Data Inputs/Outputs
VCC	Power(+5V)
VSS	Ground
NC	No Connection

128KX8 Bit High-Speed Static RAM

FEATURES

- **Fast Access Time 20,25,35ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 40mA (max.)**
  - **(CMOS) : 2mA (max.)**
  - **Operating KM681001-20 : 170mA(max.)**
  - **KM681001-25 : 150mA(max.)**
  - **KM681001-35 : 130mA(max.)**
- **Single 5V±10% Power Supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **-No clock or refresh required**
- **Three state Output**
- **Standard Pin Configuration**
  - **KM681001P : 32-DIP-400**
  - **KM681001J : 32-SOJ-400**

GENERAL DESCRIPTION

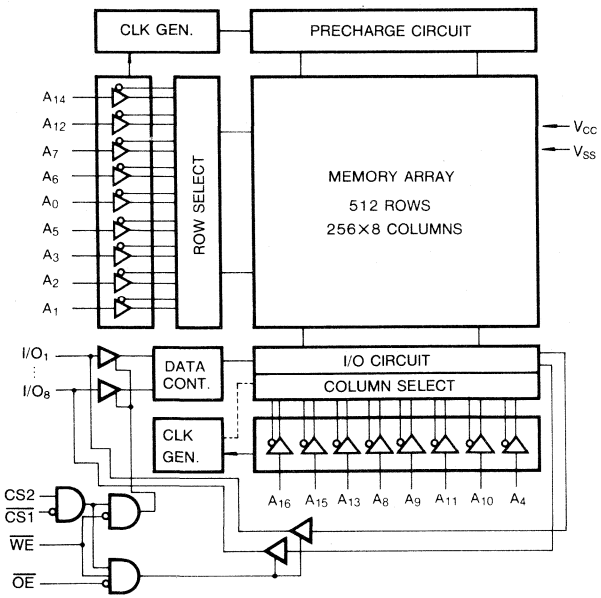
The KM681001 is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits.

The KM681001 uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

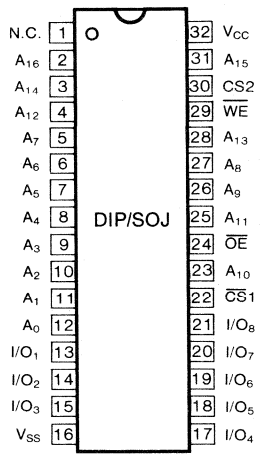
The KM681001 is packaged in a 400mil 32-pin plastic DIP or SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Pin Name	Pin Function
A0-A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS_1}$, CS_2	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	Pd	1.0	W
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature	T_a	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL}(min.)=−3.0V for≤10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}			2	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} or V_{OUT}=V_{SS} to V_{CC}			2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty	20ns		170	mA
		$\overline{CS1}$=V_{IL}, CS2=V_{IH}	25ns		150	mA
		$I_{I/O}$=0mA	35ns		130	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} Min Cycle.			40	mA
	I_{SB1}	$\overline{CS1}$≥V_{CC}-0.2V, CS2≥V_{CC}-0.2V or CS2≤0.2V V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V			2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA			0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE* (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	7	pF

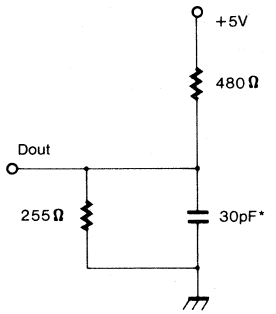
*Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

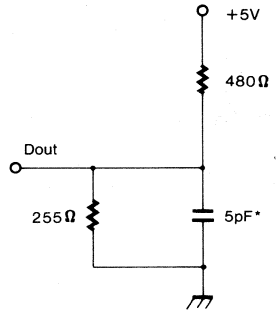
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{OLZ}, t_{OHZ}, t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



*Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20		25		35		ns
Address Access Time	t_{AA}		20		25		35	ns
Chip Select to Output	t_{CO1}, t_{CO2}		20		25		35	ns
Output Enable to Output	t_{OE}		10		13		15	ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Enable to Low-Z Output	t_{LZ1}, t_{LZ2}	0		0		0		ns
Output Disable to High-Z Output	t_{OHZ}	0	8	0	10	0	15	
Chip Disable to High-Z Output	t_{HZ1}, t_{HZ2}	0	12	0	15	0	15	ns
Output Hold from Address Change	t_{OH}	3		5		5		ns

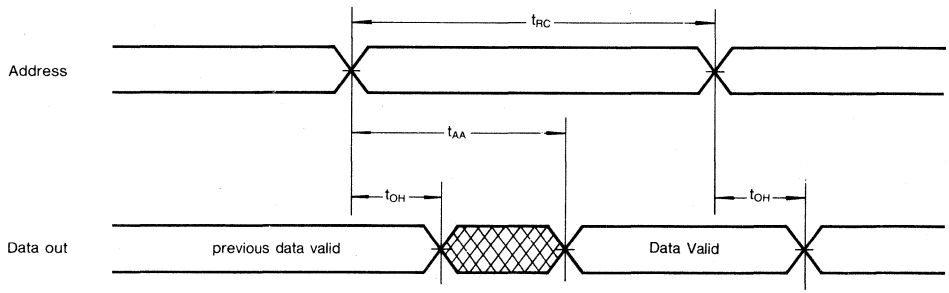
WRITE CYCLE

Parameter	Symbol	-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	20		25		35		ns
Chip Select to End of Write	t_{CW}	17		20		30		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	17		20		30		ns
Write Pluse Width	t_{WP}	15		20		25		ns
Write Recovery Time	t_{WR}	2		3		3		ns
Write to Output High-Z	t_{WZ}	0	8	0	10	0	12	ns
Data to Write Time Overlap	t_{DW}	12		15		20		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		ns

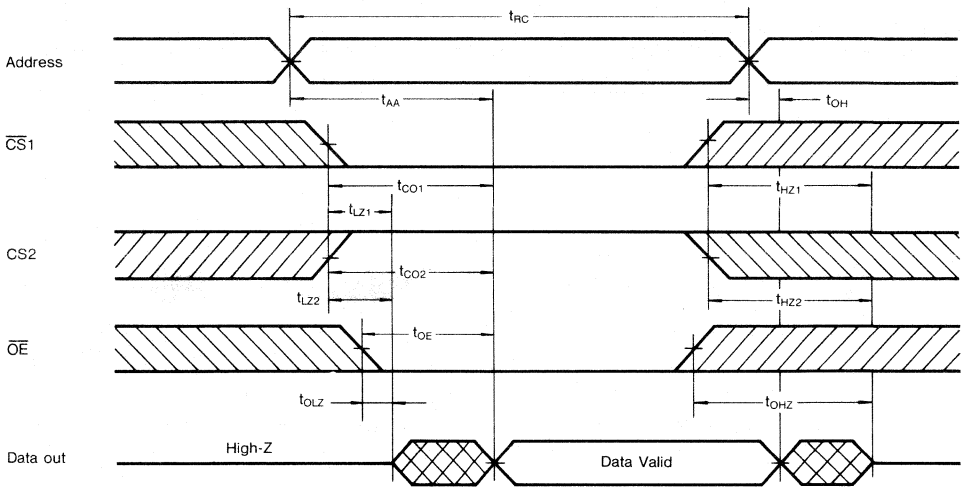
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS1}$=$\overline{OE}$=V_{IL}, CS2=V_{IH}, $\overline{WE}$=V_{IH})



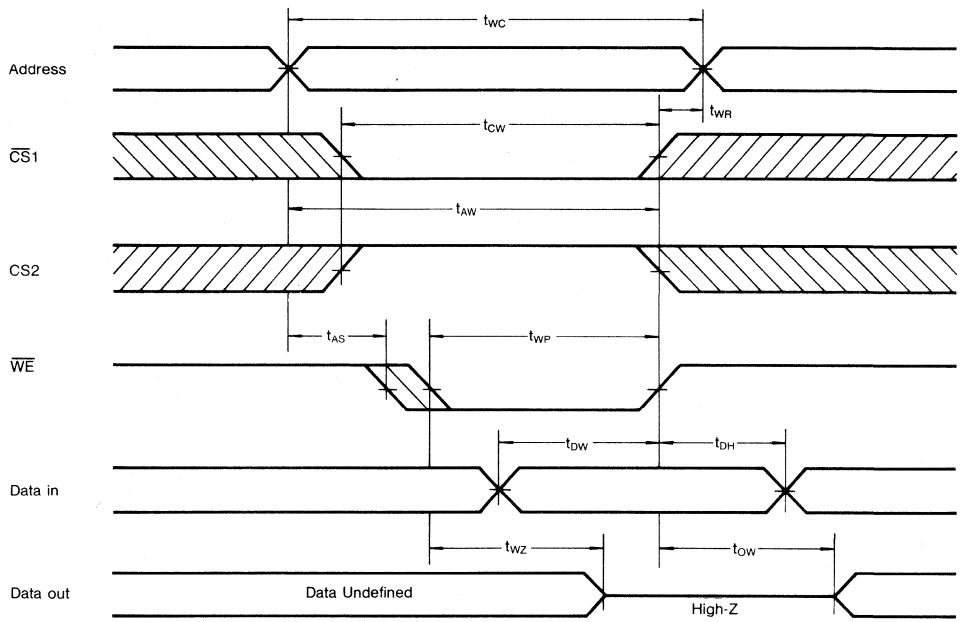
TIMING WAVEFORM OF READ CYCLE



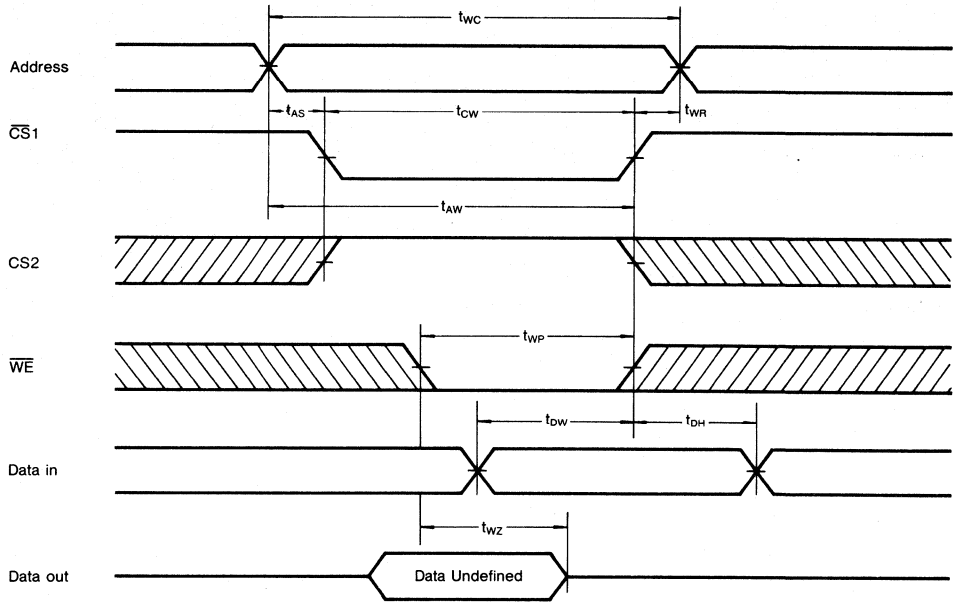
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
3. At any given temperature and voltage condition, t_{HZ}(max) is less than t_{LZ}(min).

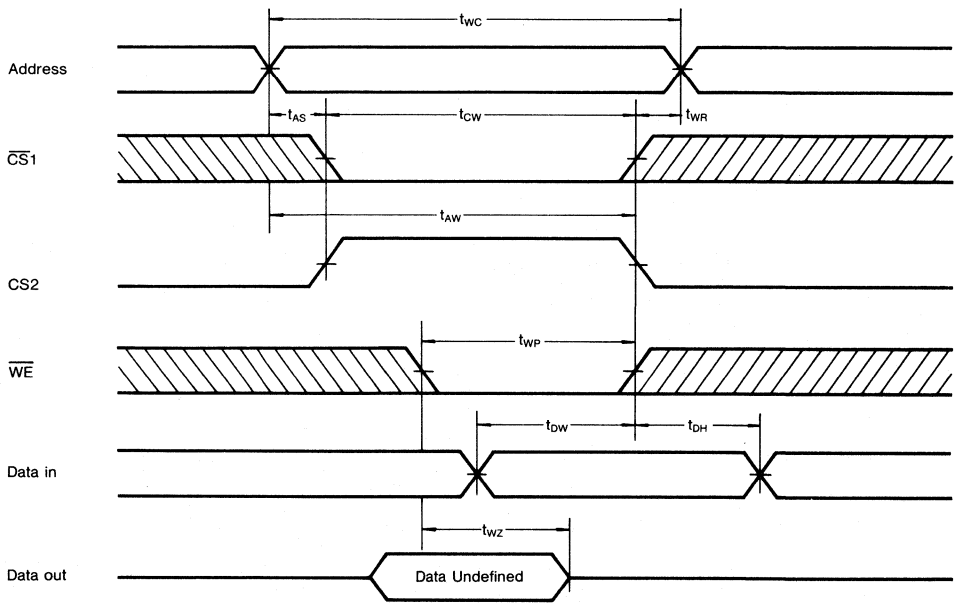
TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$1 Controlled)



TIMING WAVEFORM OF WRITE CYCLE (CS2 Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and WE going low: A write ends at the earlist transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
5. If $\overline{OE}$, $\overline{CS1}$, CS2 and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
7. D_{OUT} is the read data of the new address.
8. When $\overline{CS1}$ is low and CS2 is high: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

2

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

131,072 WORD x 8 Bit High-Speed CMOS Static RAM

FEATURES

- **Fast Access Time: 15, 17, 20ns (Max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 40mA (Max.)**
  - **(CMOS): 10mA (Max.)**
  - **Operating : KM681002-15: 170mA (Max.)**
  - **KM681002-17: 160mA (Max.)**
  - **KM681002-20: 150mA (Max.)**
- **Single 5V ± 10% Power Supply**
- **TTL compatible inputs and outputs**
- **I/O compatible with 3.3V Device**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three state Output**
- **Center Power/Ground Pin Configuration**
- **Standard Pin Configuration**
  KM681002J : 32-SOJ-400

GENERAL DESCRIPTION

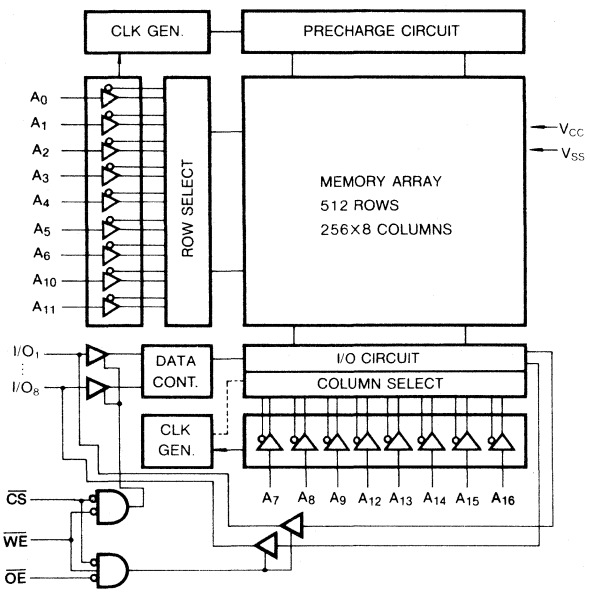
The KM681002 is a 1,048,576-bit high-speed static random access memory organized as 131,072 words by 8 bits.

The KM681002 uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

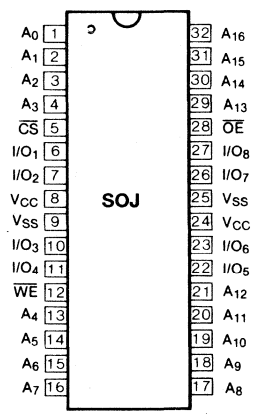
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM681002 is packaged in a 400mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Pin Names	Pin Function
A_0-A_{16}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$I/O_1 \sim I/O_8$	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	Pd	1.0	W
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature	T_a	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL}(min.)=−3.0V for≤10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-2	+2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=V_{SS} to V_{CC}		-2	+2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	15ns	-	170	mA
			17ns	-	160	
			20ns	-	150	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, V_{IN}=V_{IH}/V_{IL}, Min Cycle.		-	40	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V f= oMHz V_{IN}≥Vcc-0.2 or V_{IN}≤0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4.0mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	V

Note : *Temp=25° C , Vcc=5V±5%

CAPACITANCE (f = 1MHz, T_A = 25°C)*

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	8	pF

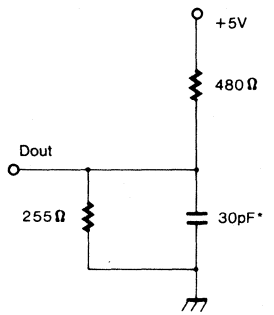
*Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

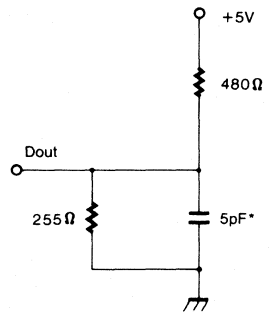
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{OLZ}, t_{OHZ}, t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



*Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	-15		-17		-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		ns
Address Access Time	t_{AA}		15		17		20	ns
Chip Select to Output	t_{CO}		15		17		20	ns
Output Enable to OUtput	t_{OE}		8		9		10	ns
Output Enable to Low-Z OUtput	t_{OLZ}	0		0		0		ns
Chip Enable to Low-Z Output	t_{LZ}	3		3		3		ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	8	ns
Output Hold from Address Change	t_{OH}	3		3		4		ns
Chip Select to Power Up Time	t_{PU}	0		0		0		ns
Chip Select to Power Down Time	t_{PD}		15		17		20	ns

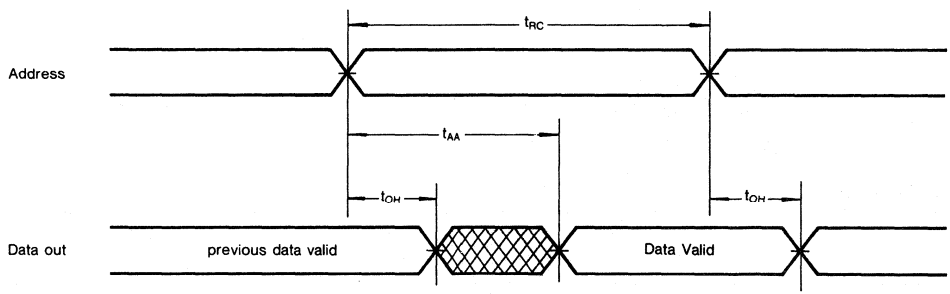
WRITE CYCLE

Parameter	Symbol	-15		-17		-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		ns
Chip Select to End of Write	t_{CW}	12		12		20		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	12		12		13		ns
Write Pulse Width	t_{WP}	12		12		13		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	8	0	8	0	10	ns
Data to Write Time Overlap	t_{DW}	8		9		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End of Write to Output Low-Z	t_{OW}	3		4		5		ns

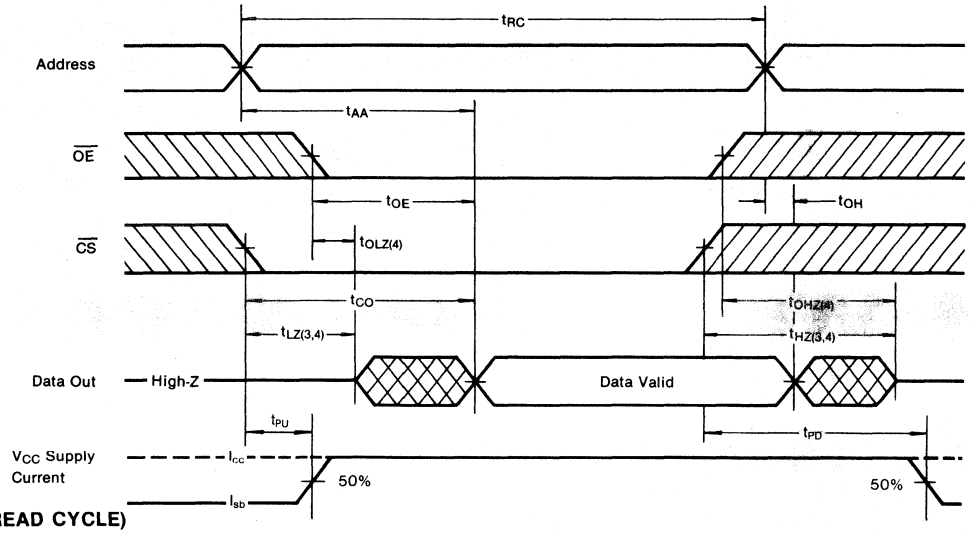
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



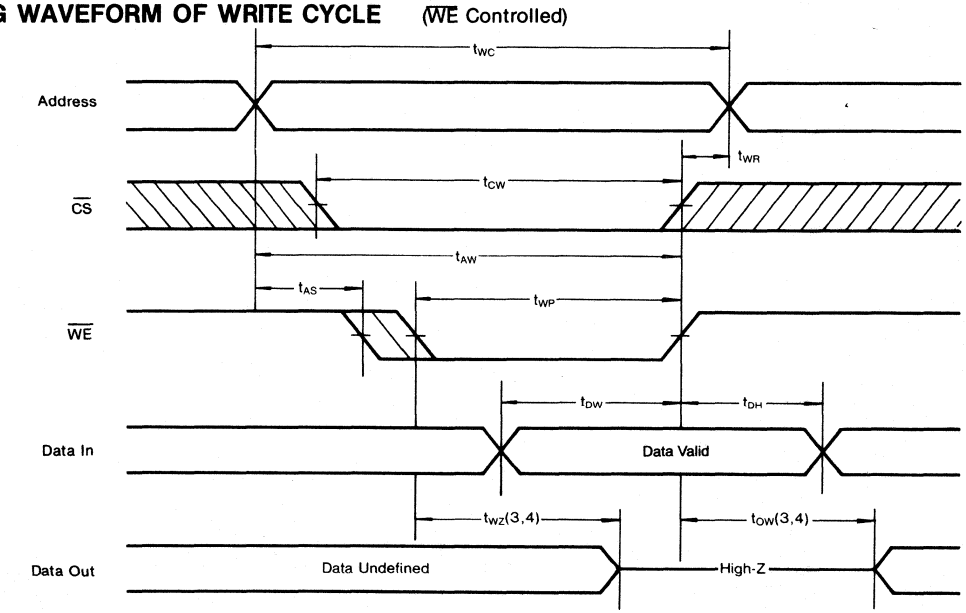
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



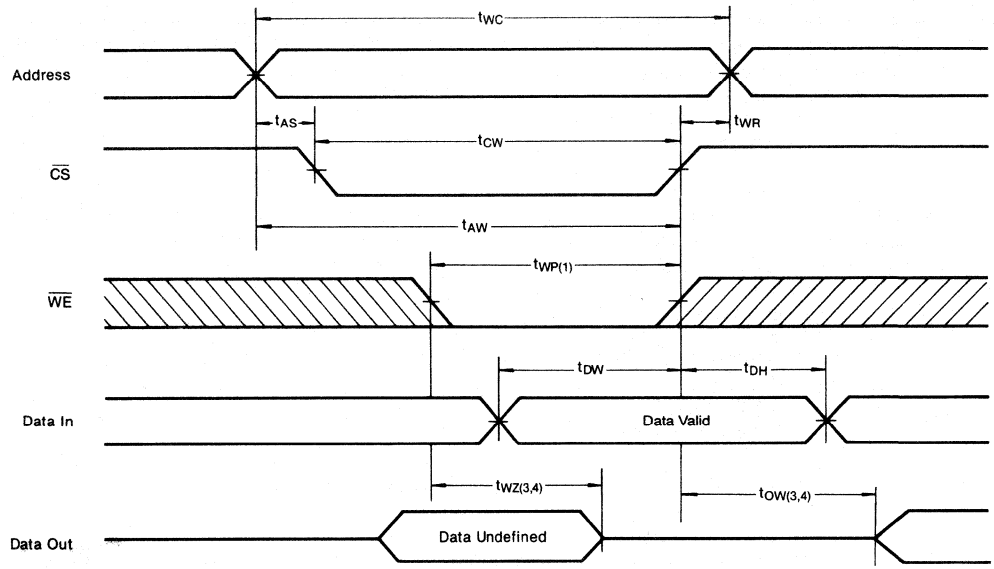
Notes (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Device is continuously selected with $\overline{CS}$=V_{IL}.
6. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltate with Load (B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ} (max.) is less than t_{OW} (min.) both for a given device and from device to device.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.
6. When $\overline{CS}$ is low; I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note: X means Don't Care.

131,072 WORDx8 Bit High-Speed CMOS Static RAM

FEATURES

- **Fast Access Time : 12, 15, 17, 20ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 20mA (max.)**
  - **(CMOS) : 3mA (max.)**
  - **Operating : KM681002A-12 : 185mA (max.)**
  - **KM681002A-15 : 165mA (max.)**
  - **KM681002A-17 : 145mA (max.)**
  - **KM681002A-20 : 125mA (max.)**
- **Single 5V±10% power supply**
- **I/O compatible with 3.3V device**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three State Output**
- **Center Power/Ground Pin Configuration**
- **Standard Pin Configuration**
  - **KM681002AJ : 32-SOJ-400**
  - **KM681002AT : 32-TSOP(II)-400F**

GENERAL DESCRIPTION

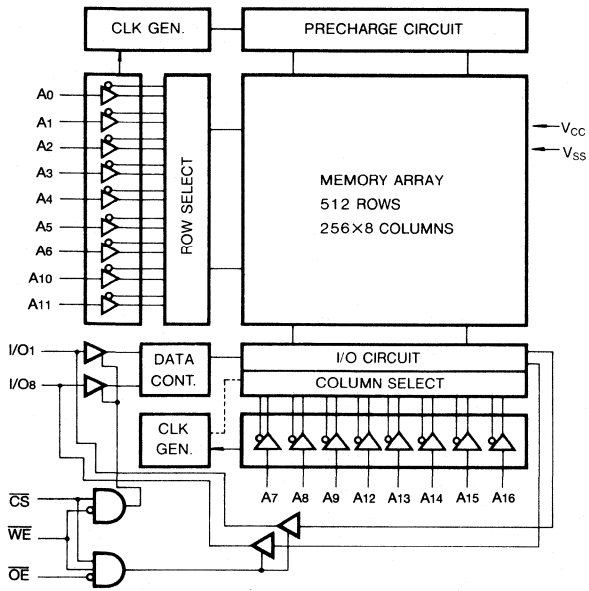
The KM681002A is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits.

The KM681002A uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

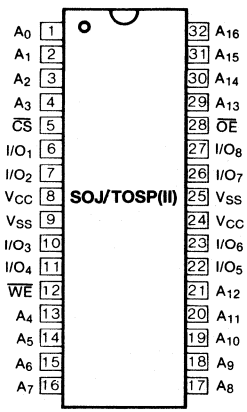
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM681002A is packaged in a 400mil 32-pin plastic SOJ and TSOP(II)

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O8	Data Inputs/Outputs
VCC	Power(+3.3V)
VSS	Ground

65,536 WORD × 16 Bit High-Speed CMOS Static RAM

FEATURES

- **Fast Access Time: 15, 17, 20ns (Max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 40mA (Max.)**
  - **(CMOS) : 10mA (Max.)**
  - **Operating : KM6161002-15 : 230mA (Max.)**
  - **KM6161002-17 : 220mA (Max.)**
  - **KM6161002-20 : 210mA (Max.)**
- **Single 5V ± 10% Power Supply**
- **TTL compatible inputs and outputs**
- **I/O Compatible with 3.3V Device**
- **Fully Static Operation**
  - **— No clock or refresh required**
- **Three State Outputs**
- **Battery Back-up Control : $\overline{LB}$: I/O1 ~ I/O8**
  $\overline{UB}$: I/O9 ~ I/O16
- **Standard Pin Configuration**
  KM6161002J : 44-SOJ-400

GENERAL DESCRIPTION

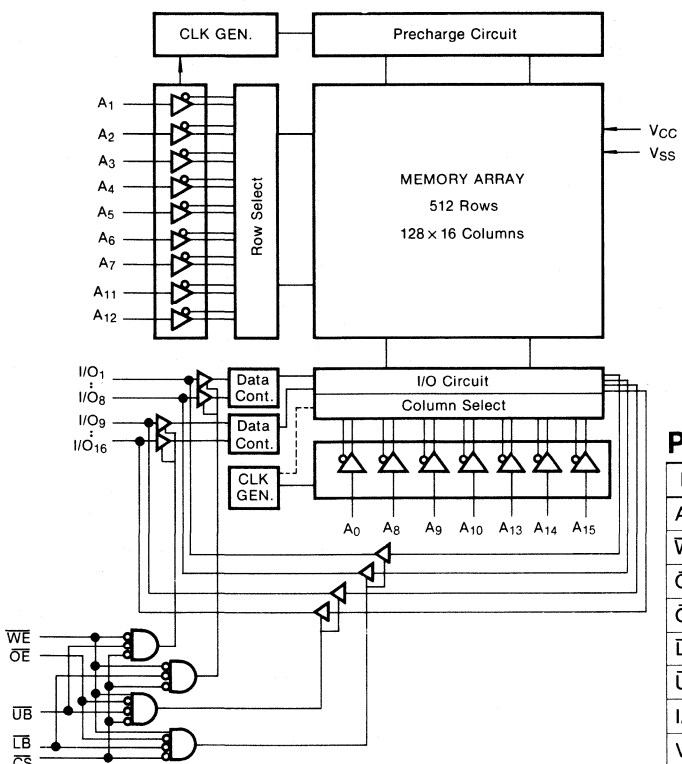
The KM6161002 is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits.

The KM6161002 uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{LB}$, $\overline{UB}$).

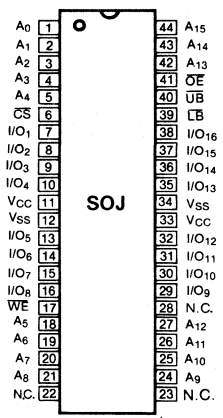
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM6161002 is packaged in a 400 mil 44-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



PIN NAMES

Pin Name	Pin Function
A_0-A_{15}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control (I/O1 ~ I/O8)
$\overline{UB}$	Upper-byte Control (I/O9 ~ I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	Pd	1.5	W
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature	T_a	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL}(min.)=−3.0V for≤10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CC}		-	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to V_{CC}		-	2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	15ns	-	230	mA
			17ns	-	220	mA
			20ns	-	210	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, V_{IN}=V_{IH}/V_{IL}, Min Cycle.		-	40	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V f=0MHz V_{IN}≥V_{CC}-0.2 or V_{IN}≤0.2V		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4.0mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	V

Note : *Temp=25° C, V_{CC}=5V±5%

CAPACITANCE (f=1Mhz, T_A=25°C)*

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	8	pF

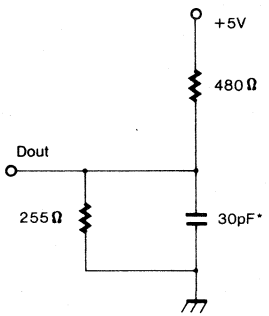
*Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

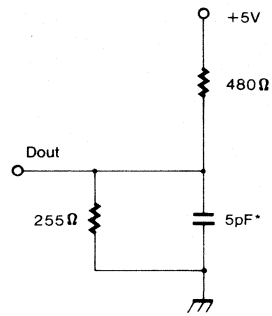
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)

(for t_{OLZ}, t_{OHZ}, t_{HZ}, t_{LZ}, t_{OW}, t_{WZ} t_{BLZ} & t_{BHZ})



*Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	-15		-17		-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		ns
Address Access Time	t_{AA}		15		17		20	ns
Chip Select to Output	t_{CO}		15		17		20	ns
Output Enable to Output	t_{OE}		8		9		10	ns
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}		8		9		10	ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Enable to Low-Z Output	t_{LZ}	3		3		3		ns
$\overline{LB}$, $\overline{UB}$ Enable to Low-Z Output	t_{BLZ}	0		0		0		ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	ns
Chip Disable to High-Z Output	t_{HZ}	0	6	0	7	0	8	ns
$\overline{LB}$, $\overline{UB}$ Disable to High-Z Output	t_{BHZ}	0	6	0	7	0	8	ns
Output Hold from Address Change	t_{OH}	3		3		4		ns

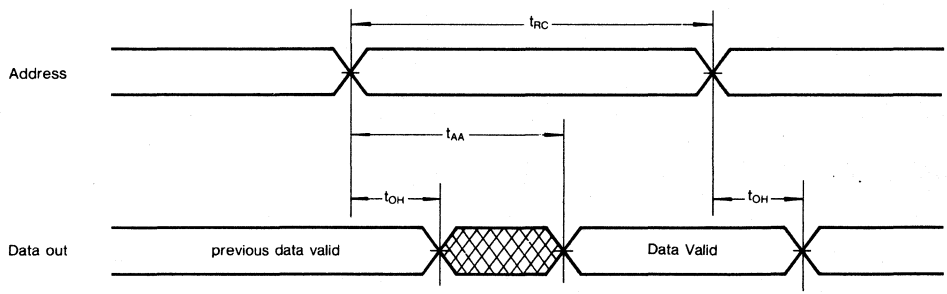
WRITE CYCLE

Parameter	Symbol	-15		-17		-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		ns
Chip Select to End of Write	t_{CW}	12		13		14		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	12		13		14		ns
Write Pulse Width	t_{WP}	12		13		14		ns
$\overline{LB}$, $\overline{UB}$ Valid to End of Write	t_{BW}	12		13		14		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	8	0	8	0	8	ns
Data to Write Time Overlap	t_{DW}	8		9		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	3		4		5		ns

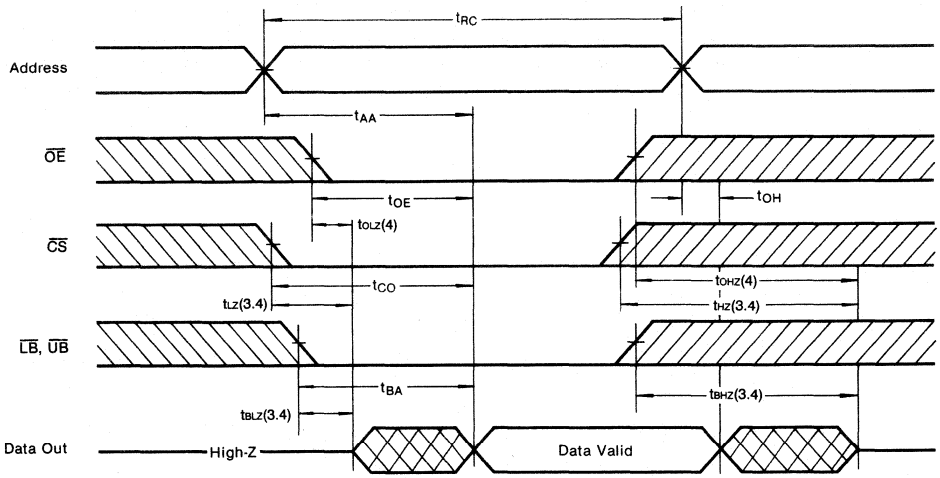
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{UB}$ or $\overline{LB}$=V_{IL})



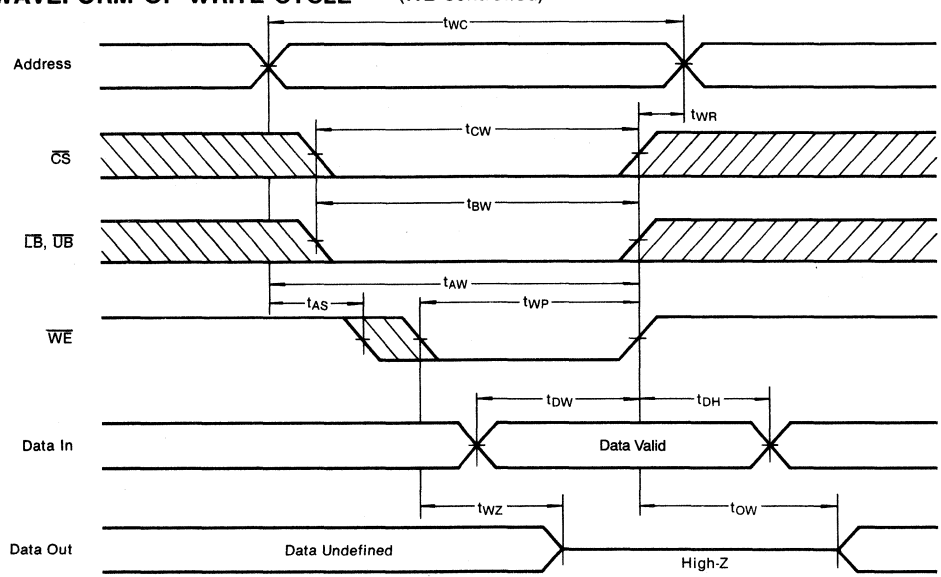
TIMING WAVEFORM OF READ CYCLE



Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
4. Transition is measured ± 200mV from steady state voltage with Load(B). This parameter is sample and not 100% tested.
5. Device is continuously selected with $\overline{CS} = V_{IL}$.
6. Address valid prior to or concident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



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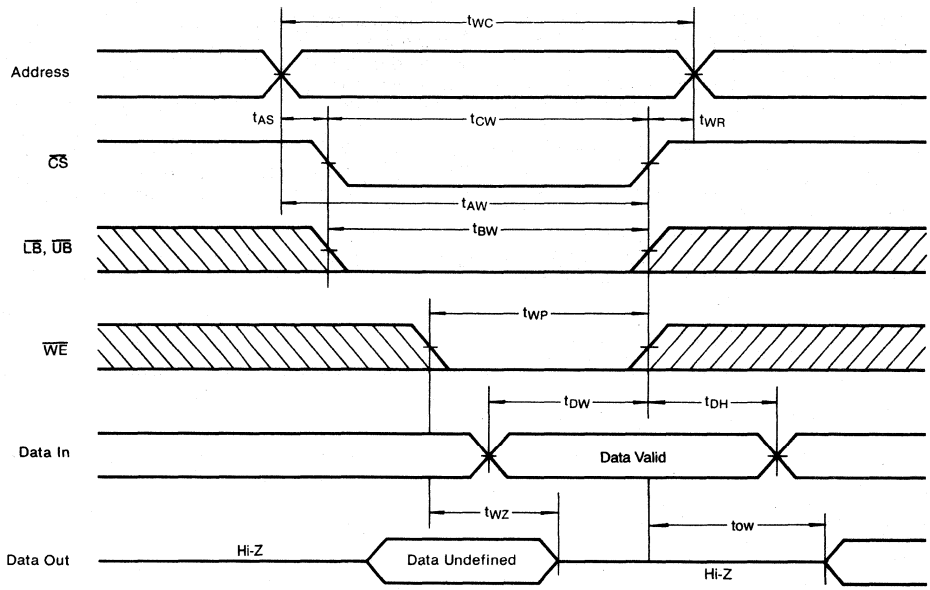
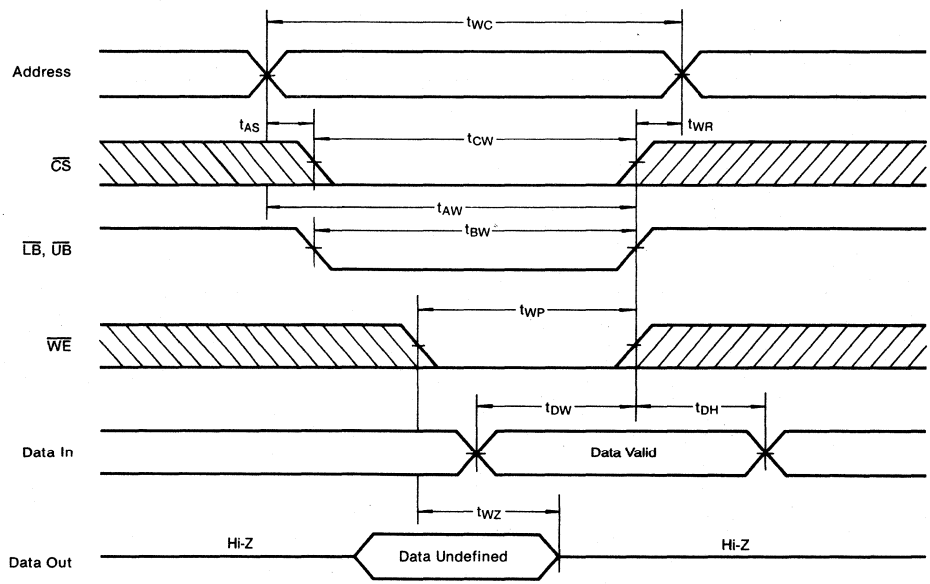
TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{LB}$, $\overline{UB}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
   A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low
   A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high
2. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
5. If $\overline{OE}$, $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
7. D_{OUT} is the read data of the new address.
8. When $\overline{CS}$ is low; I/O pins are in the output state.
   The input signals in the opposite phase leading to the output should not be applied.
9. $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X*	X	X	Not Select	High-Z	High-Z	Isb. Isb1
L	H	H	X	X	Output Disable	High-Z	High-Z	Icc
L	X	X	H	H				
L	H	L	L	H	Read	Dout	High-z	Icc
			H	L		High-z	Dout	
			L	L		Dout	Dout	
L	L	X	L	H	Write	Din	High-Z	Icc
			H	L		High-Z	Din	
			L	L		Din	Din	

*Note: X means Don't Care

65,536 WORDx16 Bit High-Speed CMOS Static RAM

FEATURES

- **Fast Access Time : 12, 15, 17, 20ns (max.)**
- **Low Power Dissipation**
  Standby (TTL) : 30mA (max.)
  (CMOS) : 3mA (max.)
  Operating : KM6161002A-12 : 250mA (max.)
  KM6161002A-15 : 230mA (max.)
  KM6161002A-17 : 220mA (max.)
  KM6161002A-20 : 210mA (max.)
- **Single 5V±10% power supply**
- **I/O tolerence & compatible with 3.3V Device**
- **Fully Static Operation**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - No clock or refresh required
- **Three State Output**
- **Data Byte Control : $\overline{LB}$: I/O1~I/O8**
  $\overline{UB}$: I/O9~I/O16
- **Standard Pin Configuration**
  KM6161002AJ : 44-SOJ-400
  KM6161002AT : 44-TSOP(II)-400F

GENERAL DESCRIPTION

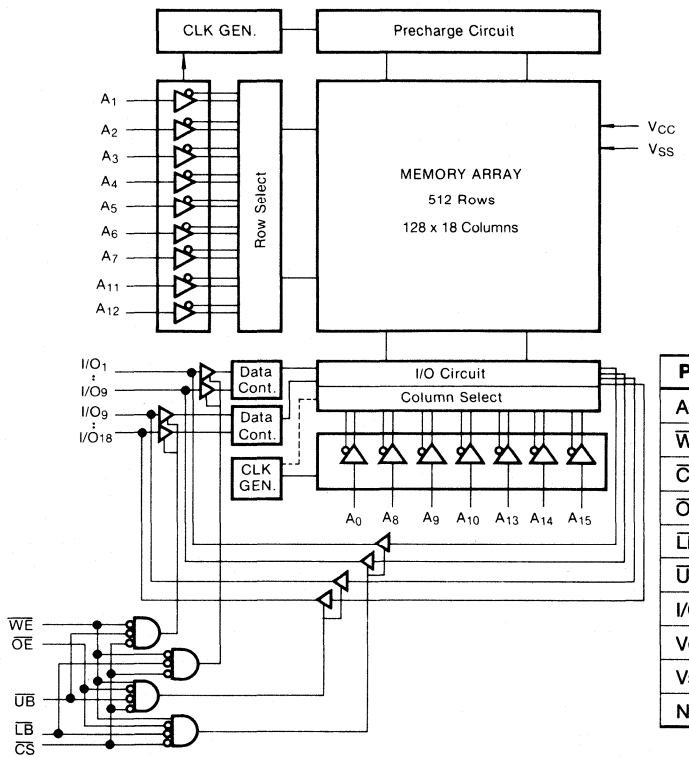
The KM6161002A is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits.

The KM6161002A uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{UB}$, $\overline{LB}$).

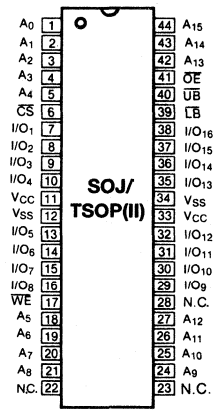
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particulay well suited for use in high-density high-speed system applications.

The KM6161002A is packaged in a 400mil 44-pin plastic SOJ and TSOP(II).

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A15	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1~I/O16	Data Inputs/Outputs
VCC	Power(+5V)
VSS	Ground
NC	No Connection

1,048,576 WORD×4 Bit High-Speed CMOS Static RAM

FEATURES

- **Fast Access Time : 17, 20, 25ns (Max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 60mA (Max.)**
  - **(CMOS) : 10mA (Max.)**
  - **L-Ver : 500μA (Max.)**
  - **Operating : KM644002-17 : 170mA (Max.)**
  - **KM644002-20 : 150mA (Max.)**
  - **KM644002-25 : 130mA (Max.)**
- **Single 5V±10% power supply**
- **Low Data Retention Voltage : 2V (Min.)**
- **TTL compatible inputs and outputs**
- **I/O compatible with 3.3V Device**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three state Output**
- **Standard Pin Configuration**
  - **KM644002J/LJ : 32-SOJ-400**

GENERAL DESCRIPTION

The KM644002/L is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits.

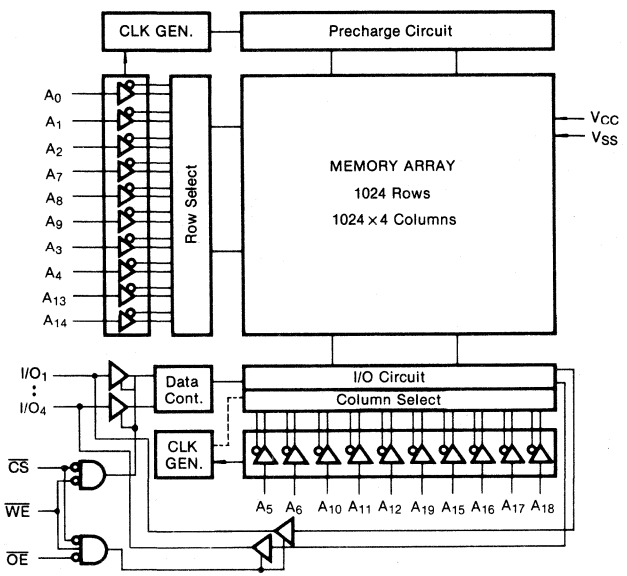
The KM644002/L uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particulay well suited for use in high-density high-speed system applications.

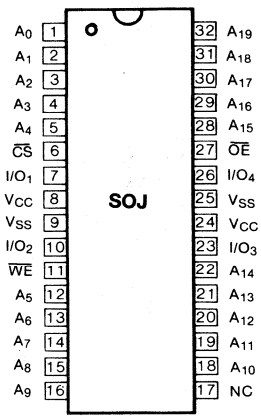
The KM644002/L is packaged in a 400mil 32-pin plastic SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A_0-A_{19}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_4	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL}(min.)= -3.0V for ≤ 10ns pulse.

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-2	+2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}		-2	+2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{out}=0mA	17ns	-	170	mA
			20ns	-	150	mA
			25ns	-	130	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min Cycle.		-	60	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC}-0.2V, f= o		-	10	mA
		V_{IN} ≥ V_{CC}-0.2 or V_{IN} ≤ 0.2V	L-Ver	-	500	μA
Output Low Voltage	V_{OL}	I_{OL}=8mA		2.4	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4mA		-	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	V

*Note : Temp=25° C, V_{CC}=5V±5%

CAPACITANCE* (f=1MHz, T_A=25°C)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	8	pF

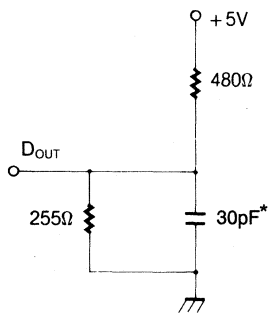
*Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS

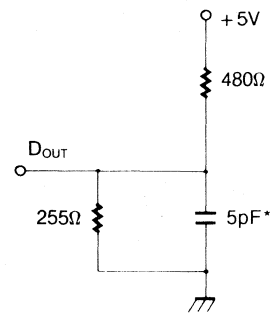
(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

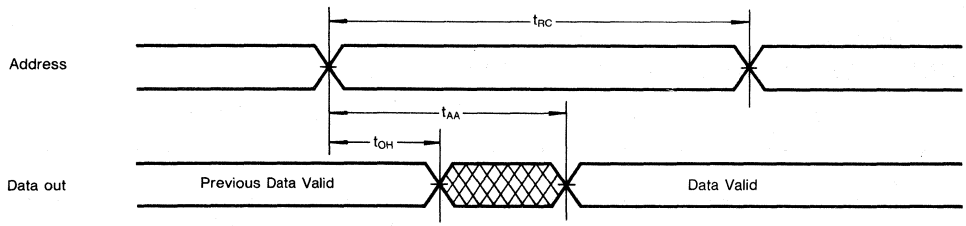
Parameter	Symbol	-17		-20		-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	17		20		25		ns
Address Access Time	t_{AA}		17		20		25	ns
Chip Select to Output	t_{CO}		17		20		25	ns
Output Enable to Valid Output	t_{OE}		8		10		12	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	0	10	ns
Output Disable to High-Z Output	t_{OHZ}	0	7	0	8	0	10	ns
Output Hold from Address Change	t_{OH}	3		4		5		ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		ns
Chip Selection to Power Down Time	t_{PD}		17		20		25	ns

WRITE CYCLE

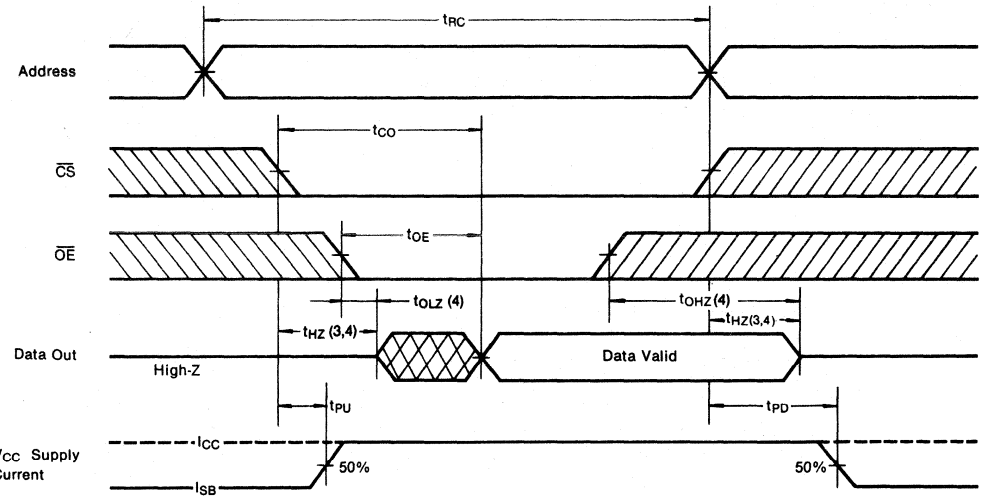
Parameter	Symbol	-17		-20		-25		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	17		20		25		ns
Chip Select to End of Write	t_{CW}	12		13		15		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	12		13		15		ns
Write Pulse Width	t_{WP}	12		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	8	0	8	0	10	ns
Data to Write Time Overlap	t_{DW}	8		9		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End of Write to Output Low-Z	t_{OW}	0		0		0		ns

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



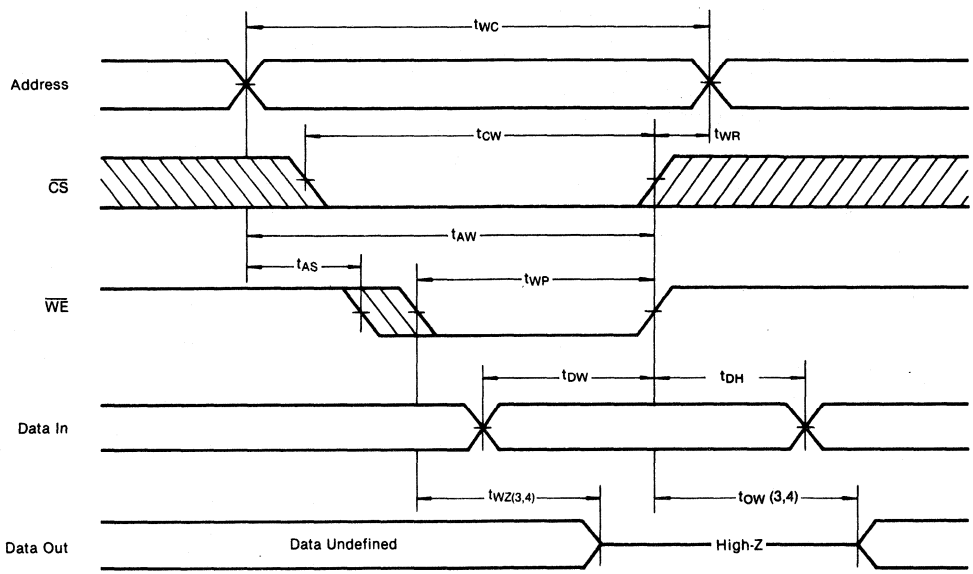
TIMING WAVEFORM OF READ CYCLE



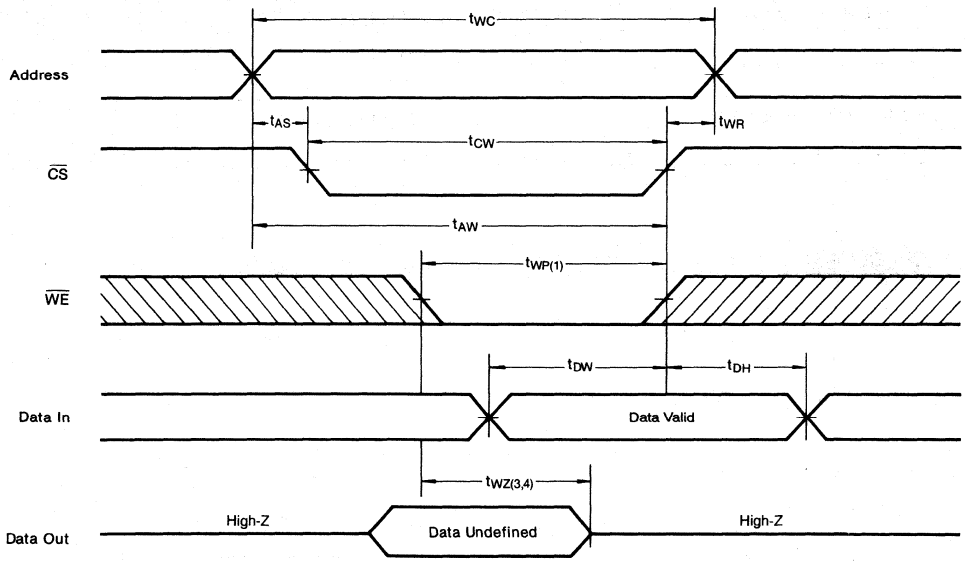
Notes (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltate with Load (B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ} (max.) is less than t_{OW} (min.) both for a given device and from device to device.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.
6. When $\overline{CS}$ is low; I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

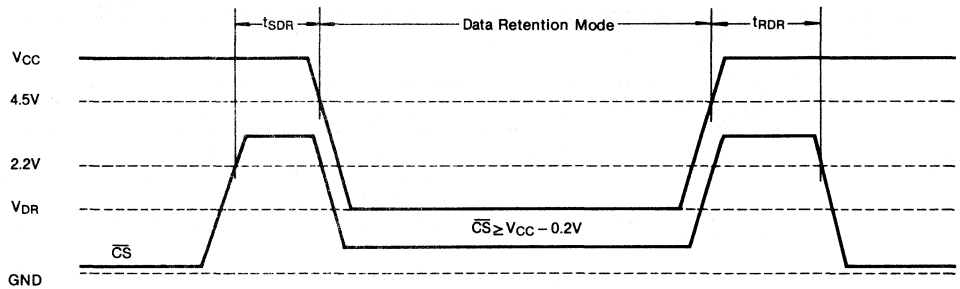
Note: X means Don't Care.

DATA RETENTION CHARACTERISTICS* (T_A=0 to 70°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V	2		5.5	V
Data Retention Current	I_{DR}	$V_{IN} \geq V_{CC}$-0.2V or $V_{IN} \leq 0.2V$, V_{CC}=3V		1	200	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention	0			ns
Recovery Time	t_{RDR}	Wave forms(below)	5			ms

* L-Ver Only

DATA RETENTION WAVEFORM



524,288 WORD x 8 Bit High Speed CMOS Static RAM

FEATURES

- **Fast Access Time : 17, 20, 25ns (Max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 60mA (Max.)**
  - **(CMOS) : 3mA (Max.)**
  - **L-Ver : 500μA (Max)**
  - **Operating : KM684002-17 : 180mA (Max.)**
  - **KM684002-20 : 170mA (Max.)**
  - **KM684002-25 : 160mA (Max.)**
- **Single 5V±10% power supply**
- **Low Data Retention Voltage : 2V(Min.)**
- **TTL compatible inputs and outputs**
- **I/O compatible with 3.3V device**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three State Output**
- **Standard Pin Configuration**
  - **KM684002J/LJ : 36-SOJ-400**

GENERAL DESCRIPTION

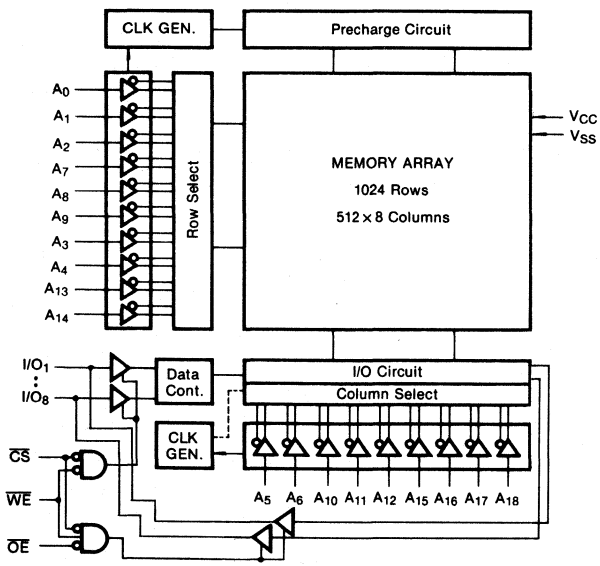
The KM684002/L is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits.

The KM684002/L uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.

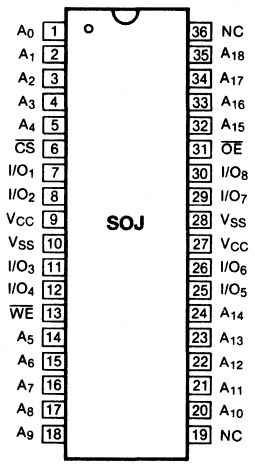
It is particulay well suited for use in high-density high-speed system applications.

The KM684002/L is packaged in a 400mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS (Top View)



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	Pd	1.0	W
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.)=−3.0V for≤10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	+2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=Vss to Vcc		-2	+2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{OUT}=0mA	17ns	-	180	mA
			20ns	-	170	mA
			25ns	-	160	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min Cycle.		-	60	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V f= oMHz		-	10	mA
		V_{IN}≥Vcc-0.2 or V_{IN}≤0.2V	L-Ver	-	500	μA
Output Low Voltage	V_{OL}	I_{OL}=8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4.0mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	V

Note : *Temp=28° C, Vcc=5V±5%

CAPACITANCE* (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	8	pF

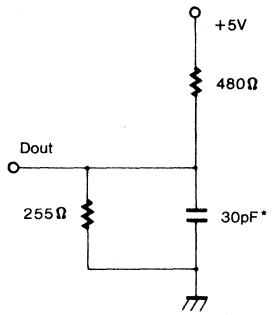
*Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

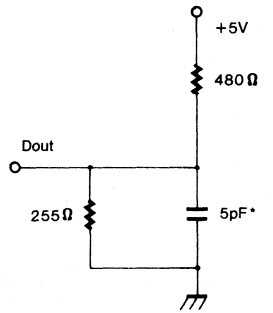
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}, t_{OLZ} & t_{OHZ})



*Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	-17		-20		-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	17		20		25		ns
Address Access Time	t_{AA}		17		20		25	ns
Chip Select to Output	t_{CO}		17		20		25	ns
Output Enable to Valid Output	t_{OE}		8		10		12	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	0	10	ns
Output Disable to High-Z Output	t_{OHZ}	0	7	0	8	0	10	ns
Output Hold from Address Change	t_{OH}	3		4		5		ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		ns
Chip Selection to Power Down Time	t_{PD}		17		20		25	ns

WRITE CYCLE

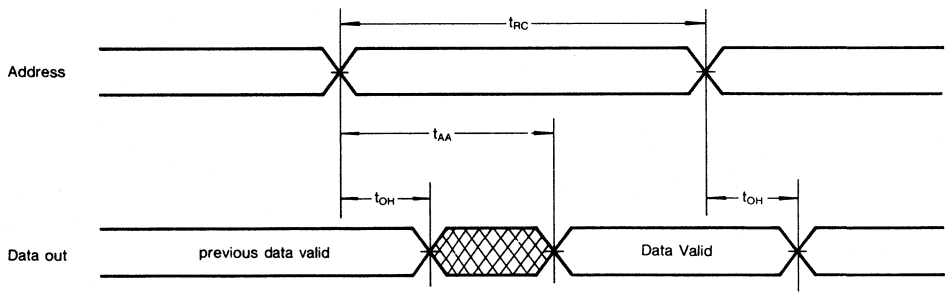
Parameter	Symbol	-17		-20		-25		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	17		20		25		ns
Chip Select to End of Write	t_{CW}	12		13		15		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	12		13		15		ns
Write Pulse Width	t_{WP}	12		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	8	0	8	0	10	ns
Data to Write Time Overlap	t_{DW}	8		9		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		ns

2

TIMING DIAGRAMS

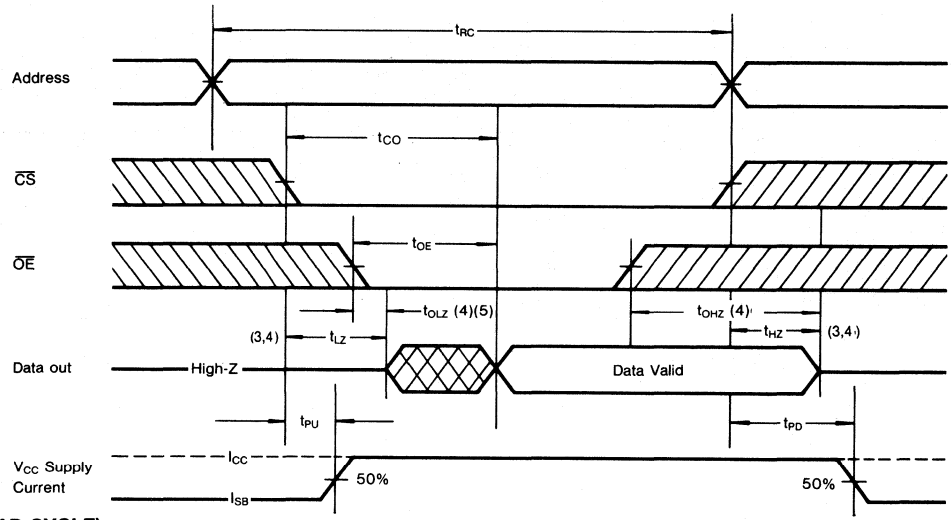
TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



SAMSUNG ELECTRONICS

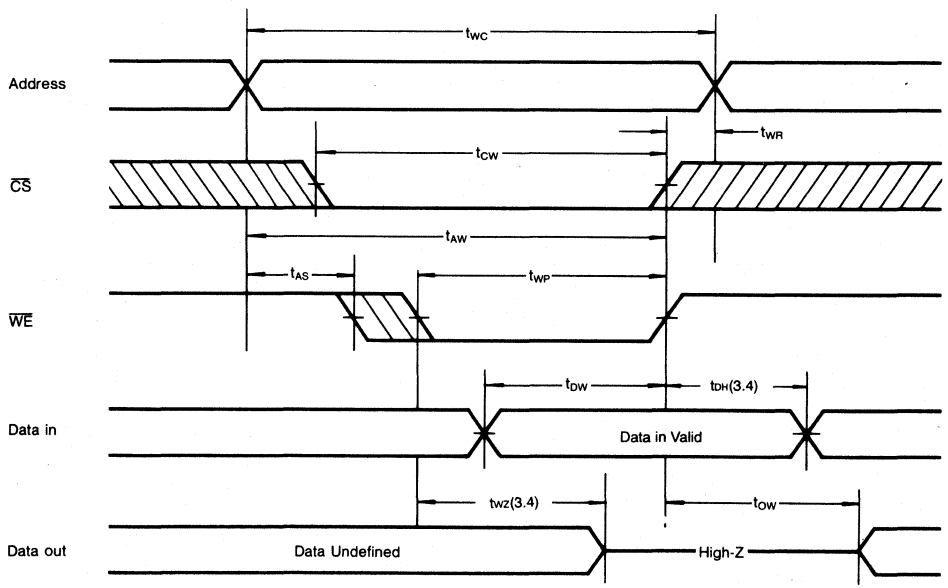
TIMING WAVEFORM OF READ CYCLE



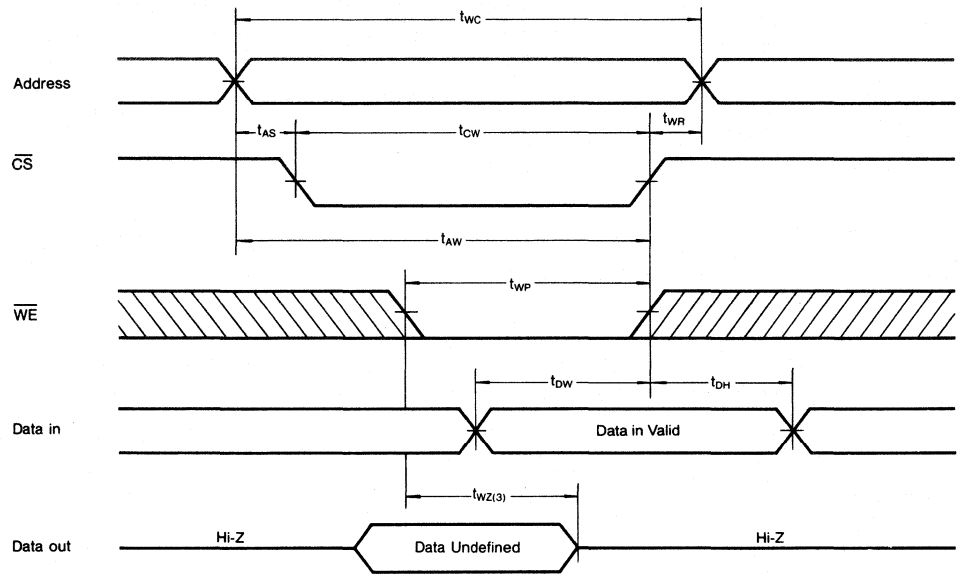
Notes(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ} (max.) is less than t_{OW} (min.) both for a given device and from device to device.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.
6. When $\overline{CS}$ is low; I/O pins are in the output state, the input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

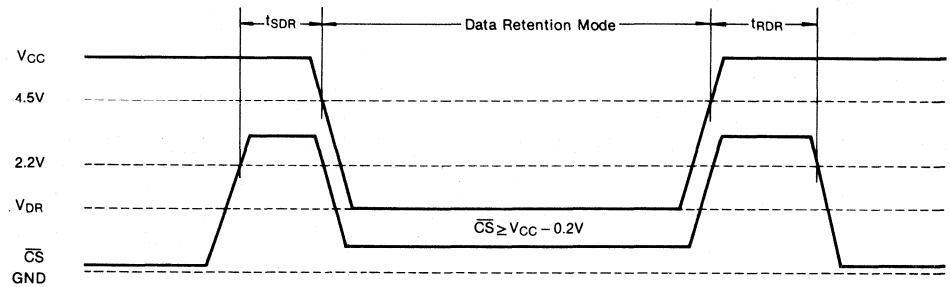
* Note: X means Don't Care

DATA RETENTION CHARACTERISTICS* (T_A=0 to 70°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V,	2		5.5	V
Data Retention Current	I_{DR}	$V_{IN} \geq V_{CC}$-0.2V or $V_{IN} \leq 0.2V$, V_{CC}=3V		1	200	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention	0			ns
Recovery Time	t_{RDR}	Wave forms(below)	5			ms

* L-Ver Only

DATA RETENTION WAVEFORM



262,144 WORD x 16 Bit High Speed CMOS Static RAM

FEATURES

- **Fast Access Time : 20, 25, 35ns (Max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 60mA (Max.)**
  - **(CMOS) : 10mA (Max.)**
  - **L-Ver : 500μA (Max)**
  - **Operating : KM6164002-20 : 250mA (Max.)**
  - **KM6164002-25 : 240mA (Max.)**
  - **KM6164002-35 : 220mA (Max.)**
- **Single 5V±10% power supply**
- **TTL compatible inputs and outputs**
- **I/O Compatible with 3.3V Device**
- **2V Minimum Data Retetion : L-Ver**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three State Output**
- **Data Byte Control : LB : I/O_1~I/O_8**
  UB : I/O_9~I/O_{16}
- **Standard Pin Configuration**
  - **KM684002J/LJ : 44-SOJ-400**

GENERAL DESCRIPTION

The KM6164002/L is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits.

The KM6164002/L uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{UB}$, $\overline{LB}$). The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.

It is particularly well suited for use in high-density high-speed system applications

The KM6164002/L is packaged in a 400mil 44-pin plastic SOJ.

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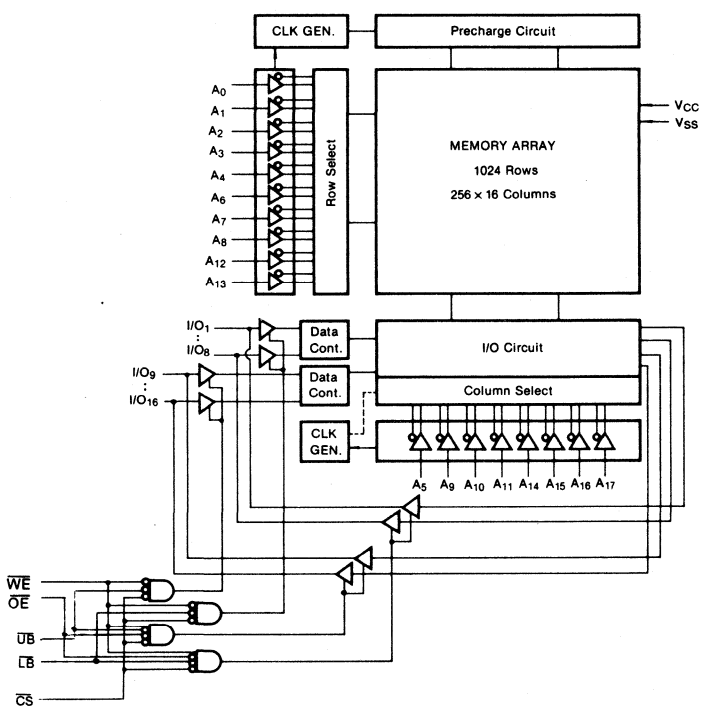
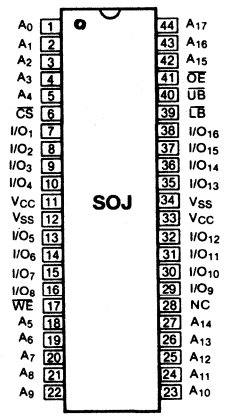
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control (I/O_1 ~ I/O_8)
$\overline{UB}$	Upper-byte Control (I/O_9 ~ I/O_{16})
I/O_1-I/O_{16}	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	Pd	1.5	W
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature	T_a	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.)=−3.0V for≤10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	+2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=Vss to Vcc		-2	+2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{OUT}=0mA	20ns	-	240	mA
			25ns	-	220	mA
			35ns	-	200	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min Cycle.		-	60	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V f= oMHz		-	10	mA
		V_{IN}≥Vcc-0.2 or V_{IN}≤0.2V	L-Ver	-	500	μA
Output Low Voltage	V_{OL}	I_{OL}=8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4.0mA		2.4	-	V
	V_{OH1}	I_{OH1}=-100μA		-	3.95	V

Note : Temp=25° C, Vcc=5V±5%

CAPACITANCE* (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	6	pF
Input/Output Capacitance	C_{OUT}	V_{OUT}=0V	—	8	pF

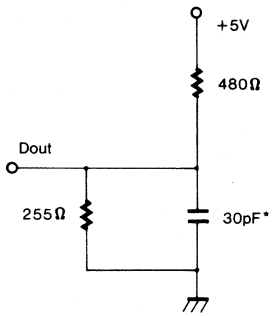
*Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

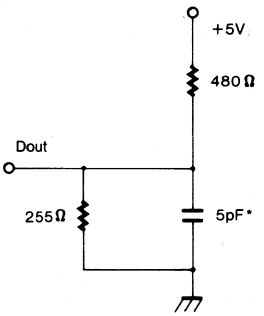
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}, t_{BHZ} & t_{BLZ})



*Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20		25		35		ns
Address Access Time	t_{AA}		20		25		35	ns
Chip Select to Output	t_{CO}		20		25		35	ns
Output Enable to Output	t_{OE}		10		12		15	ns
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}		10		12		15	ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Enable to Low-Z Output	t_{LZ}	5		5		5		ns
$\overline{LB}$, $\overline{UB}$ Enable to Low-Z Output	t_{BLZ}	0		0		0		ns
Output Disable to High-Z Output	t_{OHZ}	0	7	0	8	0	10	ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	0	10	ns
$\overline{LB}$, $\overline{UB}$ Disable to High-Z Output	t_{BHZ}	0	7	0	8	0	10	ns
Output Hold from Address Change	t_{OH}	4		5		5		ns

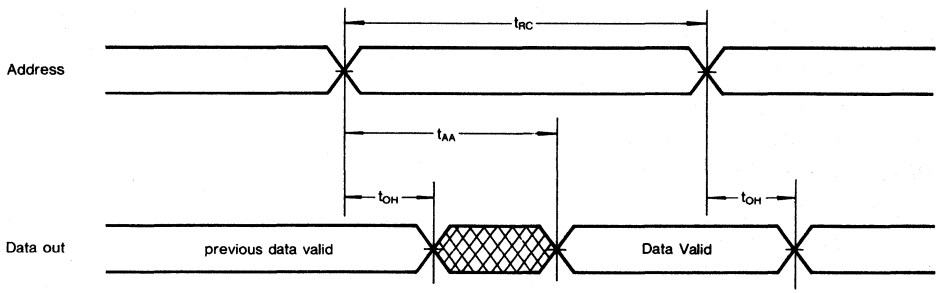
WRITE CYCLE

Parameter	Symbol	-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	20		25		35		ns
Chip Select to End of Write	t_{CW}	15		17		20		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	15		17		20		ns
Write Pulse Width	t_{WP}	15		17		20		ns
$\overline{LB}$, $\overline{UB}$ Valid to End of write	t_{BW}	15		17		20		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	8	0	8	0	8	ns
Data to Write Time Overlap	t_{DW}	10		12		15		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	3		4		4		ns

TIMING DIAGRAMS

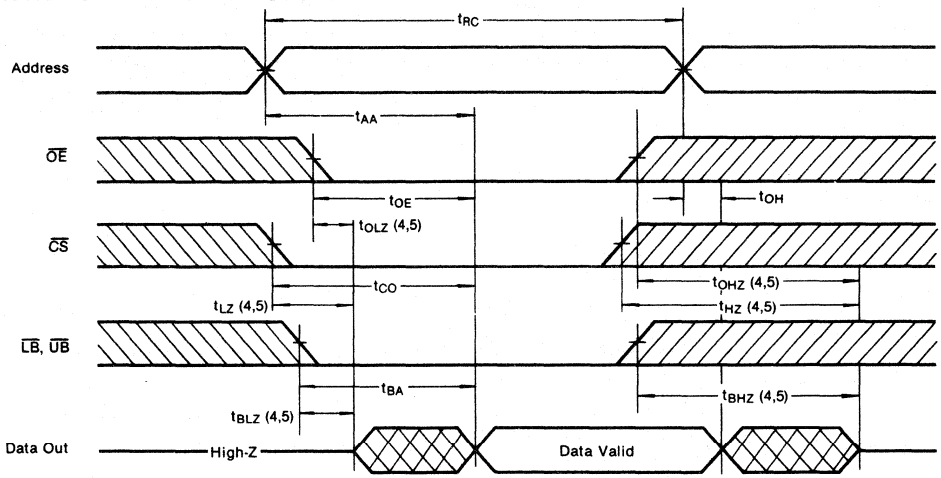
TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$, $\overline{OE}$, $\overline{UB}$ or $\overline{LB} = V_{IL}$, $\overline{WE} = V_{IH}$)



TIMING DIAGRAMS

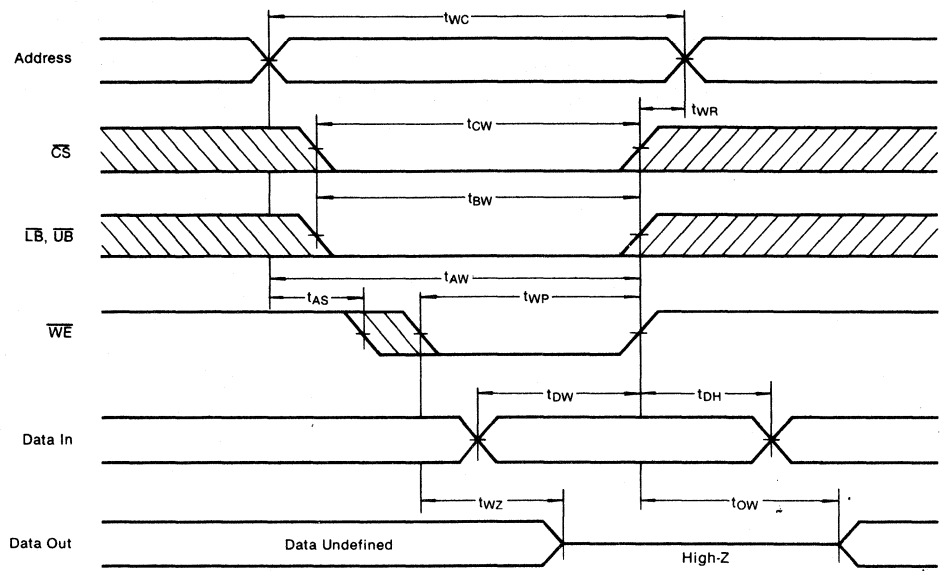
TIMING WAVEFORM OF READ CYCLE



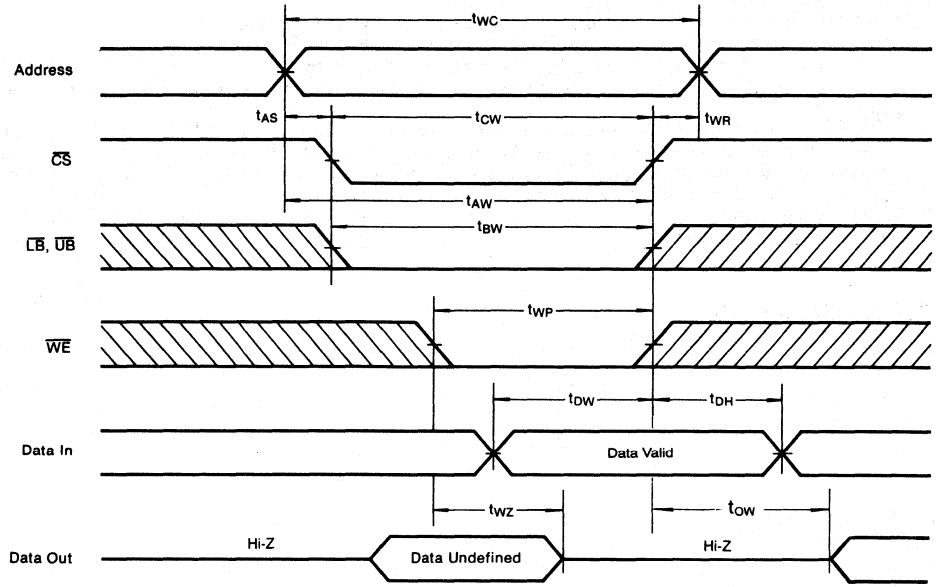
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Device is continuously selected with $\overline{CS} = V_{IL}$.
6. Address valid prior to or coincident with $\overline{CS}$ transition low.

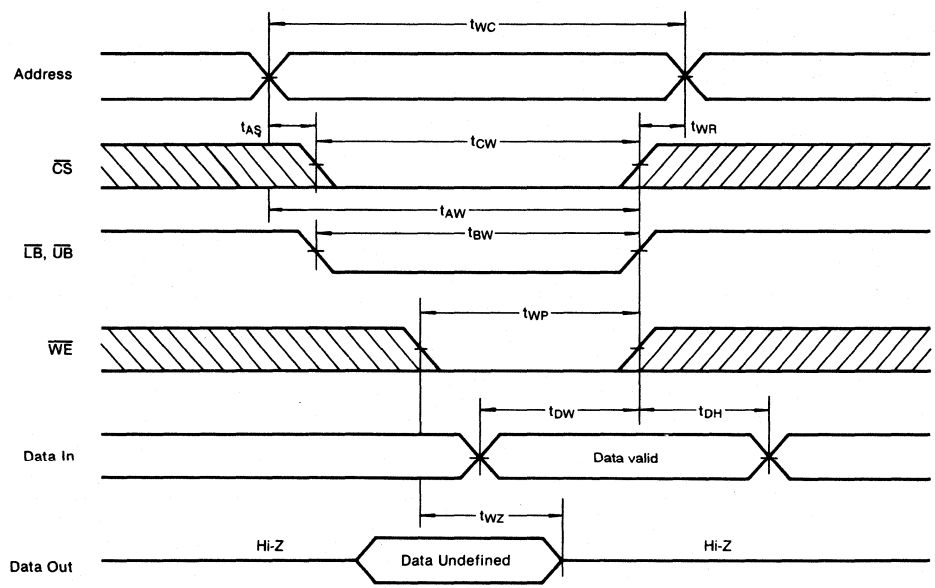
TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{LB}$, $\overline{UB}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
   A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low.
   A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high.
2. t_{AS} is measured from the address valid to the beginning of write.
3. t_{WR} is measured from the end of write to the address change. t_{WR} applies in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
4. If $\overline{OE}$, $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
5. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
6. D_{OUT} is the read data of the new address.
7. When $\overline{CS}$ is low and I/O pins are in the output state, the input signals in the opposite phase leading to the output should not be applied.

2

FUNCTION DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X*	X	X	Not Select	High-Z	High-Z	Isb. Isb1
L	H	H	X	X	Output Disable	High-Z	High-Z	Icc
L	X	X	H	H				
L	H	L	L	H	Read	Dout	High-z	Icc
			H	L		High-z	Dout	
			L	L		Dout	Dout	
L	L	X	L	H	Write	Din	High-Z	Icc
			H	L		High-Z	Din	
			L	L		Din	Din	

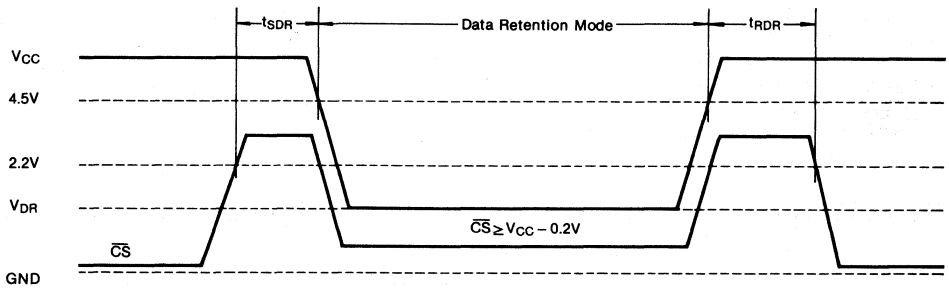
*Note: X means Don't Care

DATA RETENTION CHARACTERISTICS* (T_A=0 to 70°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V	2		5.5	V
Data Retention Current	I_{DR}	$V_{IN} \geq V_{CC}$-0.2V or $V_{IN} \leq 0.2V, V_{CC}$=3V		1	200	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention	0			ns
Recovery Time	t_{RDR}	Wave forms(below)	5			ms

* L-Ver Only

DATA RETENTION WAVEFORM



65,536 WORDx4 Bit High Speed CMOS Static RAM (3.3V Operating)

FEATURES

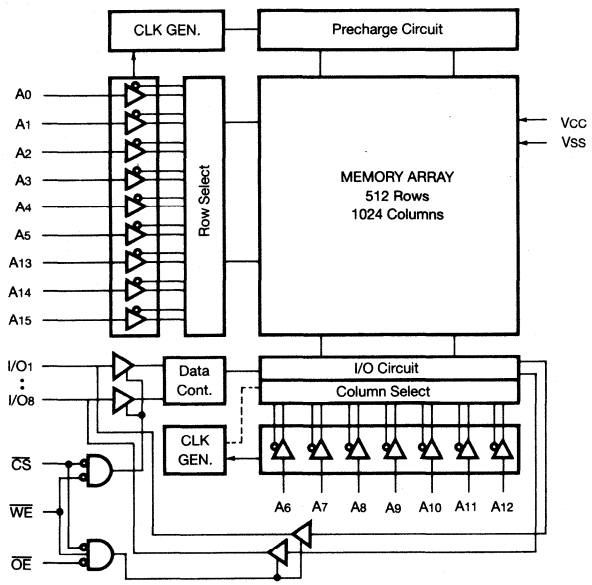
- **Fast Access Time : 20, 25, 35ns(Max.)**
- **Low Power Dissipation**
  Standby (TTL) : 30mA (max)
  (CMOS) : 100μA (max)
  Operating : KM64V258C-15 : 80mA (max)
  KM64V258C-17 : 70mA (max)
  KM64V258C-20 : 60mA (max)
- **Single 3.3V±0.3V power supply**
- **TTL compatible inputs and outputs**
- **2V Minimum Data Retetion**
- **Fully Static Operation**
  - No clock or refresh required
- **Three state Output**
- **Low Data Retention Voltage : 2V(min.)**
- **Standard Pin Configuration**
  - KM64V258CP : 28-DIP-300
  - KM64V258CJ : 28-SOJ-300

GENERAL DESCRIPTION

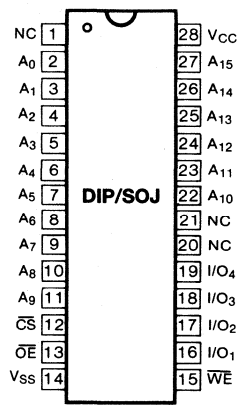
The KM64V258C is a 262,144 bit high-speed Static Random Access Memory organized as 65, 536 words by 4 bits.
The KM64V258C uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.
The KM64V258C is designed to operate at 3.3 volts. It is particularly well suited for use in high-density high-speed system applications.
The KM64V258C is packaged in a 300mil 28-pin plastic DIP or SOJ

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A15	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1~I/O8	Data Inputs / Outputs
VCC	Power (+3.3V)
VSS	Ground

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 5.5	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	-65 to 150	°C
Operating Temperature	T_a	0 to 70	°C

* Stresses greater than those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.3*	—	0.8	V

* V_{IL}(min.)=-2.0V for $\leq$ 10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=3.3V$\pm$0.3V, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	LI_{VIN}=V_{SS} to V_{CC}		-	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IN} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}		-	2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{out}=0mA	15ns	-	80	mA
			17ns	-	70	mA
			20ns	-	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min Cycle.		-	30	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}$-0.2V, f= oMHz $V_{IN}\geq V_{CC}$-0.2 or $V_{IN}\leq$0.2V		-	100	μA
Output Low Voltage	V_{OL}	I_{OL}=8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4.0mA		2.4	-	V

CAPACITANCE (f=1MHz, T_A=25°C)*

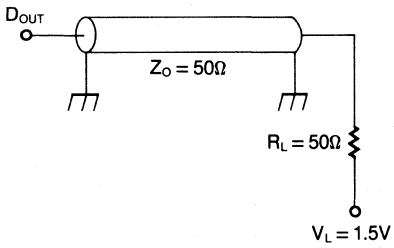
Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note : Capacitance is sampled and not 100% tested.

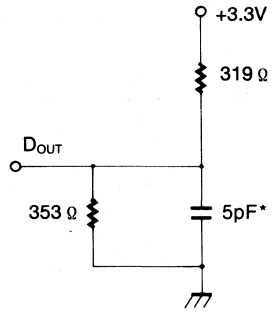
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=3.3V±0.3V, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	-15		-17		-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		ns
Address Access Time	t_{AA}		15		17		20	ns
Chip Select to Output	t_{CO}		15		17		20	ns
Output Enable to Valid Output	t_{OE}		7		8		10	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	0	10	ns
Output Disable to High-Z Output	t_{OHZ}	0	7	0	8	0	10	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Chip selection to Power Up time	t_{PU}	0		0		0		ns
Chip Selection to Power Down Time	t_{PD}		15		17		20	ns

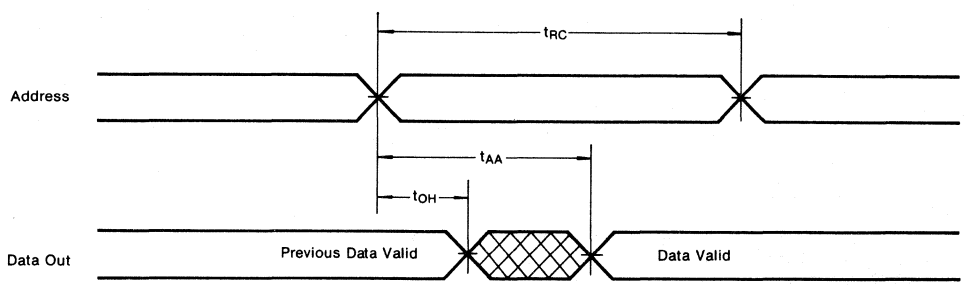
WRITE CYCLE

Parameter	Symbol	-15		-17		-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		ns
Chip Select to End of Write	t_{CW}	11		12		13		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	11		12		13		ns
Write Pulse Width(OE High)	t_{WP}	11		12		13		ns
Write Pulse Width(OE Low)	t_{WP}	15		17		20		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WHZ}	0	6	0	6	0	8	ns
Data to Write Time Overlap	t_{DW}	8		8		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		ns

TIMING DIAGRAMS

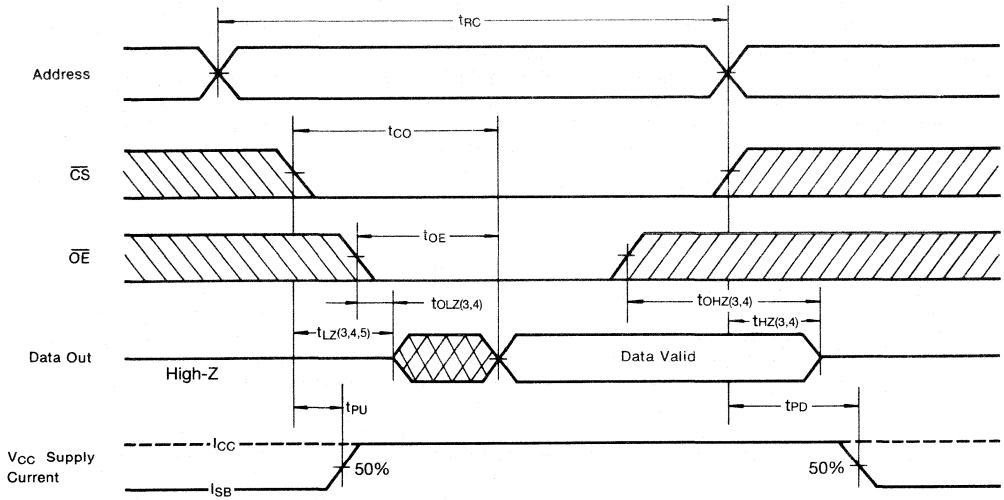
TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



SAMSUNG ELECTRONICS

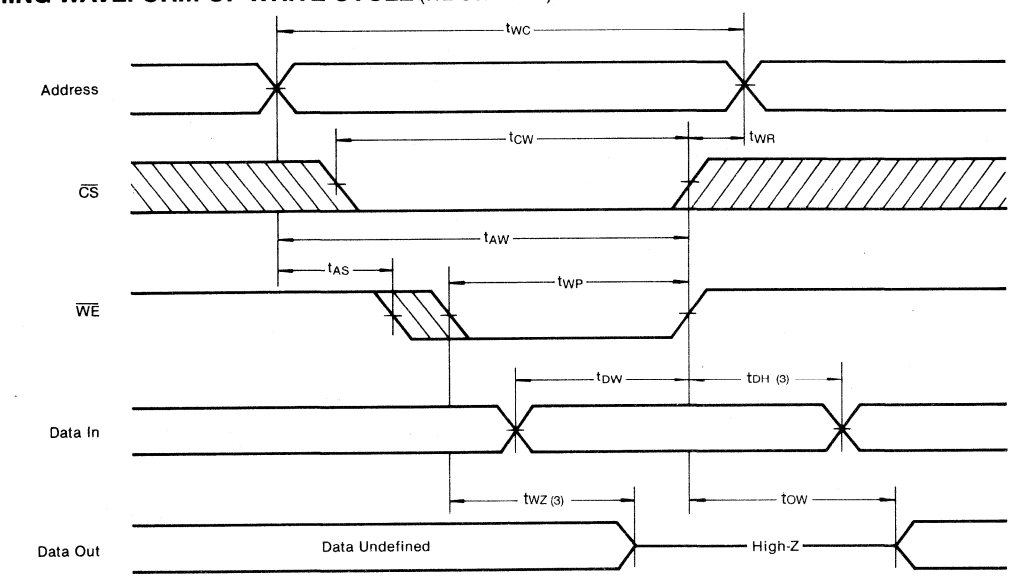
TIMING WAVEFORM OF READ CYCLE



Notes(Read Cycle)

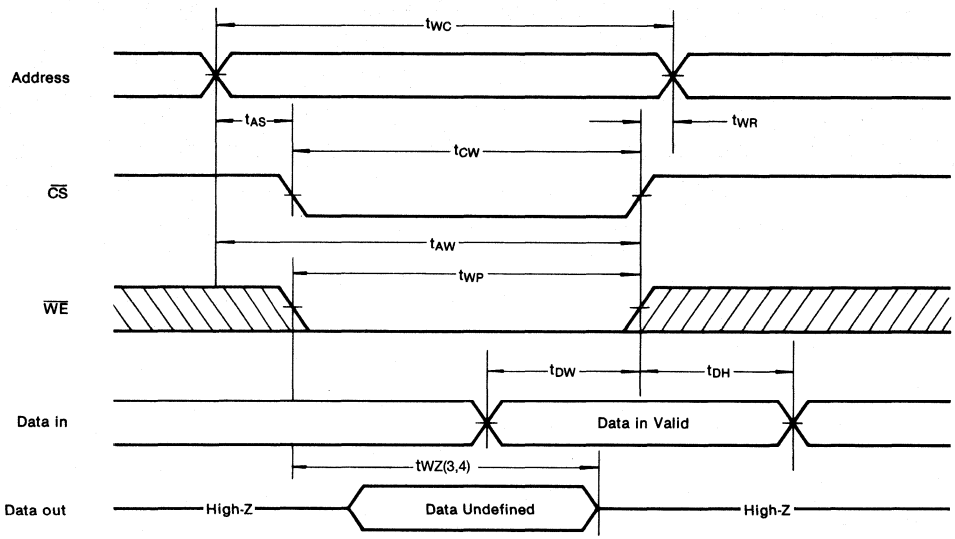
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.)both for a given device and from device to device.
4. Transition is measured ± 200mV from steady state voltage with Load (B) This parameter is sampled and not 100% tested.
5. Address valid prior to or coincident with $\overline{CS}$ transition low.
6. Device is continuously Selected with $\overline{CS}$=V_{IL}.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes(Write Cycle)

1. A write occurs during the overlap(tWP) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B) This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, twz(max.) is less than tOW(min.) both for a given device and fiom device to device.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

*Note: X means Don't Care.

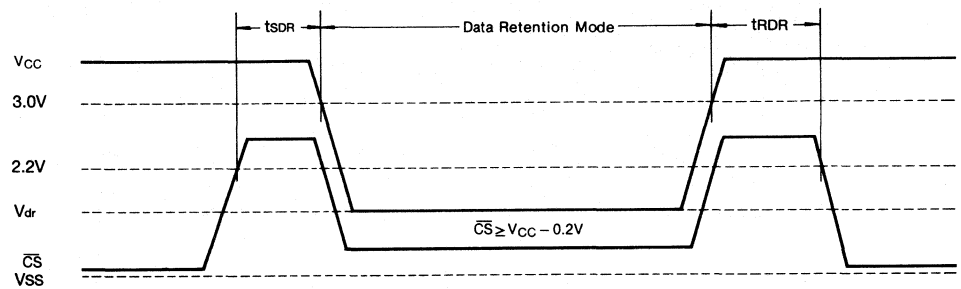
DATA RETENTION CHARACTERISTICS (T_A=0 to 70°C)

Parameter	Symbol	Test Condition	Min	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V	2.0	3.6	V
Data Retention Current	I_{DR}	V_{CC}=3.0V, $\overline{CS} \geq V_{CC}$-0.2V ($V_{IN} \geq$0.2V or $V_{IN} \leq V_{CC}$-0.2V)		100	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention	0		ns
Recovery Time	t_{RDR}	Waveforms(below)	t_{RC}*		ns

* t_{RC}=Read cycle time

2

DATA RETENTION WAVEFORM



SAMSUNG ELECTRONICS

32,768 WORDx8 Bit High Speed CMOS Static RAM(3.3V Operating)

FEATURES

- **Fast Access Time : 15, 17, 20ns(Max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 30mA (max)**
  - **(CMOS) : 100μA (max)**
  - **Operating : KM68V257C-15 : 90mA (max.)**
  - **KM68V257C-17 : 80mA (max.)**
  - **KM68V257C-20 : 70mA (max.)**
- **Single 3.3V±0.3V power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three state Outputs**
- **2V minimum Data Retention**
- **Standard Pin Configuration**
  - **KM68V257CP : 28-DIP-300**
  - **KM68V257CJ : 28-DIP-300**

GENERAL DESCRIPTION

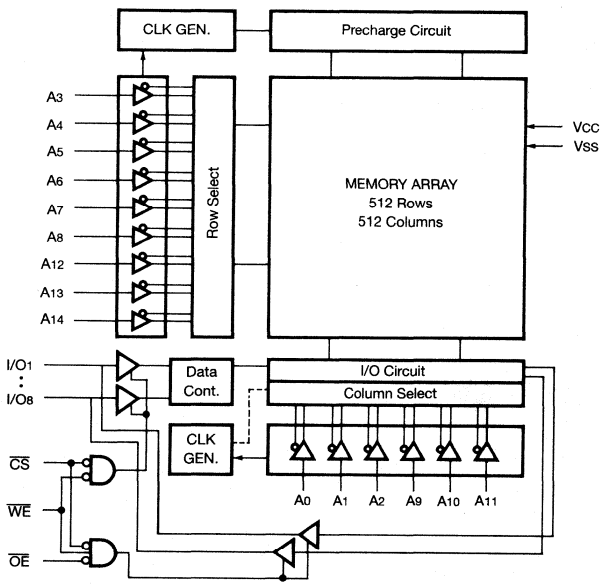
The KM68V257C is a 262,144 bit high speed Static Random Access Memory organized as 32,768 words by 8 bits.

The KM68V257C uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.

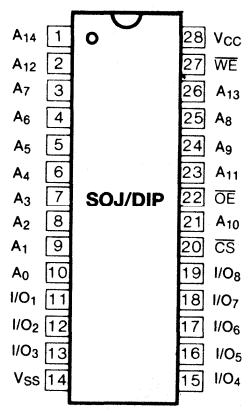
The KM68V257C is designed to operate at 3.3 volts. It is particularly well suited for use in high-density high-speed system applications.

The KM68V257C is packaged in a 300mil 28-pin plastic DIP or SOJ

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A14	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O8	Data Inputs/Outputs
VCC	Power(+3.3V)
VSS	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 5.5	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	-65 to 150	°C
Operating Temperature	T_a	0 to 70	°C

* Stresses greater than those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.3*	—	0.8	V

* V_{IL}(min)=-2.0V for $\leq$ 10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=3.3V$\pm$0.3V, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IN} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}		-	2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{out}=0mA	15ns	-	90	mA
			17ns	-	80	mA
			20ns	-	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min Cycle.		-	30	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}$-0.2V, f= o $V_{IN}\geq V_{CC}$-0.2 or $V_{IN}\leq$0.2V		-	100	μA
Output Low Voltage	V_{OL}	I_{OL}=8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4.0mA		2.4	-	V

CAPACITANCE (f=1MHz T_A=25°C)*

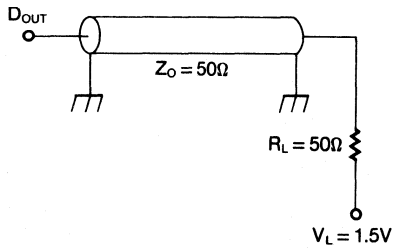
Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note : Capacitance is sampled and not 100% tested.

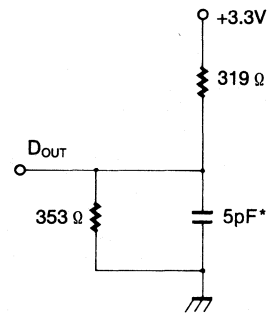
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=3.3V±0.3V, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{OLZ}, t_{OHZ}, t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	-15		-17		-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		ns
Address Access Time	t_{AA}		15		17		20	ns
Chip Select to Output	t_{ACS}		15		17		20	ns
Output Enable to Valid Output	t_{OE}		7		8		10	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	0	10	ns
Output Disable to High-Z Output	t_{OHZ}	0	7	0	8	0	10	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Chip selection to Power Up time	t_{PU}	0		0		0		ns
Chip Selection to Power Down Time	t_{PD}		15		17		20	ns

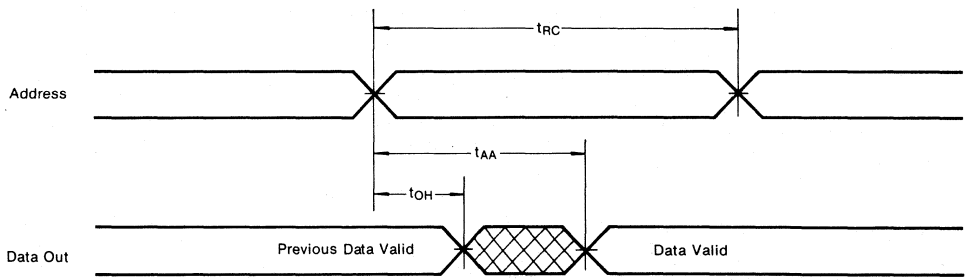
WRITE CYCLE

Parameter	Symbol	-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		ns
Chip Select to End of Write	t_{CW}	11		12		13		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	11		12		13		ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	11		12		13		ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP}	15		17		20		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	6	0	6	0	8	ns
Data to Write Time Overlap	t_{DW}	8		8		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		ns

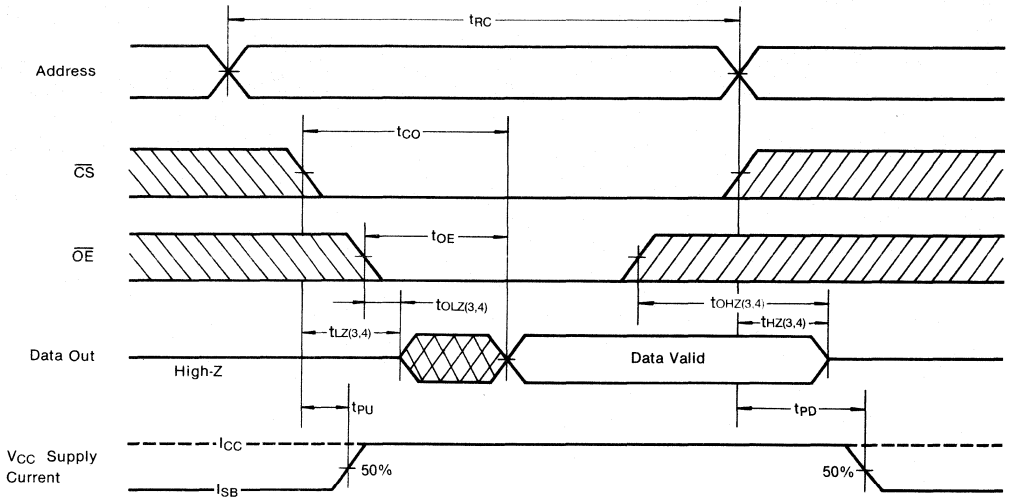
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



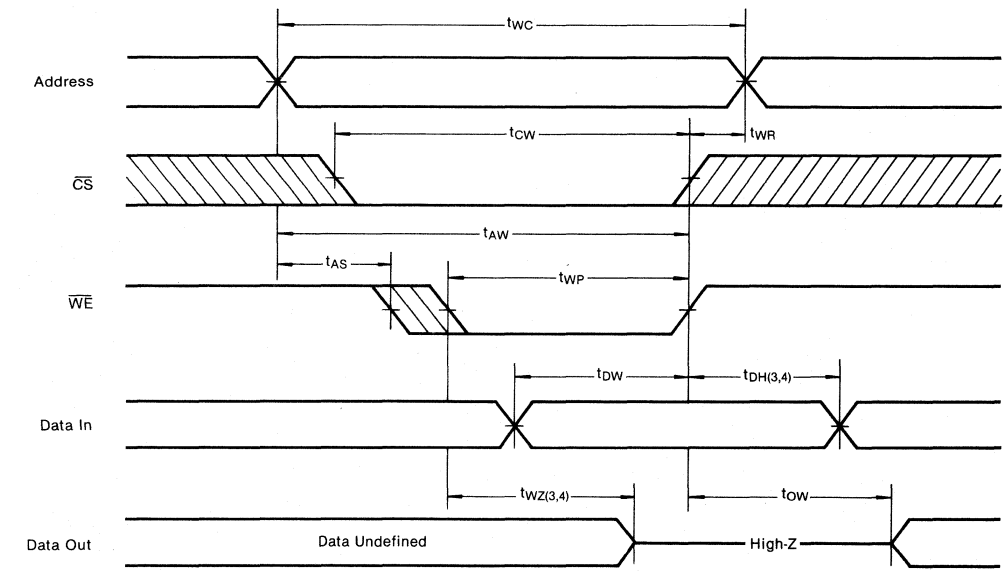
TIMING WAVEFORM OF READ CYCLE



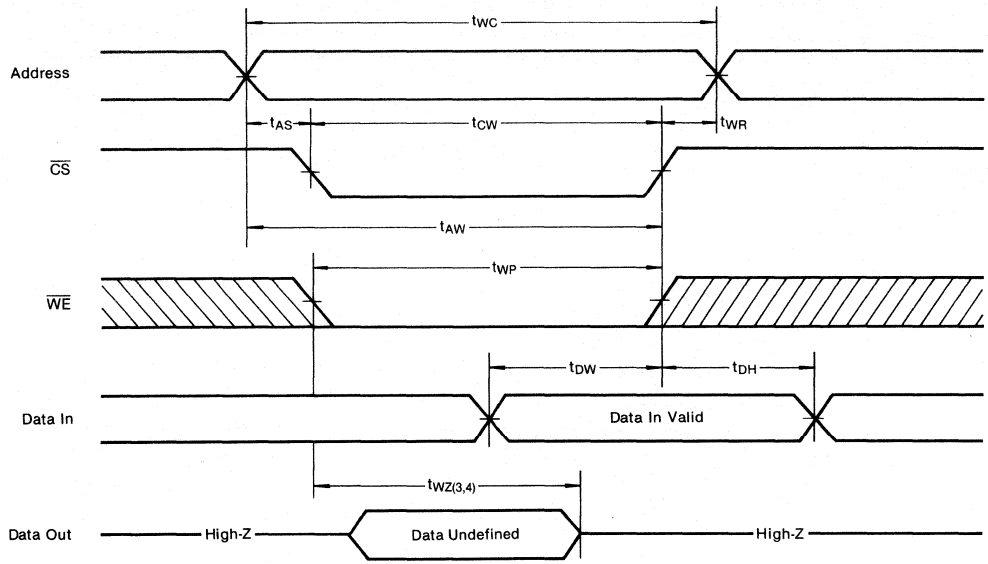
Notes(Read Cycle)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Address valid prior to or coincident with $\overline{CS}$ transition low
6. Device is continuously selected with $\overline{CS}$=V_{IL}.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Note (Write cycle)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, twz(max.) is less than tow(min.) both for a given device and from device to cevice.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

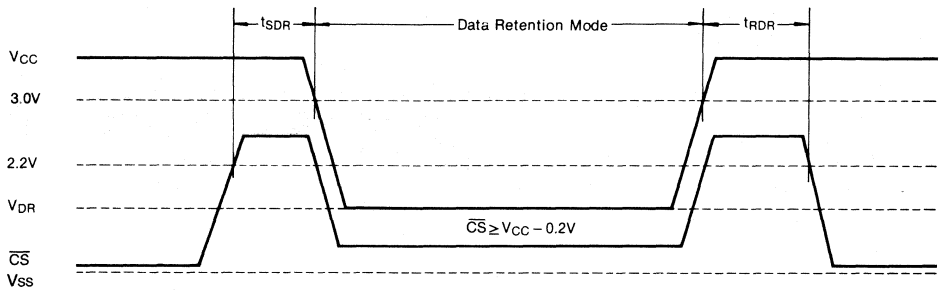
* Note: X means Don't Care.

DATA RETENTION CHARACTERISTICS (T_A=0 to 70°C)

Parameter	Symbol	Test Condition	Min	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V	2.0	3.6	V
Data Retention Current	I_{DR}	V_{CC}=3.0V, $\overline{CS} \geq V_{CC}$-0.2V $V_{IN} \leq V_{CC}$-0.2V or $V_{IN} \geq$ 0.2V	—	100	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention	0	—	ns
Recovery Time	t_{RDR}	Waveforms(below)	t_{RC}*	—	ns

* t_{RC}=Read cycle time

DATA RETENTION WAVEFORM



262,144 WORDx4 Bit High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

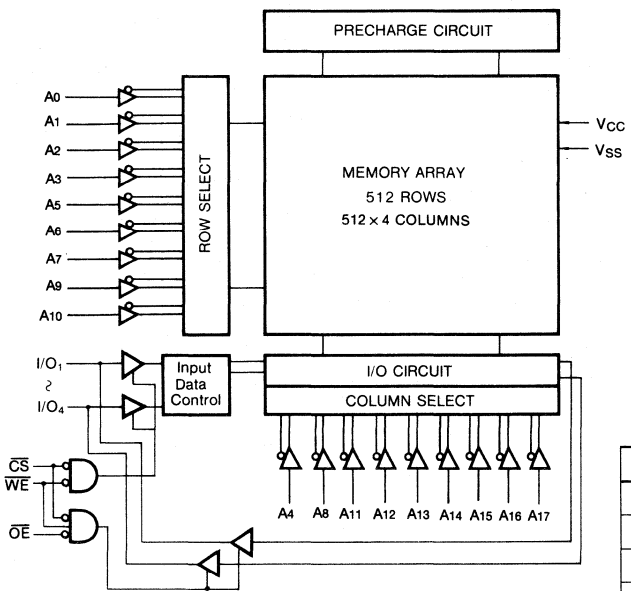
- **Fast Access Time : 12, 15, 17, 20ns (max.)**
- **Low Power Dissipation**
  Standby (TTL) : 20mA (max.)
  (CMOS) : 2mA (max.)
  Operating : KM64V1003-12 : 95mA (max.)
  KM64V1003-15 : 85mA (max.)
  KM64V1003-17 : 75mA (max.)
  KM64V1003-20 : 65mA (max.)
- **Single 3.3V±0.3V power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - No clock or refresh required
- **Three State Output**
- **Center Power/Ground Pin Configuration**
- **Standard Pin Configuration**
  KM64V1003AJ : 32-SOJ-400
  KM64V1003AT : 32--TSOP(II)-400F

GENERAL DESCRIPTION

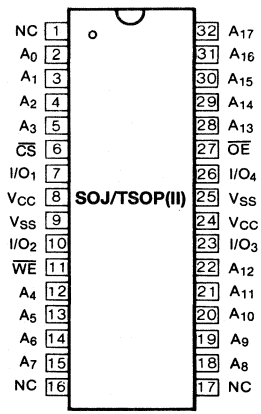
The KM64V1003A is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits.
The KM64V1003A uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology.
The KM64V1003A is designed to operate a 3.3V, it is particularly well suited for use in high-density high-speed system applecations
The KM64V1003A is packaged in a 400mil 32-pin plastic SOJ and TSOP(II).

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A0-A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Inputs / Outputs
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

131,072 WORDx8 Bit High-Speed CMOS Static RAM (3.3V Operating)

FEATURES

- **Fast Access Time : 12, 15, 17, 20ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 20mA (max.)**
  - **(CMOS) : 2mA (max.)**
  - **Operating : KM68V1002A-12 : 95mA (max.)**
  - **KM68V1002A-15 : 85mA (max.)**
  - **KM68V1002A-17 : 75mA (max.)**
  - **KM68V1002A-20 : 65mA (max.)**
- **Single 3.3V±0.3V power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three State Output**
- **Center Power/Ground Pin Configuration**
- **Standard Pin Configuration**
  - **KM681V002AJ : 32-SOJ-400**
  - **KM68V1002AT : 32-TSOP(I!)-400F**

GENERAL DESCRIPTION

The KM68V1002A is a 1,048,576-bit high speed Static Random Access Memory organized as 131,072 words by 8 bits.

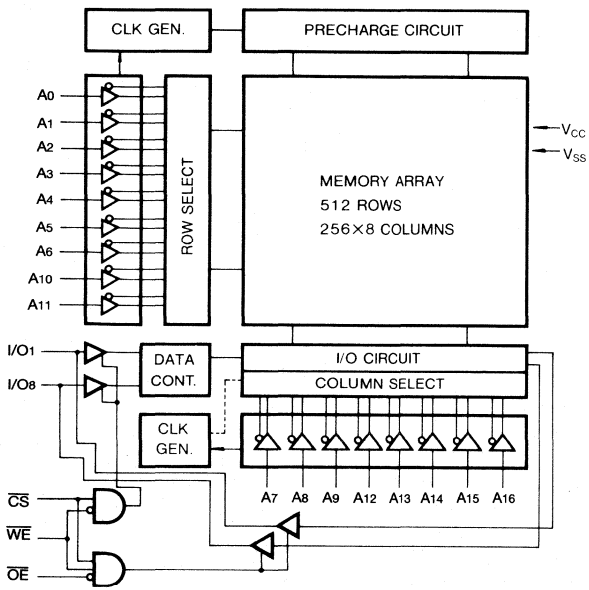
The KM68V1002A uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology.

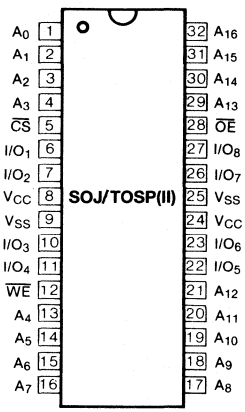
The KM68V1002A is designed to operate a 3.3V, it is particularly well suited for use in high-density high-speed system applications.

The KM68V1002A is packaged in a 400mil 32-pin plastic SOJ and a 400mil 32-pin plastic TSOP(II).

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A16	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1~I/O8	Data Inputs/Outputs
VCC	Power(+3.3V)
VSS	Ground

65,536 WORDx16 Bit High-Speed CMOS Static RAM (3.3V Operating)

FEATURES

- **Fast Access Time : 12, 15, 17, 20ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 20mA (max.)**
  - **(CMOS) : 2mA (max.)**
  - **Operating : KM616V1002A-12 : 110mA (max.)**
  - **KM616V1002A-15 : 100mA (max.)**
  - **KM616V1002A-17 : 90mA (max.)**
  - **KM616V1002A-20 : 80mA (max.)**
- **Single 3.3V±0.3V power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three State Output**
- **Data Byte Control : $\overline{LB}$: I/O1~I/O8**
  $\overline{UB}$: I/O9~I/O16
- **Standard Pin Configuration**
  KM616V1002AJ : 44-SOJ-400
  KM616V1002AT : 44-TSOP(II)-400F

GENERAL DESCRIPTION

The KM616V1002A is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits.

The KM616V1002A uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{UB}$, $\overline{LB}$).

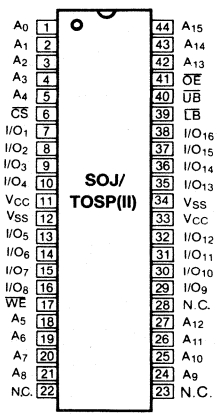
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology.

The KM616V1002A is designed to operate a 3.3V, it is particularly well suited for use in high-density high-speed system applications.

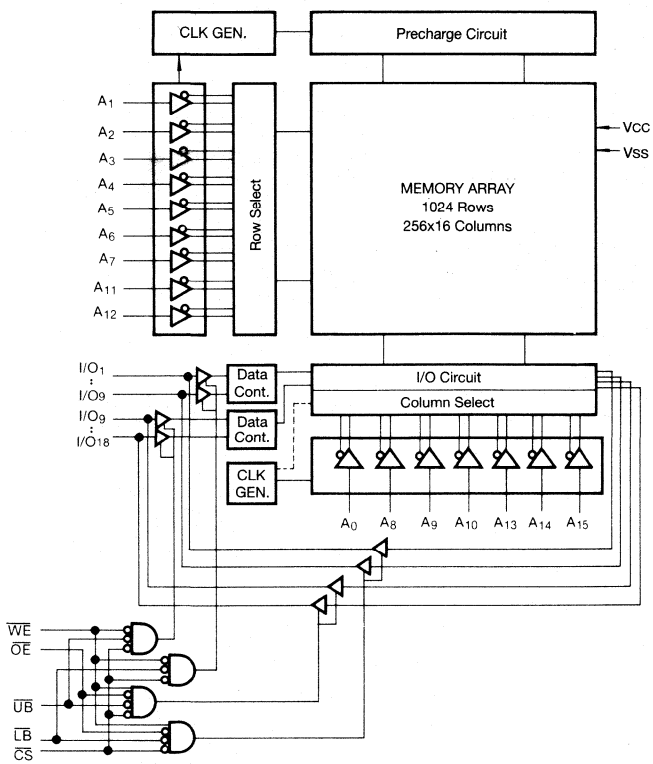
The KM616V1002A is packaged in a 400mil 44-pin plastic SOJ and a 400mil 44-pin plastic TSOP(II).

2

PIN CONFIGURATION (Top Views)



FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A0-A15	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1~I/O16	Data Inputs/Outputs
VCC	Power(+3.3V)
VSS	Ground
NC	No Connection

65,536 WORD × 4 Bit (With $\overline{OE}$) High-Speed BiCMOS Static RAM

FEATURES

- **Fast Access Time: 8, 10, 12ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 110mA (max.)**
  - **(CMOS): 20mA (max.)**
  - **Operating KM64B258AJ-8: 185mA (max.)**
  - **KM64B258AJ-10: 175mA (max.)**
  - **KM64B258AJ-12: 165mA (max.)**
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three State Outputs**
- **Standard Pin Configuration**
  - **KM64B258AJ: 28-SOJ-300**

GENERAL DESCRIPTION

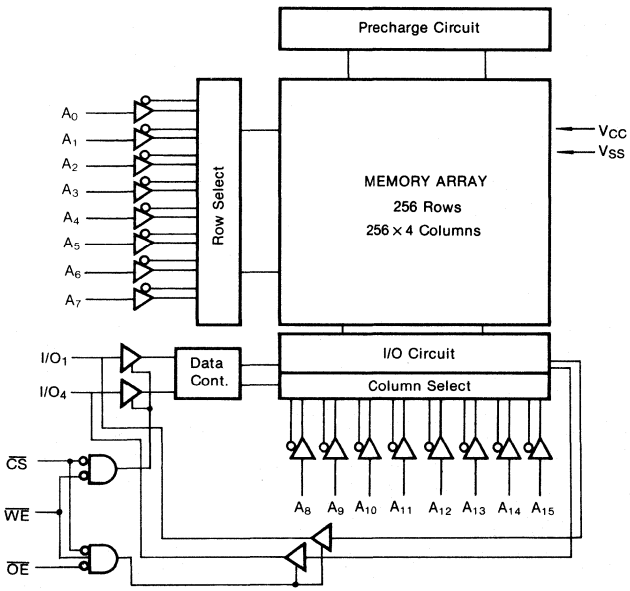
The KM64B258A is a 262,144-bit high-speed Static Random Access Memory organized as 65,536 words by 4 bits.

The KM64B258A uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology.

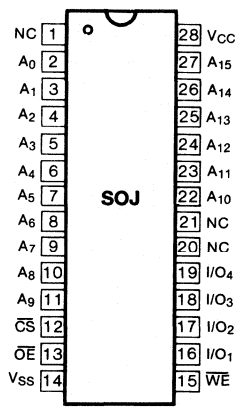
It is particularly well suited for use in high-density high-speed system applications.

The KM64B258A is packaged in a 300 mil 28-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Pin Name	Pin Function
A_0-A_{15}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_1-I/O_4	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5**	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL} (min.) = −2.0V ac (pulse width ≤ 8ns) for I ≤ 20mA
** V_{IH} (max.) = V_{CC} + 2V ac (pulse width ≤ 8ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}		—	2	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{OUT} = V_{SS}$ to V_{CC}		—	10	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty, $\overline{CS} = V_{IL}$, I_{OUT} = 0mA	8ns	—	185	mA
			10ns	—	175	mA
			12ns	—	165	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$, $V_{IN} = V_{IH}/V_{IL}$, Min. Cycle		—	110	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		—	20	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA		—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4.0mA		2.4	—	V

CAPACITANCE (f = 1MHz, T_A = 25°C)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

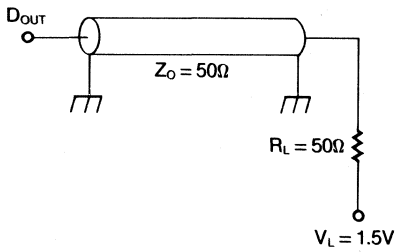
Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

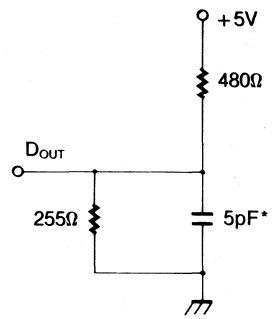
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{OLZ}, t_{OHZ}, t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including Scope and Jig Capacitance

READ CYCLE

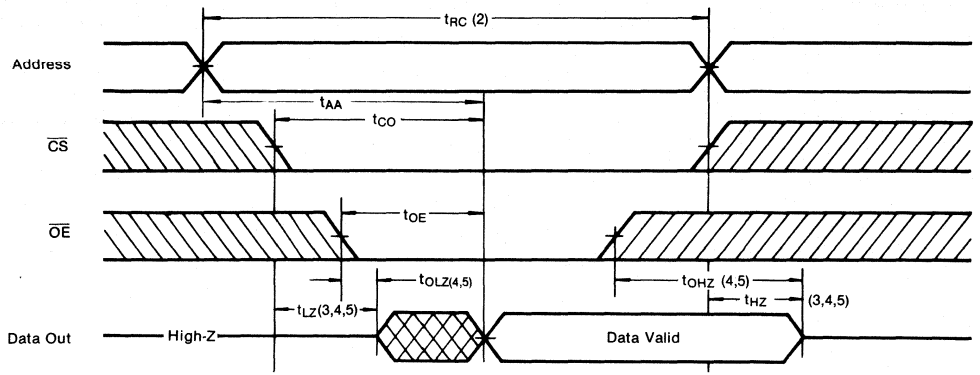
Parameter	Symbol	KM64B258A-8		KM64B258A-10		KM64B258A-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	8	-	10	-	12	-	ns
Address Access Time	t_{AA}	-	8	-	10	-	12	ns
Chip Select to Output	t_{ACS}	-	8	-	10	-	12	ns
Output Enable to Valid Output	t_{OE}	-	4	-	5	-	6	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	4	0	5	0	6	ns
Output Disable to High-Z Output	t_{OHZ}	0	4	0	5	0	6	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM64B258A-8		KM64B258A-10		KM64B258A-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	8	-	10	-	12	-	ns
Chip Select to End of Write	t_{CW}	6	-	7	-	9	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	6	-	7	-	9	-	ns
Write Pulse Width ($\overline{OE}$ Low)	t_{WP}	8	-	10	-	12	-	ns
Write Pulse Width ($\overline{OE}$ High)	t_{WP}	6	-	7	-	9	-	ns
Write Recovery Time	t_{WR}	1	-	1	-	1	-	ns
Write to Output High-Z	t_{WZ}	0	4	0	5	0	6	ns
Data to Write Time Overlap	t_{DW}	4	-	5	-	6	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

TIMING DIAGRAMS

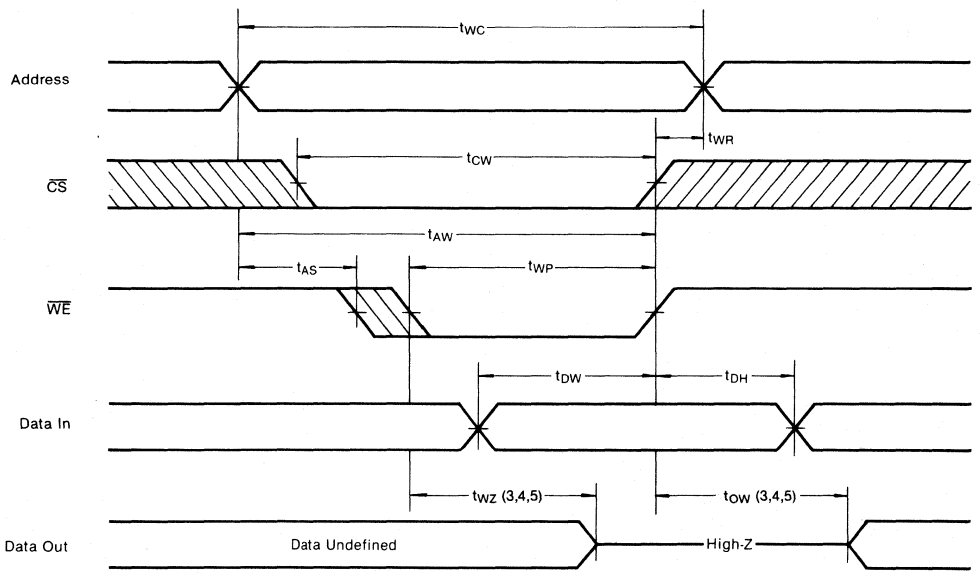
TIMING WAVEFORM OF READ CYCLE



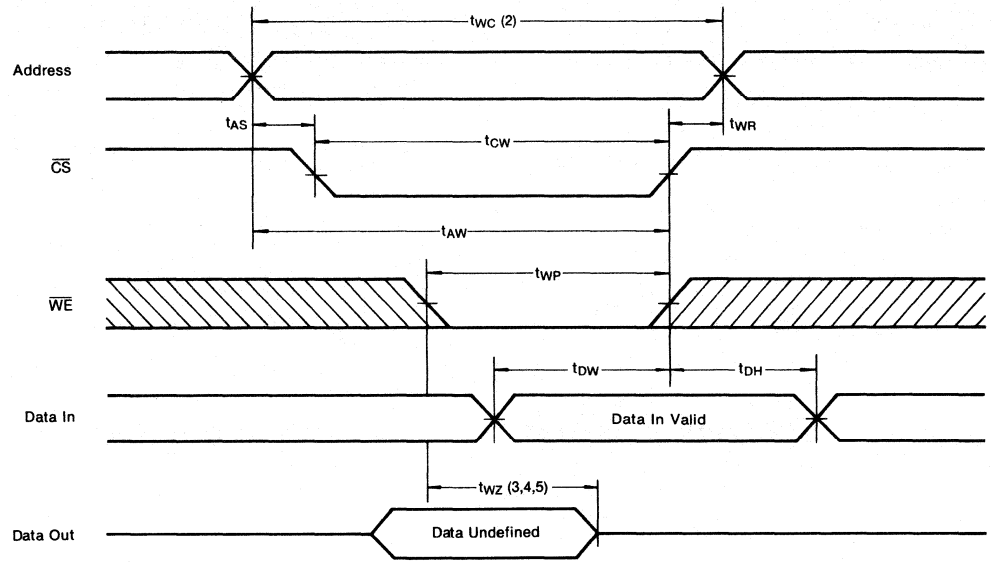
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B).
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS} = V_{IL}$.
7. Address valid prior to or coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ} (max.) is less than t_{OW} (min.) both for a given device and from device to device.
6. For common I/O applications, minimization or elimination of bus contention conditions is neessary during read and write cycles.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

65,536 WORD×4 Bit High-Speed BiCMOS Static RAM

FEATURES

- **Fast Access Time: 6, 7, 8 ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 90mA (max.)**
  - **(CMOS): 20mA (max.)**
- **Operating Current : 160mA (f = 100 MHz.)**
- **Single 5V ± 5% Power Supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **— No clock or refresh required**
- **Three State Output**
- **Center Power/Ground Pin Configuration**
- **Package: 28-SOJ-300**

GENERAL DESCRIPTION

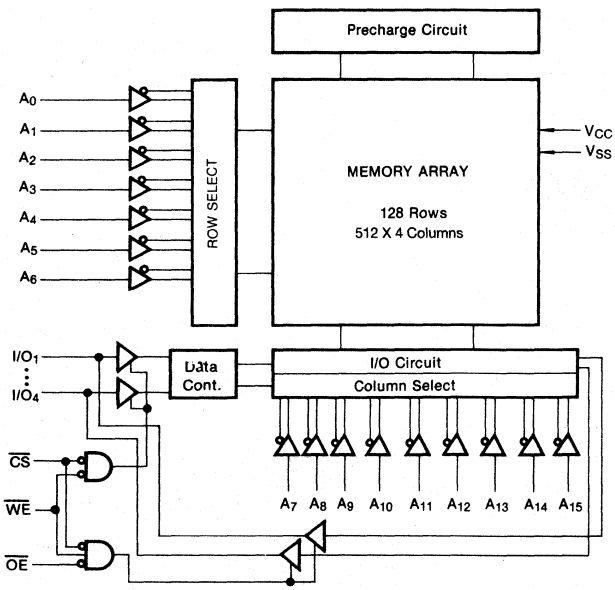
The KM64B261A is a 262,144-bit high-speed Static Random Access Memory organized as 65,536 words by 4 bits.

The KM64B261A uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed system applications.

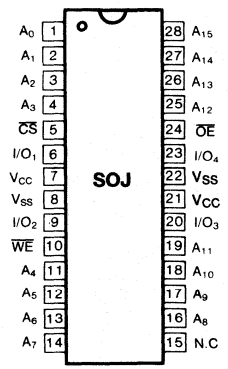
It is particularly well suited for use in high-density high-speed system applications.

The KM64B261A is packaged in a 300mil 28-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(Top View)



Pin Names	Pin Function
A_0-A_{15}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$I/O_1 \sim I/O_4$	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.)=-3.0V ac (pulse width 3≤ns) for I≤20mA

** V_{IH}(max.)=V_{CC}+2.0V ac (pulse width ≤8ns) for I≤20mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±5%, unless otherwise specified)

Item	Symbol	Test Condition	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = V_{SS} to V_{CC}	—	10	μA
Average Operating Current	I_{CC}	f = 100 MHz, 100% Duty $\overline{CS}$ = V_{IL}, I_{OUT} = 0mA	—	160	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH}/V_{IL}, Min. Cycle	—	90	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC}-0.2V, f=0 MHz V_{IN} ≥ V_{CC}-0.2 or V_{IN} ≤ 0.2V	—	20	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	0.4	V
Output High Voltage	I_{OH}	I_{OH} = −4mA	2.4	—	V

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)*

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	7	pF

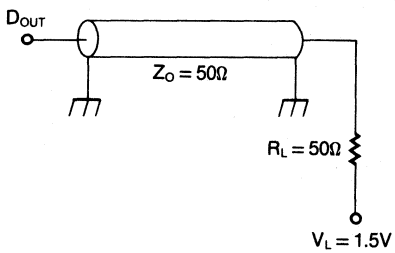
*Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS

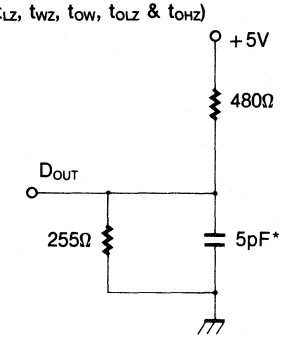
(T_A=0 to 70°C, V_{CC}=5V±5%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

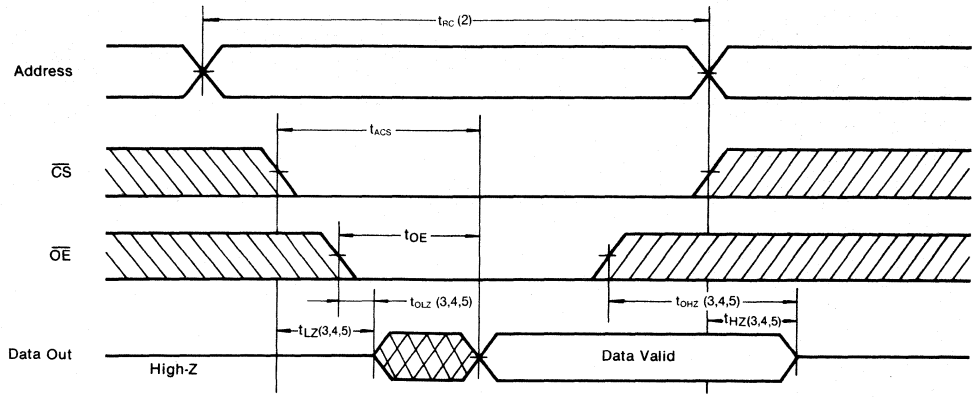
READ CYCLE

Parameter	Symbol	KM64B261A-6		KM64B261A-7		KM64B261A-8		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	6	-	7	-	8	-	ns
Address Access Time	t_{AA}	-	6	-	7	-	8	ns
Chip Select to Output	t_{ACS}	-	6	-	7	-	8	ns
Output Enable to Valid Output	t_{OE}	-	4	-	4	-	4	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	1	-	1	-	1	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	3	0	3.5	0	4	ns
Output Disable to High-Z Output	t_{OHZ}	0	3	0	3.5	0	4	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM64B261A-6		KM64B261A-7		KM64B261A-8		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	6	-	7	-	8	-	ns
Chip Select to End of Write	t_{CW}	6	-	7	-	8	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	3.5	-	4	-	4.5	-	ns
Write Pulse Width ($\overline{OE}$ Low)	t_{WP}	6	-	7	-	8	-	ns
Write Pulse Width ($\overline{OE}$ High)	t_{WP}	3.5	-	4	-	4.5	-	ns
Write Recovery Time	t_{WR}	1	-	1	-	1	-	ns
Write to Output High-Z	t_{WZ}	0	3.0	0	3.5	0	4.0	ns
Data to Write Time Overlap	t_{DW}	3	-	3.5	-	4	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

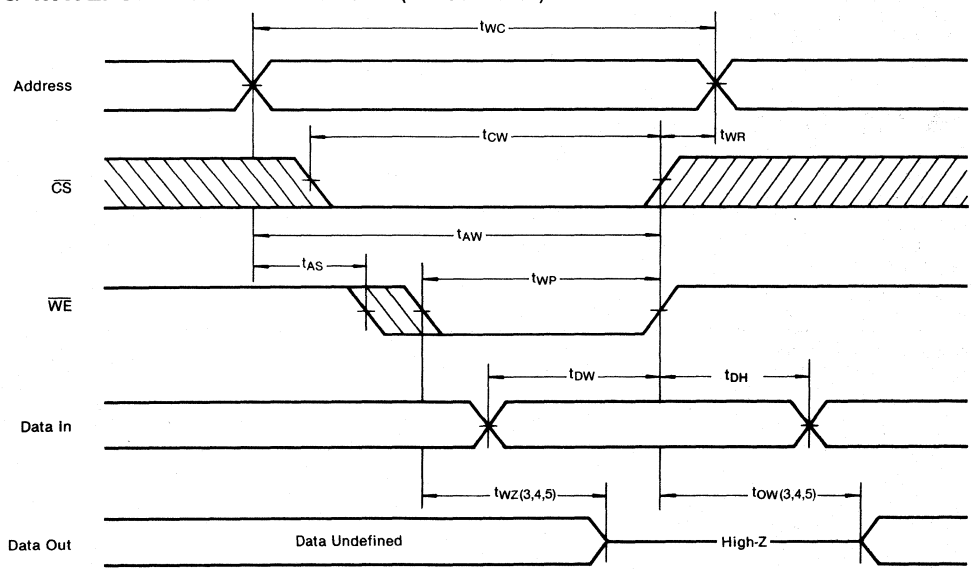
TIMING WAVEFORM OF READ CYCLE



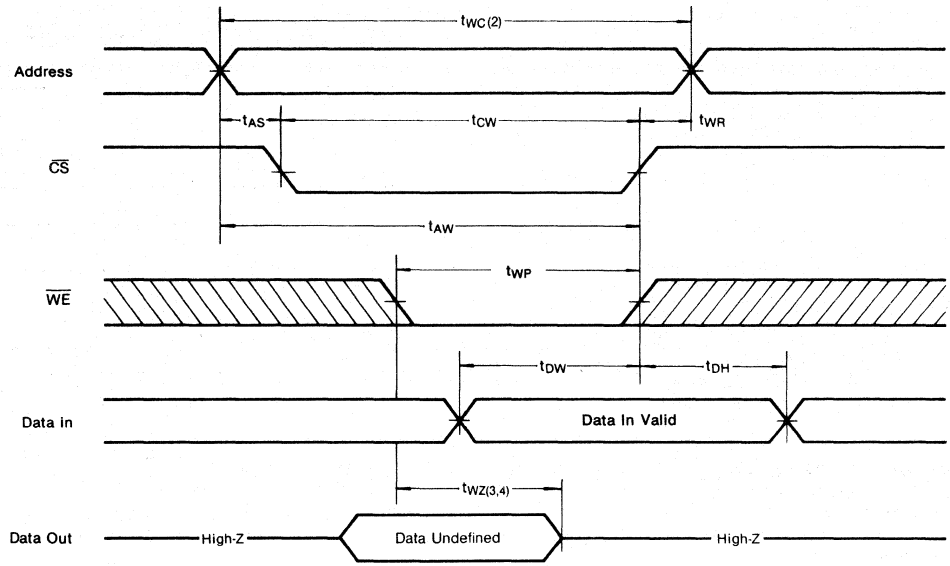
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load(B).
5. This parameter is sample and not 100% tested.
6. Device is continuously selected with $\overline{CS} = V_{IL}$.
7. Address valid prior to or concident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of $\overline{CS}$ low $\overline{WE}$ low.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltate with Load (B).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ} (max.) is less than t_{OW} (min.) both for a given device and from device to device.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

*Note: X means Don't Care.

32,768 WORD x 8 Bit High Speed BiCMOS Static RAM

FEATURES

- **Fast Access Time: 8, 9, 10, 12ns (Max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 110mA (max.)**
  - **(CMOS): 20mA (max.)**
  - **Operating KM68B257AJ-8: 185mA (Max.)**
  - **KM68B257AJ-9: 185mA (Max.)**
  - **KM68B257AJ-10: 175mA (Max.)**
  - **KM68B257AJ-12: 165mA (Max.)**
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  - **—No clock or refresh required**
- **Three State Outputs**
- **Standard Pin Configuration**
  - **KM68B257AJ: 28-SOJ-300**

GENERAL DESCRIPTION

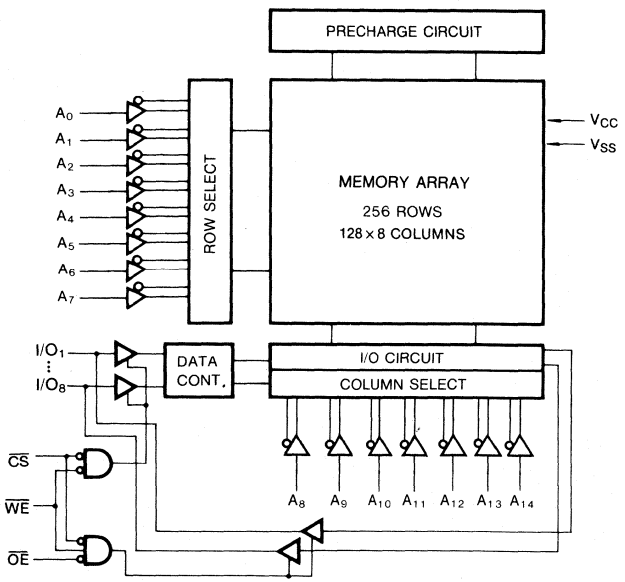
The KM68B257A is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.

The KM68B257A uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology.

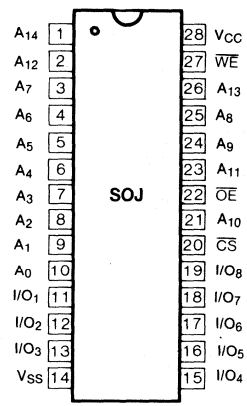
It is particularly well suited for use in high-density high-speed system applications.

The KM68B257A is packaged in a 300 mil 28-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS (Top View)



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5**	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL} (min.) = −2.0V ac (pulse width ≤ 8ns) for I ≤ 20mA
** V_{IH} (max.) = V_{CC} + 2V ac (pulse width ≤ 8ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Item	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		—	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		—	10	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty, $\overline{CS}$=V_{IL}, I_{OUT}=0mA, $\overline{WE}$=V_{IL} or $\overline{WE}$=$\overline{OE}$=V_{IH}	8ns	—	185	mA
			9ns	—	185	mA
			10ns	—	175	mA
			12ns	—	165	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, V_{IN}=V_{IH}/V_{IL}, Min. Cycle		—	110	mA
	I_{SB1}	$\overline{CS}$ ≥ Vcc−0.2V, f=0 MHz, V_{IN} ≥ Vcc−0.2V or V_{IN} ≤ 0.2V		—	20	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4.0mA		2.4	—	V

CAPACITANCE (f = 1MHz, T_A = 25°C)

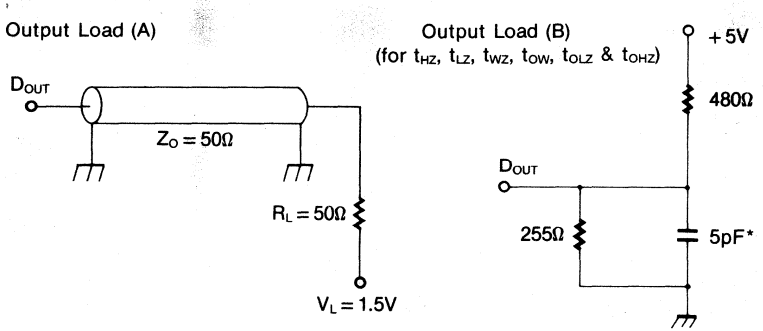
Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	See below



* Including Scope and Jig Capacitance

READ CYCLE

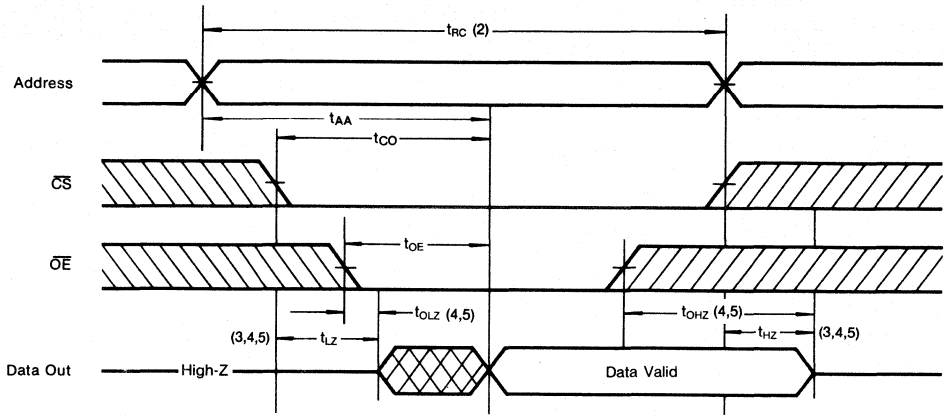
Parameter	Symbol	KM68B257A-8		KM68B257A-9		KM68B257A-10		KM68B257A-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	8	-	9	-	10	-	12	-	ns
Address Access Time	t_{AA}	-	8	-	9	-	10	-	12	ns
Chip Select to Output	t_{CO}	-	8	-	9	-	10	-	12	ns
Output Enable to Valid Output	t_{OE}	-	4	-	4	-	5	-	6	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	4	0	4	0	5	0	6	ns
Output Disable to High-Z Output	t_{OHZ}	0	4	0	4	0	5	0	6	ns
Output Hold from Address Change	t_{OH}	3	1	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM68B257A-8		KM68B257A-9		KM68B257A-10		KM68B257A-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	8	-	9	-	10	-	12	-	ns
Chip Select to End of Write	t_{CW}	6	-	6	-	7	-	9	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	6	-	7	-	7	-	9	-	ns
Write Pulse Width ($\overline{OE}$ Low)	t_{WP}	8	-	8	-	10	-	12	-	ns
Write Pulse Width ($\overline{OE}$ High)	t_{WP}	6	-	6	-	7	-	9	-	ns
Write Recovery Time	t_{WR}	1	-	1	-	1	-	1	-	ns
Write to Output High-Z	t_{WZ}	0	4	0	4	0	5	0	6	ns
Data to Write Time Overlap	t_{DW}	4	-	4	-	5	-	6	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	3	-	ns

TIMING DIAGRAMS

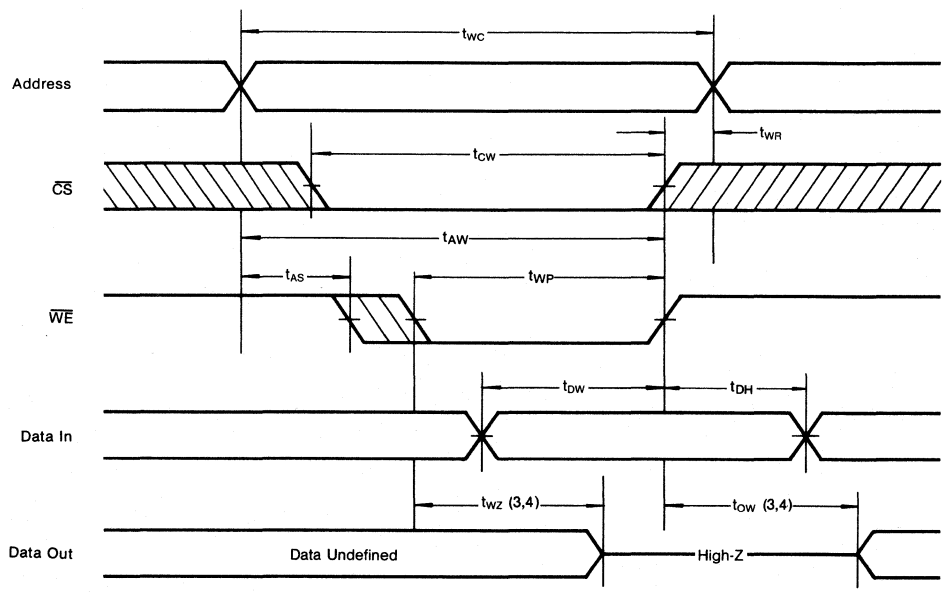
TIMING WAVEFORM OF READ CYCLE



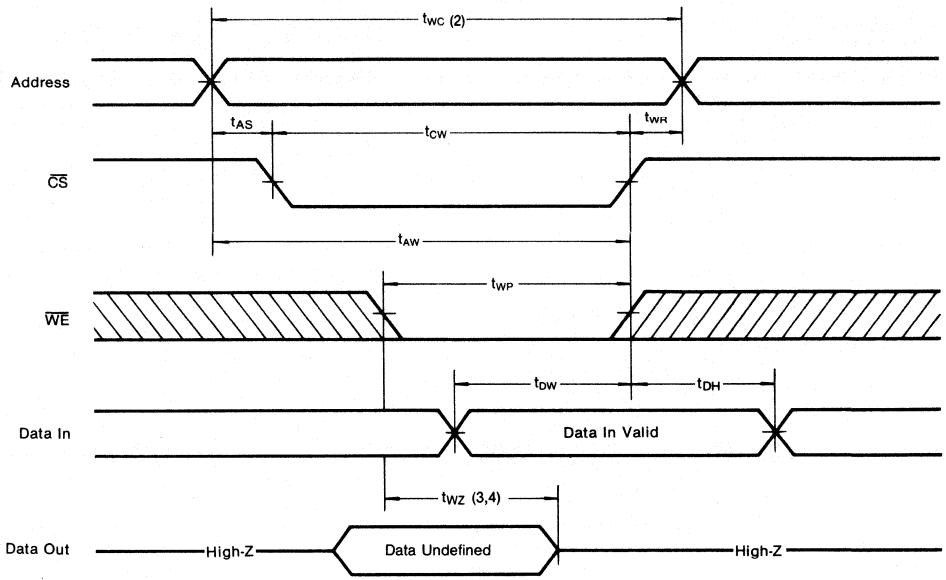
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B).
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS} = V_{IL}$.
7. Address valid prior to or coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ} (max.) is less than t_{OW} (min.) both for a given device and from device to device.
5. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

32,768 WORD x 8 Bit High-Speed CMOS Static RAM

FEATURES

- **Fast Access Time: 6, 7, 8 ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 90mA (max.)**
  - **(CMOS): 20mA (max.)**
- **Operating Current : 170mA (f = 100 MHz.)**
- **Single 5V ± 5% Power Supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **— No clock or refresh required**
- **Three State Output**
- **Center Power/Ground Pin Configuration**
- **Package: 32-SOJ-300**

GENERAL DESCRIPTION

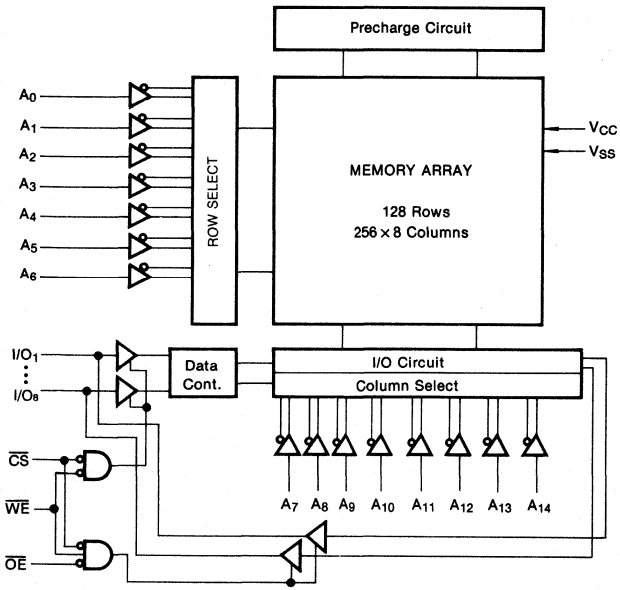
The KM68B261A is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.

The KM68B261A uses eight common input and output lines and has an output enable pin which operates faster than address access time are read cycle. The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed system applications.

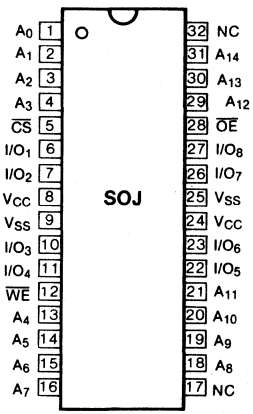
It is particularly well suited for use in high-density high-speed system applications.

The KM68B261A is packaged in a 300mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Pin Names	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$I/O_1 \sim I/O_8$	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5**	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min.) = −3.0V ac (pulse width ≤3ns) for I≤20mA.
**V_{IH} (max.) = V_{CC} + 2.0V ac (pulse width ≤8ns) for I≤20mA.

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified)

Item	Symbol	Test Condition	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}	—	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = V_{SS} to V_{CC}	—	10	μA
Average Operating Current	I_{CC}	f = 100 MHz, 100% Duty $\overline{CS}$ = V_{IL}, I_{OUT} = 0mA	—	170	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH}/V_{IL}, Min. Cycle	—	90	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC}-0.2V, f=0 MHz V_{IN} ≥ V_{CC}-0.2 or V_{IN} ≤ 0.2V	—	20	mA
Output Low Voltage	VOL	I_{OL} = 8mA	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4mA	2.4		V

CAPACITANCE (f = 1MHz, T_A = 25°C)*

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

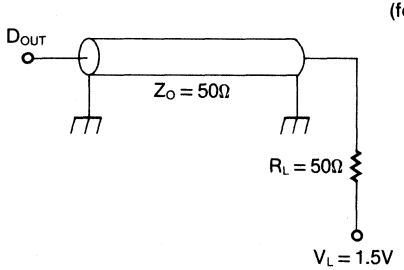
*Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS

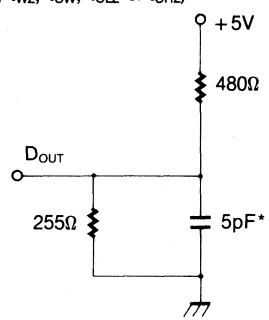
(T_A = 0 to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

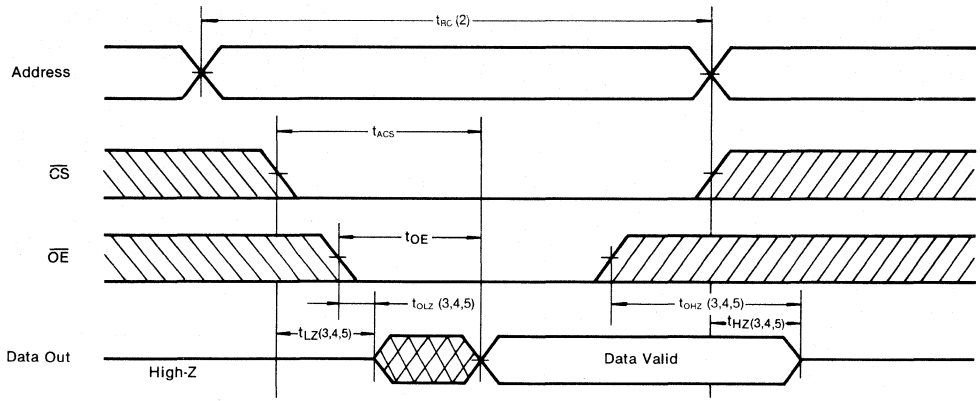
READ CYCLE

Parameter	Symbol	KM68B261A-6		KM68B261A-7		KM68B261A-8		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	6	-	7	-	8	-	ns
Address Access Time	t_{AA}	-	6	-	7	-	8	ns
Chip Select to Output	t_{ACS}	-	6	-	7	-	8	ns
Output Enable to Valid Output	t_{OE}	-	4	-	4	-	4	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	1	-	1	-	1	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	3	0	3.5	0	4	ns
Output Disable to High-Z Output	t_{OHZ}	0	3	0	3.5	0	4	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM68B261A-6		KM68B261A-7		KM68B261A-8		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	6	-	7	-	8	-	ns
Chip Select to End of Write	t_{CW}	6	-	7	-	8	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	3.5	-	4	-	4.5	-	ns
Write Pulse Width ($\overline{OE}$ Low)	t_{WP}	6	-	7	-	8	-	ns
Write Pulse Width ($\overline{OE}$ High)	t_{WP}	3.5	-	4	-	4.5	-	ns
Write Recovery Time	t_{WR}	1	-	1	-	1	-	ns
Write to Output High-Z	t_{WZ}	0	3.0	0	3.5	0	4.0	ns
Data to Write Time Overlap	t_{DW}	3	-	3.5	-	4	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

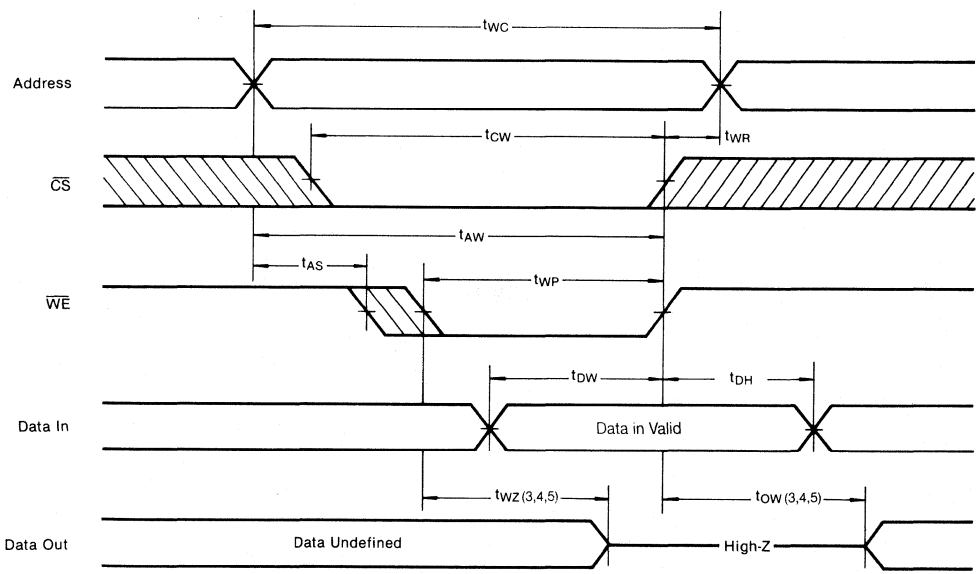
TIMING WAVEFORM OF READ CYCLE



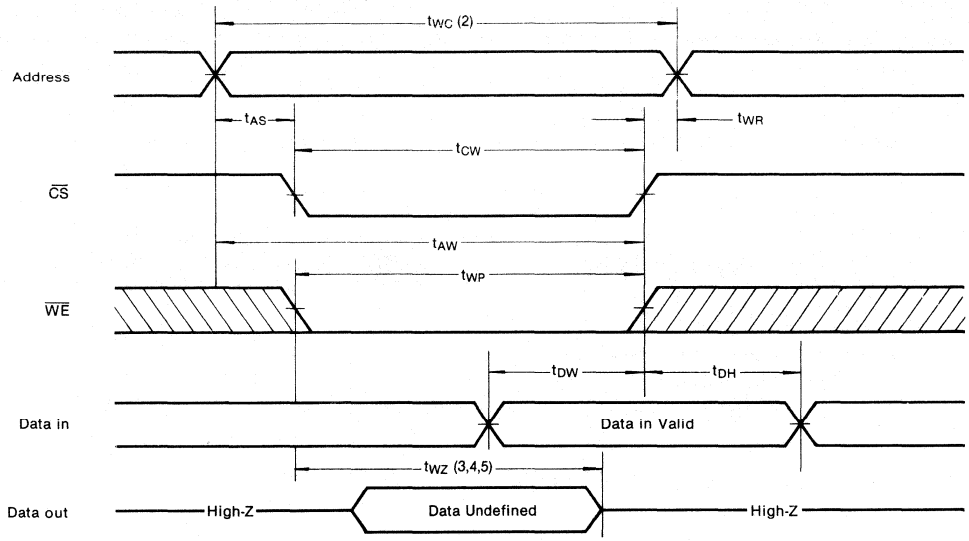
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load(B).
5. This parameter is sample and not 100% tested.
6. Device is continuously selected with $\overline{CS} = V_{IL}$.
7. Address valid prior to or concident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (CS Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of $\overline{CS}$ low and $\overline{WE}$ low.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltate with Load (B).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ} (max.) is less than t_{OW} (min.) both for a given device and from device to device.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

*Note: X means Don't Care.

262,144 WORD x 4 Bit (With $\overline{OE}$) Ultra High-Speed BiCMOS Static RAM

FEATURES

- **Fast Access Time: 8, 10, 12, 15ns (Max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 60mA (Max.)**
  - **(CMOS): 10mA (Max.)**
  - **Operating : KM6481003J-8: 165mA (Max.)**
  - **KM64B1003J-10: 155mA (Max.)**
  - **KM64B1003J-12: 145mA (Max.)**
  - **KM64B1003J-15: 135mA (Max.)**
- **Single 5V ± 10% Power Supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **— No clock or refresh required**
- **Three State Output**
- **Center Power/Ground Pin Configuration**
- **Standard Pin Configuration**
  KM64B1003J : 32-SOJ-400

GENERAL DESCRIPTION

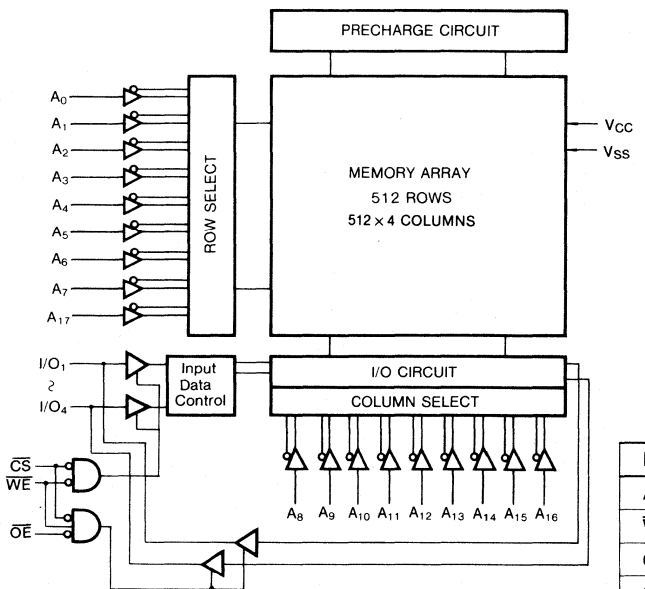
The KM64B1003 is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits.

The KM64B1003 uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

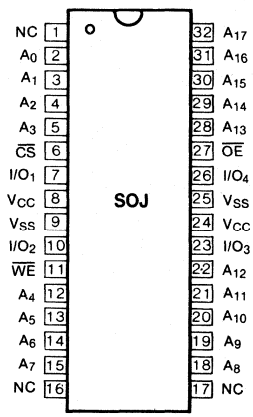
The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particulary well suited for use in high-density high-speed system applications.

The KM64B1003 is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_4	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5**	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL} (min.)=−2.0V ac (pulse width ≤ 10ns) for I ≤ 20mA
** V_{IH} (max.)= V_{CC} +2V ac (pulse width ≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}		−2	+2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL}, $\overline{OE}$=V_{IH} V_{OUT}=V_{SS} to V_{CC}		−10	+10	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{OUT}=0mA V_{IN}=V_{IH}/V_{IL}	8ns	—	165	mA
			10ns	—	155	
			12ns	—	145	
			15ns	—	135	
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH}/V_{IL}, Min. Cycle		—	60	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC}-0.2V, f=0 MHz V_{IN} ≤ 0.2 or V_{IN} ≥ V_{CC}-0.2V		—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA		—	0.4	V
Output High Voltage	I_{OH}	I_{OH} = −4mA		2.4	—	V

CAPACITANCE (f = 1MHz, T_A = 25°C)*

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	8	pF

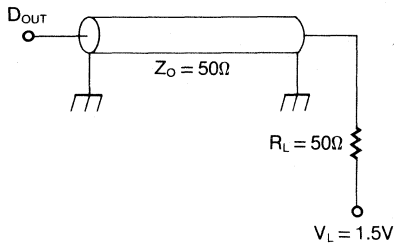
*Capacitance is sampled and not 100% tested.

TEST CONDITIONS

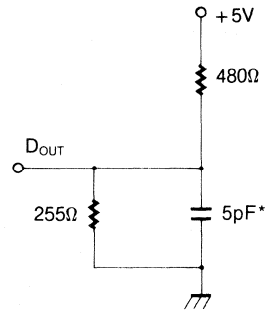
(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{OLZ}, t_{OHZ}, t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including Scope and Jig Capacitance

READ CYCLE

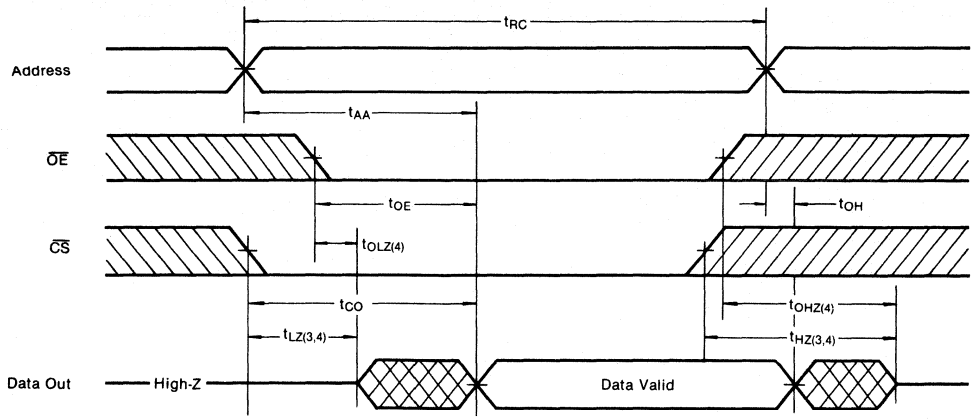
Parameter	Symbol	KM64B1003-8		KM64B1003-10		KM64B1003-12		KM64B1003-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	8	-	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	8	-	10	-	12	-	15	ns
Chip Select to Output	t_{CO}	-	8	-	10	-	12	-	15	ns
Output Enable to Valid Output	t_{OE}	-	4	-	5	-	6	-	6	ns
Chip Select to Low-Z Output	t_{LZ}	3	-	0	-	0	-	0	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	3	-	3	-	3	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	4	-	5	-	6	-	6	ns
Output Disable to High-Z Output	t_{OHZ}	0	4	-	5	-	6	-	6	ns
Output Hold from Address Change	t_{OH}	3	1	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM64B1003-8		KM64B1003-10		KM64B1003-12		KM64B1003-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	8	-	10	-	12	-	15	-	ns
Chip Select to End of Write	t_{CW}	6	-	7	-	8	-	10	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	6	-	7	-	8	-	10	-	ns
Write Pulse Width ($\overline{OE}$ High)	t_{WP}	6	-	7	-	8	-	8	-	ns
Write Pulse Width ($\overline{OE}$ Low)	t_{WP}	8	-	9	-	10	-	10	-	ns
Write Recovery Time	t_{WR}	1	-	1	-	1	-	1	-	ns
Write to Output High-Z	t_{WZ}	-	4	-	5	-	6	-	6	ns
Data to Write Time Overlap	t_{DW}	4	-	5	-	6	-	7	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	3	-	ns

TIMING DIAGRAMS

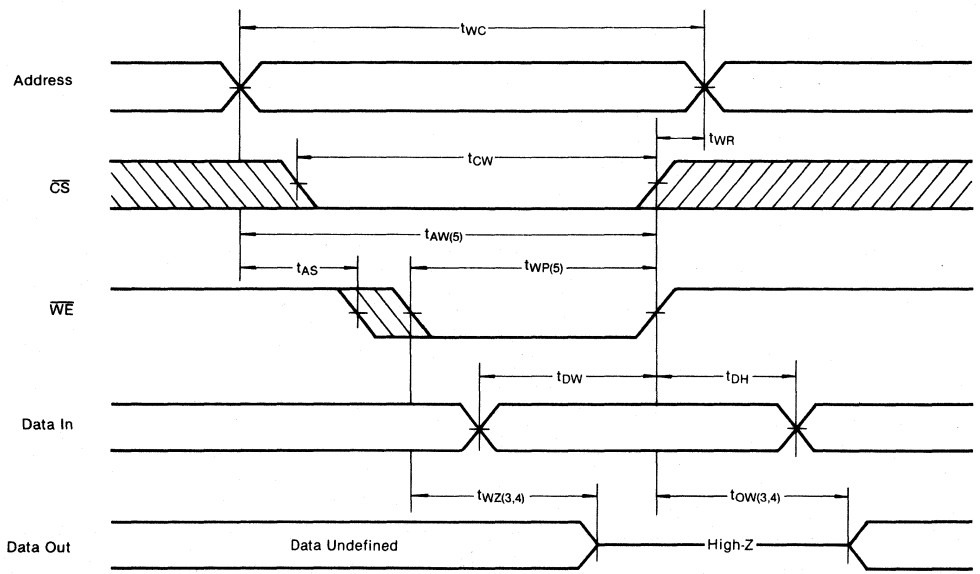
TIMING WAVEFORM OF READ CYCLE



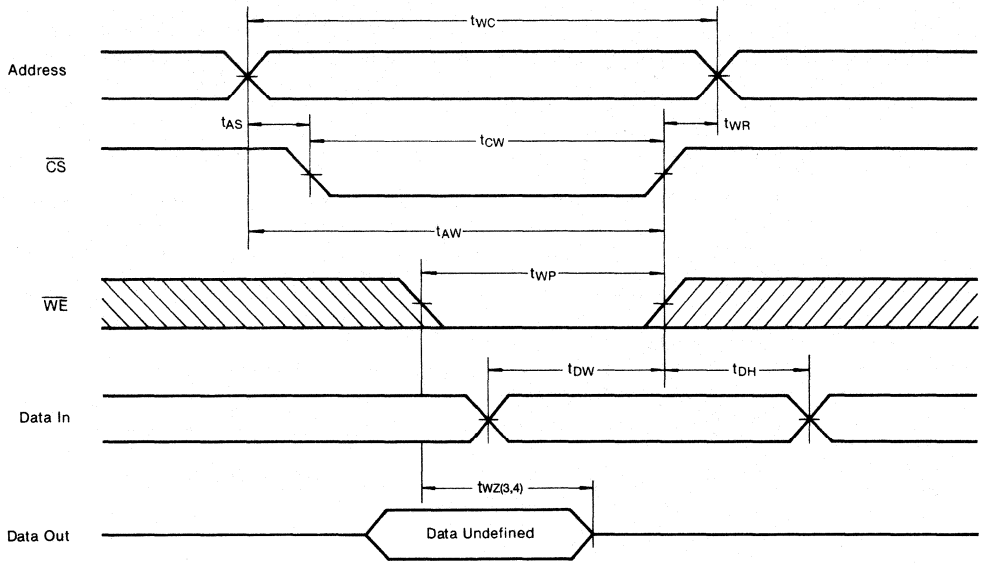
Notes (Read Cycle)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
4. Transition is measuled ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. For common I/O applications, minimization or elimination of bus contention conditions is neessary during read and write cycles.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (Write Cycle)

1. A write occures during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
5. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

131,072 WORD x 8 Bit Ultra High-Speed BiCMOS Static RAM

FEATURES

- **Fast Access Time: 8, 9, 10, 12, 15ns (Max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 60mA (Max.)**
  - **(CMOS): 10mA (Max.)**
  - **Operating KM68B1002J-8: 175mA (Max.)**
  - **KM68B1002J-9: 175mA (Max.)**
  - **KM68B1002J-10: 165mA (Max.)**
  - **KM68B1002J-12: 155mA (Max.)**
  - **KM68B1002J-15: 145mA (Max.)**
- **Single 5V ± 10% Power Supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **— No clock or refresh required**
- **Three State Output**
- **Center Power/Ground Pin Configuration**
- **Standard Pin Configuration**
  KM68B1002J : 32-SOJ-400

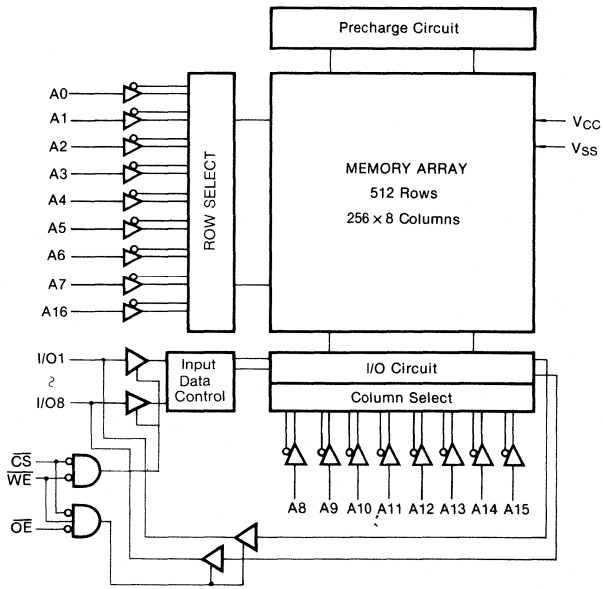
GENERAL DESCRIPTION

The KM68B1002 is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits.

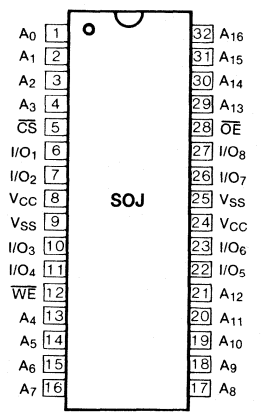
The KM68B1002 uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particulary well suited for use in high-density high-speed system applications.

The KM68B1002 is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS (Top View)



Pin Name	Pin Function
A_0-A_{16}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5**	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL} (min.) = −2.0V ac (pulse width ≤ 10ns) for I ≤ 20mA
** V_{IH} (max.) = V_{CC} + 2V ac (pulse width ≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Item	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		−2	+2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL}, $\overline{OE}$=V_{IH} V_{OUT}=V_{SS} to V_{CC}		−10	+10	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{OUT}=0mA V_{IN}=V_{IH}/V_{IL}	8ns	—	175	mA
			9ns	—	175	
			10ns	—	165	
			12ns	—	155	
			15ns	—	145	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, V_{IN}=V_{IH}/V_{IL}, Min. cycle		—	60	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC}-0.2V, f=0MHz V_{IN} ≤ 0.2V or V_{CC} ≥ V_{CC}-0.2V		—	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		—	0.4	V
Output High Voltage	I_{OH}	I_{OH}=−4mA		2.4	—	V

CAPACITANCE (f = 1MHz, T_A = 25°C)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	8	pF

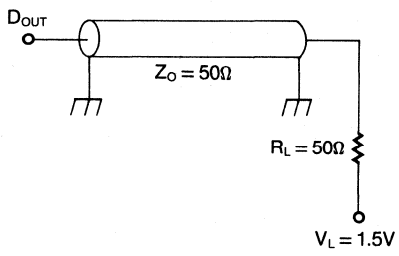
Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS

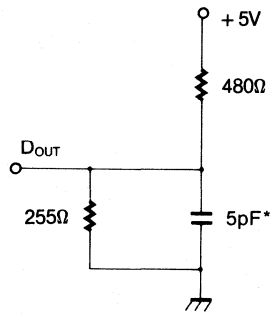
(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{OLZ}, t_{OHZ}, t_{HZ}, t_{LZ}, t_{OW} & t_{WZ})



* Including Scope and Jig Capacitance

READ CYCLE

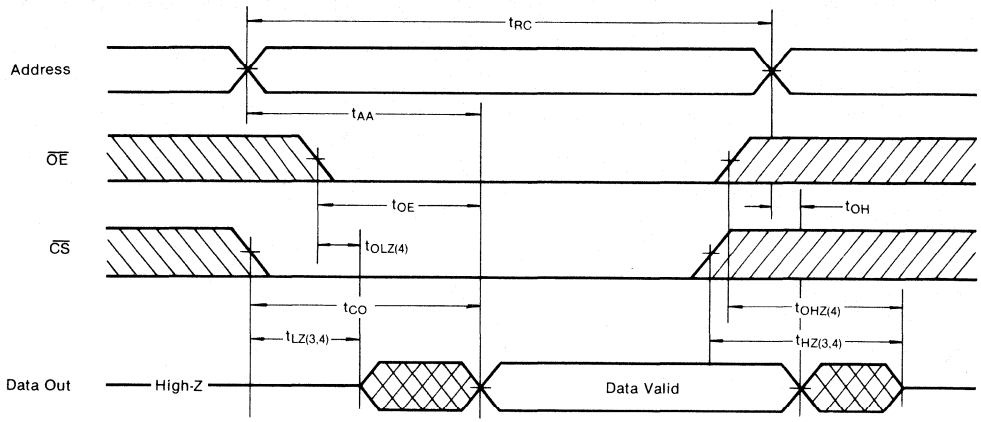
Parameter	Symbol	KM68B1002-8		KM68B1002-9		KM68B1002-10		KM68B1002-12		KM68B1002-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	8	-	9	-	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	8	-	9	-	10	-	12	-	15	ns
Chip Select to Output	t_{CO}	-	8	-	9	-	10	-	12	-	15	ns
Output Enable to Valid Output	t_{OE}	-	4	-	4	-	5	-	6	-	6	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	0	-	0	-	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	3	-	3	-	ns
Output Disable to High-Z Output	t_{OHZ}	-	4	-	4	-	5	-	6	-	6	ns
Chip Disable to High-Z Output	t_{HZ}	-	4	-	4	-	5	-	6	-	6	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM68B1002-8		KM68B1002-9		KM68B1002-10		KM68B1002-12		KM68B1002-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	8	-	9	-	10	-	12	-	15	-	ns
Chip Select to End of Write	t_{CW}	6	-	6	-	7	-	8	-	10	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	6	-	6	-	7	-	8	-	10	-	ns
Write Pulse Width ($\overline{OE}$ High)	t_{WP}	6	-	6	-	7	-	8	-	8	-	ns
Write Pulse Width ($\overline{OE}$ Low)	t_{WP}	8	-	8	-	9	-	10	-	10	-	ns
Write Recovery Time	t_{WR}	1	-	1	-	1	-	1	-	1	-	ns
Write to Output High-Z	t_{WZ}	-	4	-	4	-	5	-	6	-	6	ns
Data to Write Time Overlap	t_{DW}	4	-	4	-	5	-	6	-	7	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	3	-	3	-	ns

TIMING DIAGRAMS

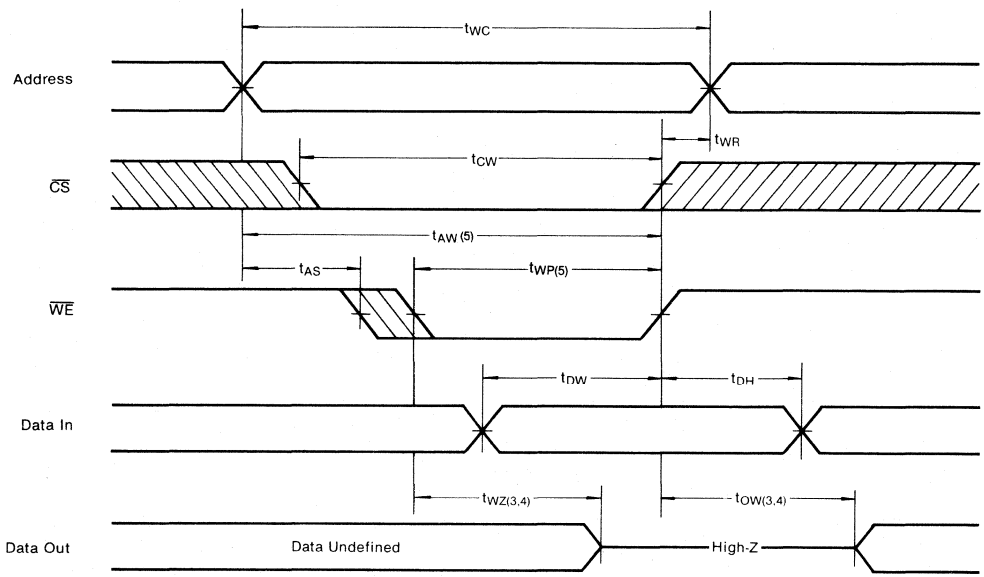
TIMING WAVEFORM OF READ CYCLE



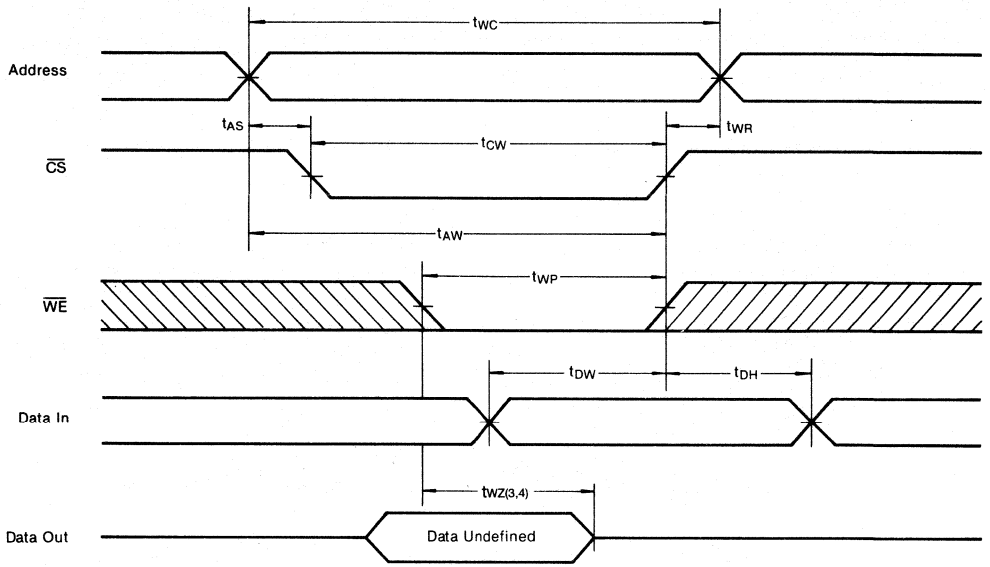
Notes (Read Cycle)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
4. Transition is measuled ±200mV from steady state voltage with Load (B).
   This parameter is sampled and not 100% tested.
5. For common I/O applications, minimization or elimination of bus contention conditions is neessary during read and write cycles.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (Write Cycle)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
5. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

*Note : X means Don't Care.

1,048,576 WORD x 4 Bit High-Speed BiCMOS Static RAM

FEATURES

- **Fast Access Time : 10ns, 12ns, 15ns**
- **Low Power Dissipation**
  Standby (TTL) : 60mA
  (CMOS) : 30mA
  Operating KM64B4002J-10 : 190mA(Max.)
  KM64B4002J-12 : 185mA(Max.)
  KM64B4002J-15 : 180mA(Max.)
- **Single 5V±10% power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - No clock or refresh required
- **Three state Output**
- **Standard Pin Configuration**
- **KM64B4002J : 32-SOJ-400**

GENERAL DESCRIPTION

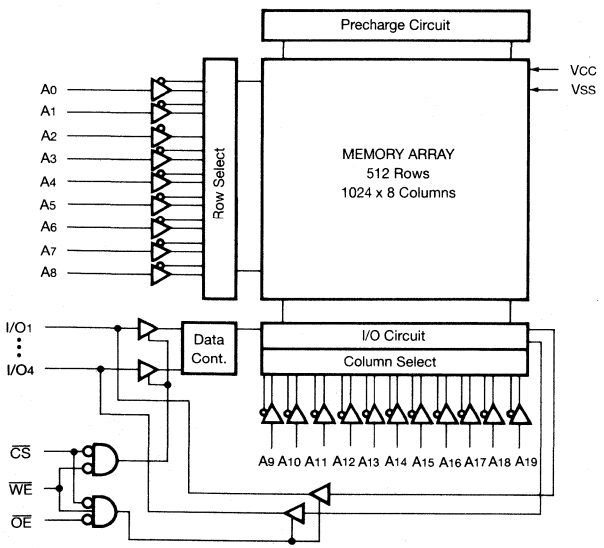
The KM64B4002 is a 4,194,304 bit high speed Static Random Access Memory organization as 1,048,576 words by 4-bits.

The KM64B4002 uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

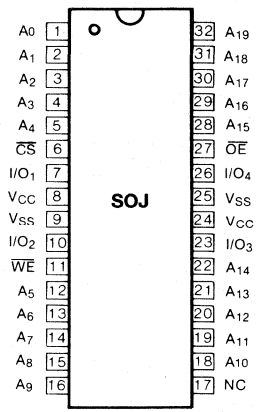
The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system application.

The KM64B4002 is packaged in a 400mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A19	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Input/Output
VCC	Power(+5V)
VSS	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5~7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5~7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	-65~150	°C
Operating Temperature	T_a	0~70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5**	V
Input Low Voltage	V_{IL}	-0.5*	—	0.8	V

* V_{IL}(min)=-2.0V AC (Pulse Width≤10ns) for 1≤20mA
** V_{IH}(max)=V_{CC}+2.0V AC (Pulse Width≤10ns) for 1≤20mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=V_{SS} to V_{CC}		-	10	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty	10ns	-	190	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0mA	12ns	-	185	
		$\overline{WE}$=V_{IL} or $\overline{WE}$=$\overline{OE}$=V_{IH}	15ns	-	180	
Standby Power SupplyCurrent	I_{SB}	$\overline{CS}$=V_{IH}, V_{IN}=V_{IH}/V_{IL}, Min Cycle		-	60	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, f=0MHz V_{IN}≤0.2V or V_{CC}≥V_{CC}-0.2V		-	30	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4mA		2.4	-	V

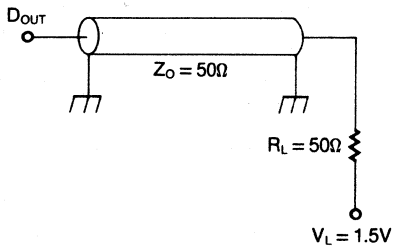
CAPACITANCE (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

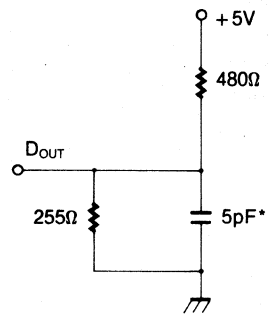
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{OLZ}, t_{OHZ}, t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including Scope and Jig Capacitance

READ CYCLE

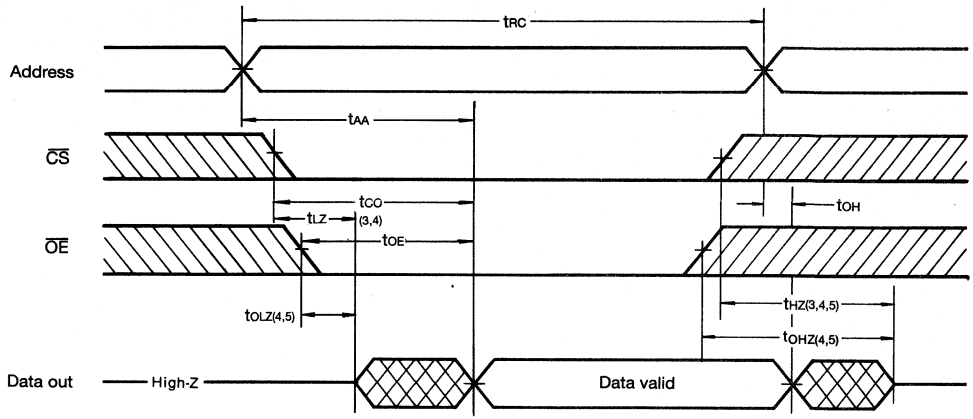
Parameter	Symbol	KM64B4002J-10		KM64B4002J-12		KM64B4002J-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	10	-	12	-	15	ns
Chip Select to Output	t_{CO}	-	10	-	12	-	15	ns
Output Enable to Output	t_{OE}	-	5	-	6	-	6	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Disable to High-Z Output	t_{OHZ}	-	5	-	6	-	6	ns
Chip Disable to High-Z Output	t_{HZ}	-	5	-	6	-	6	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM64B4002J-10		KM64B4002J-12		KM64B4002J-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	10	-	12	-	15	-	ns
Chip Select to End of Write	t_{CW}	7	-	8	-	10	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	7	-	8	-	10	-	ns
Write Pulse Width ($\overline{OE}$ High)	t_{WP}	7	-	8	-	10	-	ns
Write Pulse Width ($\overline{OE}$ Low)	t_{WP}	9	-	10	-	12	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WZ}	-	5	-	6	-	6	ns
Data to Write Time Overlap	t_{DW}	5	-	6	-	7	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

TIMING DIAGRAMS

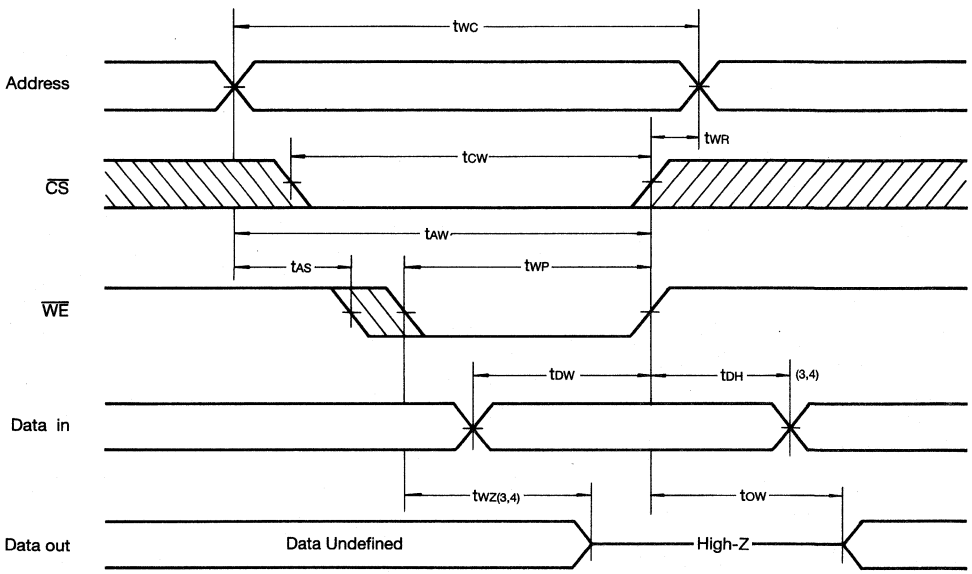
TIMING WAVEFORM OF READ CYCLE



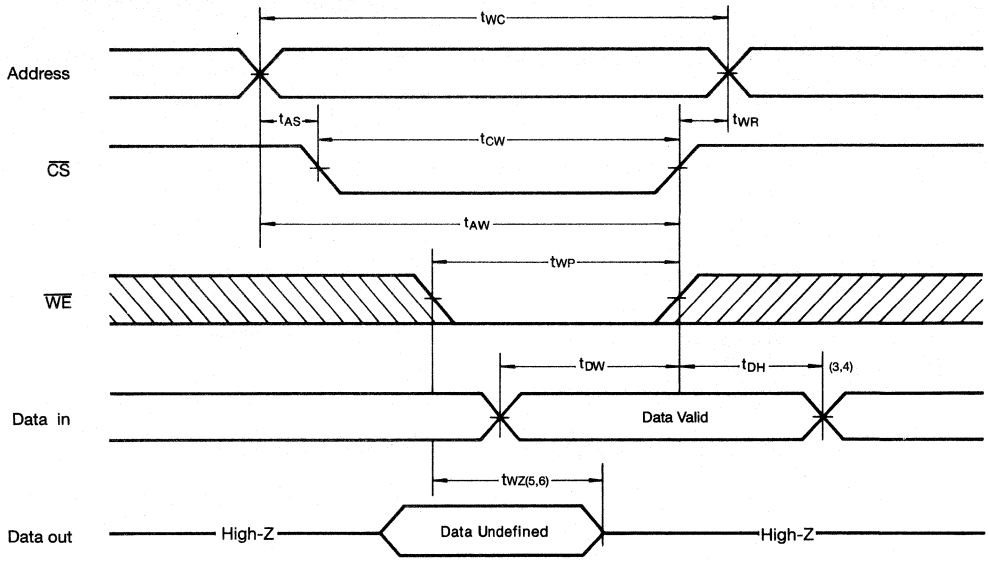
Note(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured NV00m V from steady state voltage with Load(B).
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=V_{IL}
7. Address valid prior to or coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE($\overline{CS}$ Controlled)



Note(WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS}$ and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
5. If $\overline{OE}$, $\overline{CS1}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the read data of the address.
8. When $\overline{CS}$ is low: I/O pins are in the output state. the input signals in the opposite phase leading to the output should not be applied.
9. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Note Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

*Note : X means Don't care

524,288 WORD x 8 Bit High-Speed BiCMOS Static RAM

FEATURES

- **Fast Access Time : 10ns, 12ns, 15ns**
- **Low Power Dissipation**
  Standby (TTL) : 60mA
  (CMOS) : 30mA
  Operating KM68B4002J-10 : 200mA(Max.)
  KM68B4002J-12 : 195mA(Max.)
  KM68B4002J-15 : 190mA(Max.)
- **Single 5V±10% power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - No clock or refresh required
- **Three state Outputs**
- **Standard Pin Configuration**
  KM68B4002J : 36-SOJ-400

GENERAL DESCRIPTION

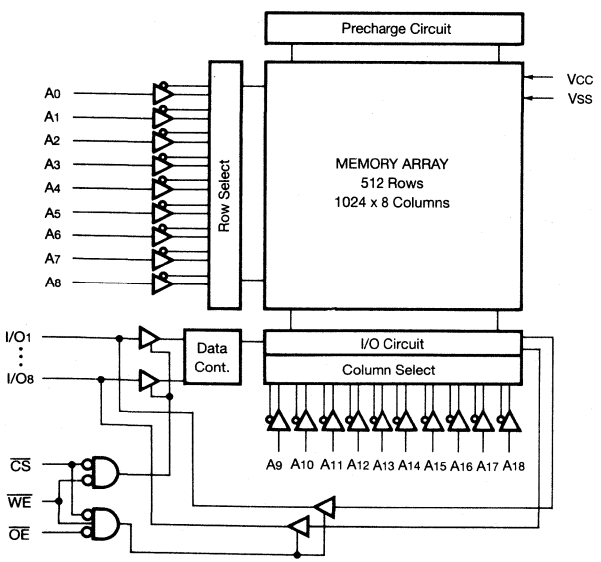
The KM68B4002 is a 4,194,304 bit high speed Static Random Access Memory organization as 524,288 words by 8-bits.

The KM68B4002 uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

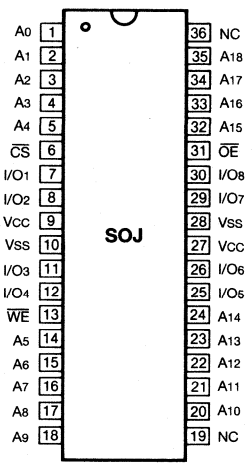
The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system application.

The KM68B4002 is packaged in a 400mil 36-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A18	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1~I/O8	Data Input/Output
VCC	Power(+5V)
VSS	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5~7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5~7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	-65~150	°C
Operating Temperature	T_a	0~70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5*	—	0.8	V

* V_{IL}(min=-2.0V AC (Pulse Width≤10ns) for I≤20mA

** V_{IH}(max=Vcc+2.0V AC (Pulse Width≤10ns) for I≤20mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, Vcc=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} V_{OUT}=Vss to Vcc		-	10	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty	10ns	-	200	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0mA	12ns	-	195	
		$\overline{WE}$=V_{IL} or $\overline{WE}$=$\overline{OE}$=V_{IH}	15ns	-	190	
Standby Power SupplyCurrent	I_{SB}	$\overline{CS}$=V_{IH}, V_{IN}=V_{IH}/V_{IL}, Min Cycle		-	60	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f=0MHz VIN≤0.2V or Vcc≥Vcc-0.2V		-	30	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4mA		2.4	-	V

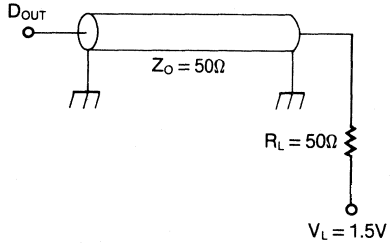
CAPACITANCE (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

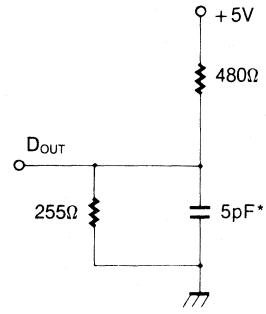
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{OLZ}, t_{OHZ}, t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68B4002J-10		KM68B4002J-12		KM68B4002J-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	10	-	12	-	15	ns
Chip Select to Output	t_{CO}	-	10	-	12	-	15	ns
Output Enable to Output	t_{OE}	-	5	-	6	-	6	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Disable to High-Z Output	t_{OHZ}	-	5	-	6	-	6	ns
Chip Disable to High-Z Output	t_{HZ}	-	5	-	6	-	6	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

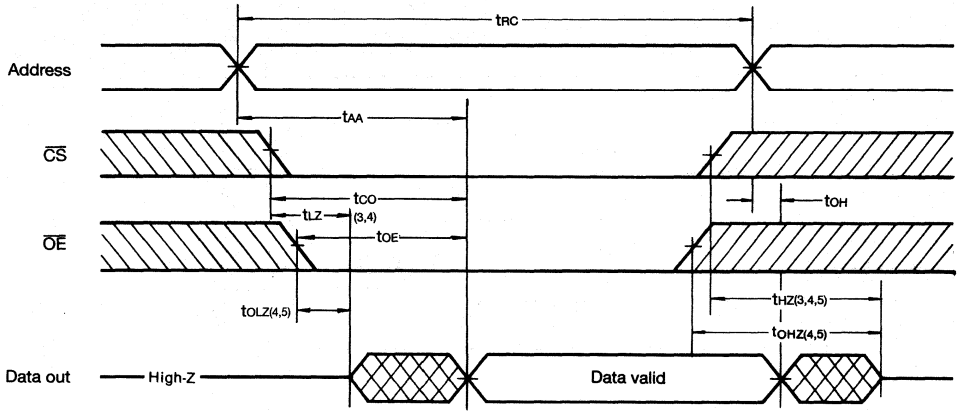
WRITE CYCLE

Parameter	Symbol	KM68B4002J-10		KM68B4002J-12		KM68B4002J-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	10	-	12	-	15	-	ns
Chip Select to End of Write	t_{CW}	7	-	8	-	10	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	7	-	8	-	10	-	ns
Write Pulse Width ($\overline{OE}$ High)	t_{WP}	7	-	8	-	10	-	ns
Write Pulse Width ($\overline{OE}$ Low)	t_{WP}	9	-	10	-	12	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WZ}	-	5	-	6	-	6	ns
Data to Write Time Overlap	t_{DW}	5	-	6	-	7	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

2

TIMING DIAGRAMS

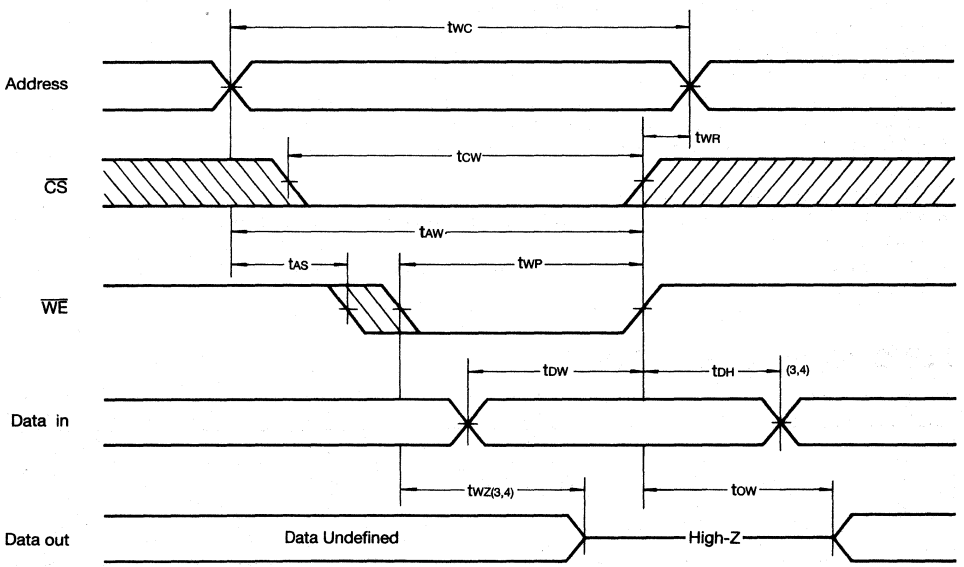
TIMING WAVEFORM OF READ CYCLE



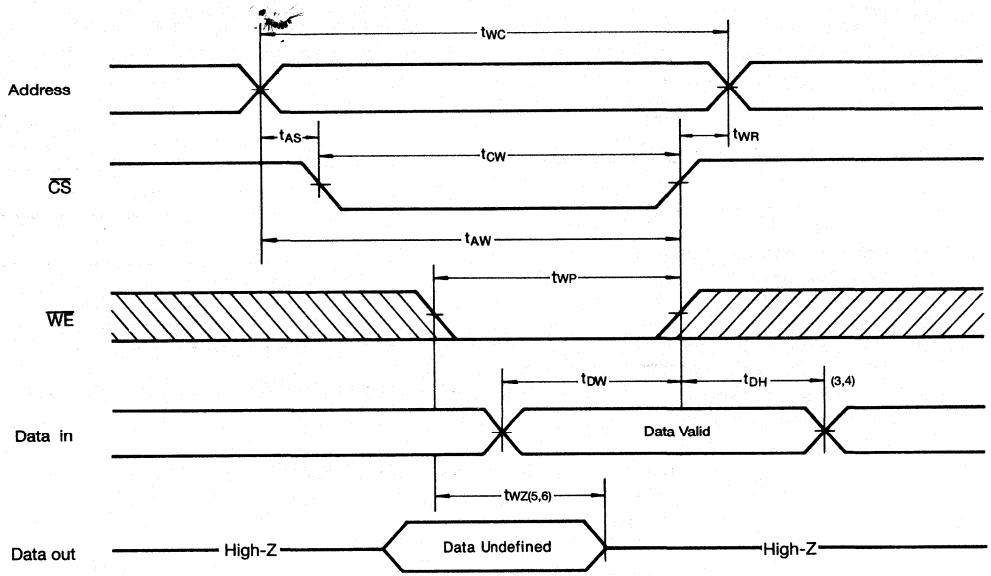
Note(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured NV00m V from steady state voltage with Load(B).
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=V_{IL}
7. Address valid prior to or coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE($\overline{CS}$ Controlled)



Note(WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS}$ and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
5. If $\overline{OE}$, $\overline{CS1}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the read data of the address.
8. When $\overline{CS}$ is low: I/O pins are in the output state. the input signals in the opposite phase leading to the output should not be applied.
9. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Note Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

*Note : X means Don't care

262,144 WORD x 16 Bit High-Speed BiCMOS Static RAM

FEATURES

- **Fast Access Time : 10ns, 12ns, 15ns**
- **Low Power Dissipation**
  Standby (TTL) : 60mA
  (CMOS) : 30mA
  Operating KM616B4002J-10 : 280mA(Max.)
  KM616B4002J-12 : 270mA(Max.)
  KM616B4002J-15 : 260mA(Max.)
- **Single 5V±10% power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - No clock or refresh required
- **Three state Output**
- **Data Byte Control : $\overline{LB}$: I/O1~I/O8**
  $\overline{UB}$: I/O9~I/O16
- **Standard Pin Configuration**
- **KM616B4002J : 44-SOJ-400**

GENERAL DESCRIPTION

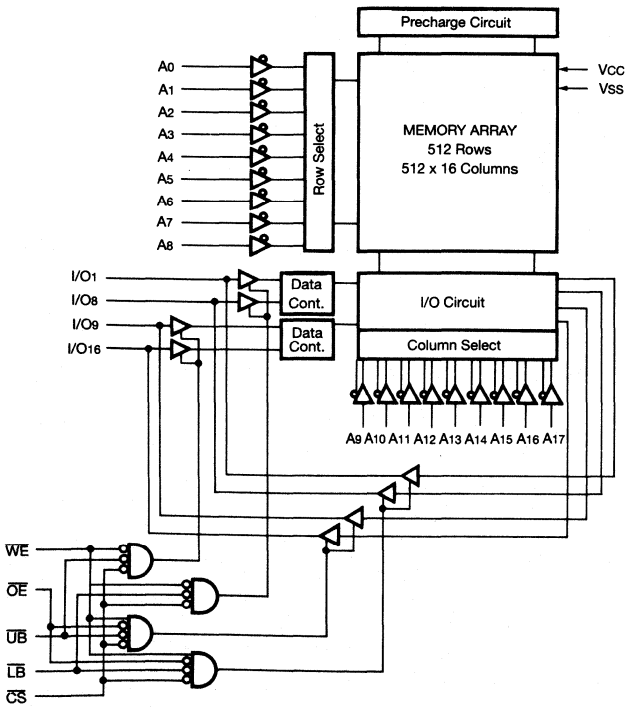
The KM616B4002 is a 4,194,304 bit high-speed Static Random Access Memory organization as 262,144 words by 16-bits.

The KM616B4002 uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control($\overline{LB}$,$\overline{UB}$).

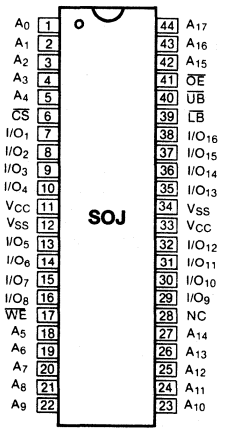
The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system application.

The KM616B4002 is packaged in a 400mil 44-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(IO1~I/O8)
$\overline{UB}$	Upper-byte Control(IO9~I/O16)
I/O1~I/O16	Data Input/Output
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5~7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5~7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	-65~150	°C
Operating Temperature	T_a	0~70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5**	V
Input Low Voltage	V_{IL}	-0.5*	—	0.8	V

* V_{IL}(min=-2.0V AC (Pulse Width≤10ns) for I≤20mA
** V_{IH}(max=V_{CC}+2.0V AC (Pulse Width≤10ns) for I≤20mA

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} V_{OUT}=V_{SS} to V_{CC}		-	10	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty	10ns	-	280	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0mA	12ns	-	270	
		$\overline{WE}$=V_{IL} or $\overline{WE}$=$\overline{OE}$=V_{IH}	15ns	-	260	
Standby Power SupplyCurrent	I_{SB}	$\overline{CS}$=V_{IH}, V_{IN}=V_{IH}/V_{IL}, Min Cycle		-	60	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, f=0MHz VIN≤0.2V or V_{CC}≥V_{CC}-0.2V		-	30	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4mA		2.4	-	V

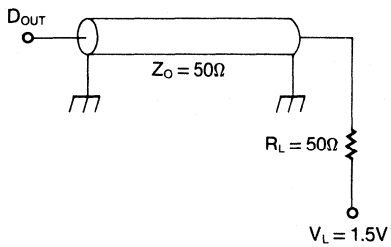
CAPACITANCE (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

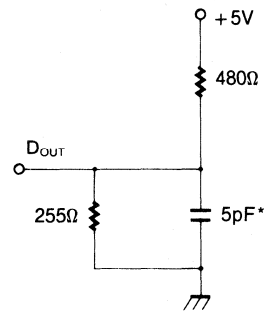
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{OLZ}, t_{OHZ}, t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including Scope and Jig Capacitance

READ CYCLE

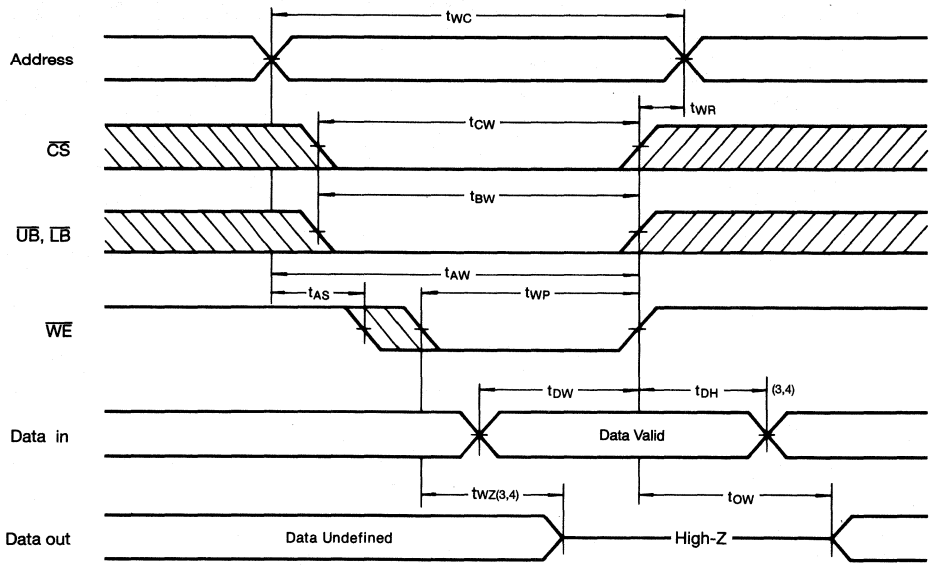
Parameter	Symbol	KM616B4002J-10		KM616B4002J-12		KM616B4002J-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	10	-	12	-	15	ns
Chip Select to Output	t_{CO}	-	10	-	12	-	15	ns
Output Enable to Output	t_{OE}	-	5	-	6	-	6	ns
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}	-	5	-	6	-	6	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
$\overline{LB}$, $\overline{UB}$ Enable to Low-Z Output	t_{BLZ}	0	-	0	-	0	-	ns
Output Disable to High-Z Output	t_{OHZ}	-	5	-	6	-	6	ns
Chip Disable to High-Z Output	t_{HZ}	-	5	-	6	-	6	ns
$\overline{LB}$, $\overline{UB}$ Disable to High-z Output	t_{BHZ}	-	5	-	6	-	6	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

WRITE CYCLE

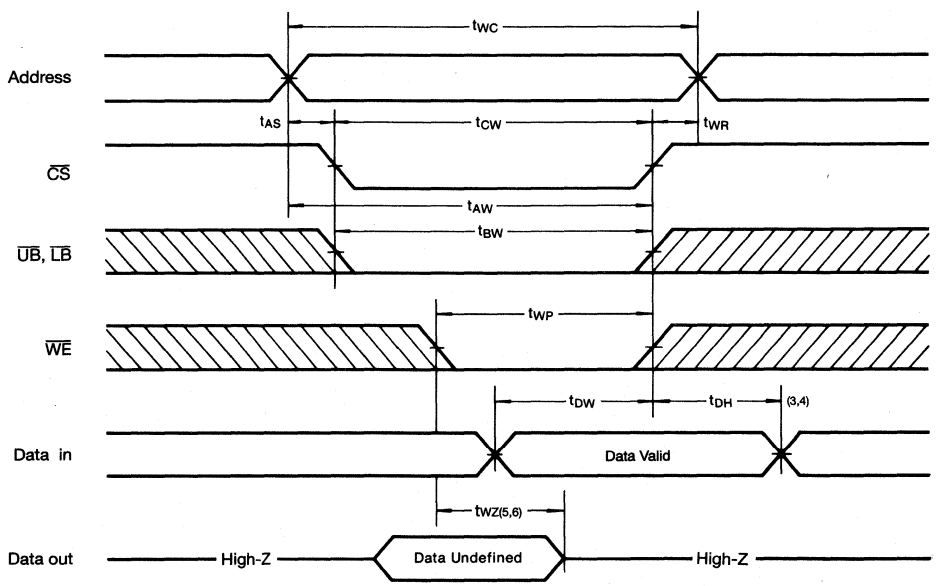
Parameter	Symbol	KM616B4002J-10		KM616B4002J-12		KM616B4002J-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	10	-	12	-	15	-	ns
Chip Select to End of Write	t_{CW}	7	-	8	-	10	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	7	-	8	-	10	-	ns
Write Pulse Width ($\overline{OE}$ High)	t_{WP}	7	-	8	-	10	-	ns
Write Pulse Width ($\overline{OE}$ Low)	t_{WP}	9	-	10	-	12	-	ns
$\overline{LB}$, $\overline{UB}$ Valid to End write	t_{BW}	7	-	8	-	10	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WZ}	-	5	-	6	-	6	ns
Data to Write Time Overlap	t_{DW}	5	-	6	-	7	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

TIMING DIAGRAMS

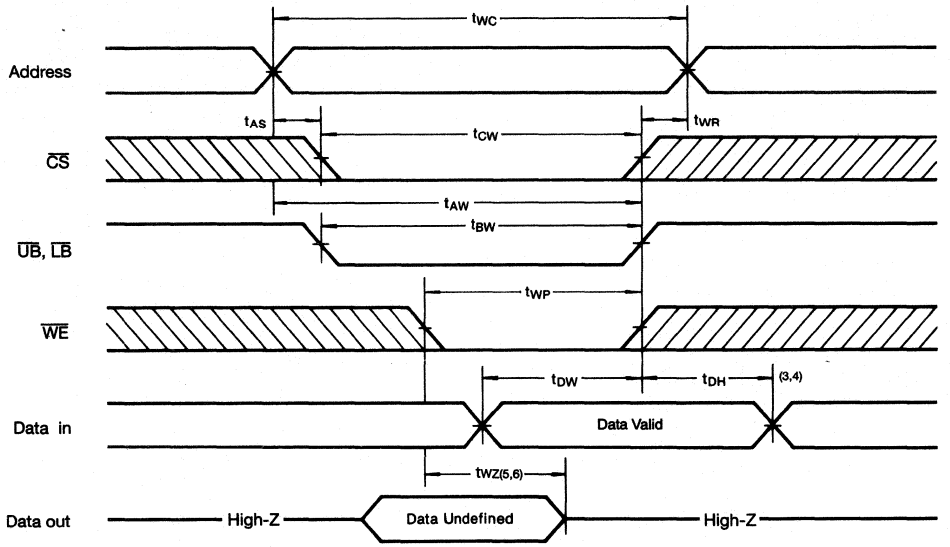
TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{UB}$,$\overline{LB}$ Controlled)



Note(WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS}$ and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
5. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the read data of the address.
8. When $\overline{CS}$ is low: I/O pins are in the output state. the input signals in the opposite phase leading to the output should not be applied.
9. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O_1~I/O_8	I/O_9~I/O_{16}	
H	X*	X	X	X	Not Select	High-Z	High-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

*Note : X means Don't care

1,048, 576 WORD x 4 Bit High-Speed BiCMOS Static RAM 3.3V Operating

FEATURES

- **Fast Access Time : 12, 15, 20ns(Max.)**
- **Low Power Dissipation**
  Standby (TTL) : 60mA(Max.)
  (CMOS) : 30mA(Max.)
  Operating KM64BV4002J-12 : 155mA(Max.)
  KM64BV4002J-15 : 150mA(Max.)
  KM64BV4002J-20 : 145mA(Max.)
- **Single 3.3V±0.3V power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - No clock or refresh required
- **Three state Output**
- **Standard Pin Configuration**
  KM64BV4002J : 32-SOJ -400

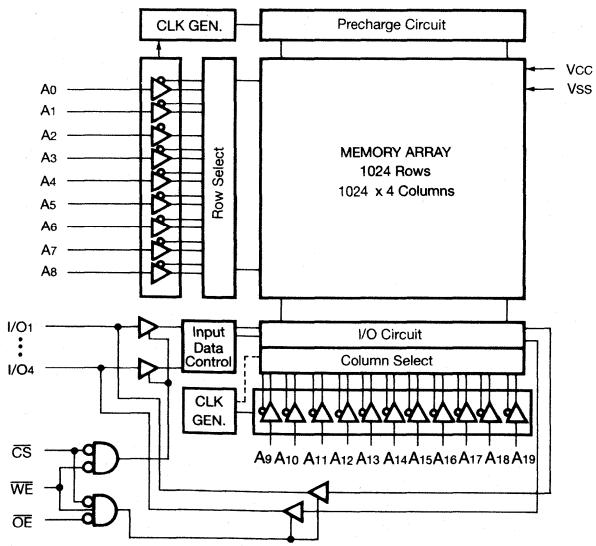
GENERAL DESCRIPTION

The KM64BV4002 is a 4,194,304 bit high speed Static Random Access Memory organization as 1,048,576 words by 4-bits.

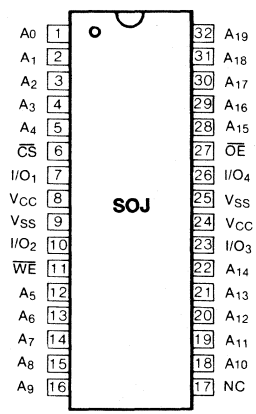
The KM64BV4002 uses four common inputs and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system application.

The KM64BV4002 is packaged in a 400mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A19	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1~I/O4	Data Input/Output
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection

524,288 WORD x 8 Bit High-Speed BiCMOS Static RAM 3.3V Operating

FEATURES

- **Fast Access Time : 12, 15, 20ns(Max.)**
- **Low Power Dissipation**
  Standby (TTL) : 60mA(Max.)
  (CMOS) : 30mA(Max.)
  Operating KM68BV4002J-12 : 165mA(Max.)
  KM68BV4002J-15 : 160mA(Max.)
  KM68BV4002J-20 : 155mA(Max.)
- **Single 3.3V±0.3V power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - No clock or refresh required
- **Three state Output**
- **Standard Pin Configuration**
  KM68BV4002J : 36-SOJ -400

GENERAL DESCRIPTION

The KM68BV4002 is a 4,194,304 bit high-speed Static Random Access Memory organization as 524,288 words by 8-bits.
The KM68BV4002 uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high density high speed system application.
The KM68BV4002 is packaged in a 400mil 36-pin plastic SOJ.

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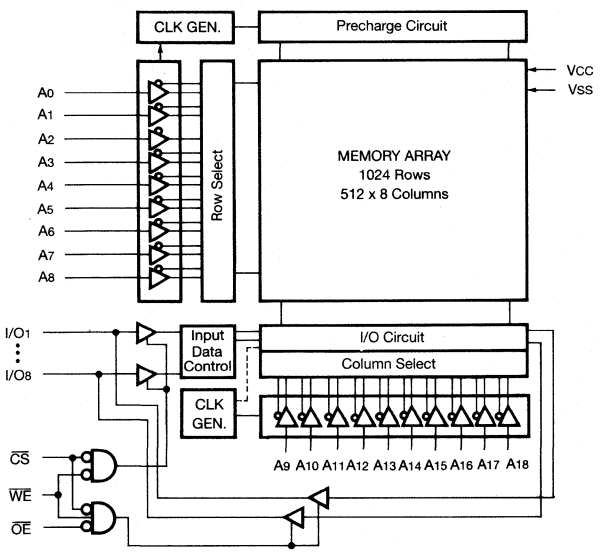
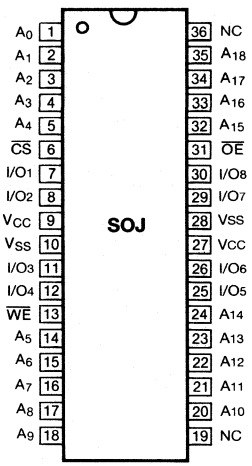
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A18	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1~I/O8	Data Input/Output
VCC	Power(+3.3V)
VSS	Ground
NC	No Connection

262,144 WORD x 16 Bit High-Speed BiCMOS Static RAM

FEATURES

- **Fast Access Time : 12, 15, 20ns(Max.)**
- **Low Power Dissipation**
  Standby (TTL) : 60mA(Max.)
  (CMOS) : 30mA(Max.)
  Operating KM616BV4002J-12 : 175mA(Max.)
  KM616BV4002J-15 : 160mA(Max.)
  KM616BV4002J-20 : 155mA(Max.)
- **Single 3.3V±0.3V power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - No clock or refresh required
- **Three state Output**
- **Data Byte Control : $\overline{LB}$: I/O1~I/O8**
  $\overline{UB}$: I/O9~I/O16
- **Standard Pin Configuration : 44-SOJ-400**

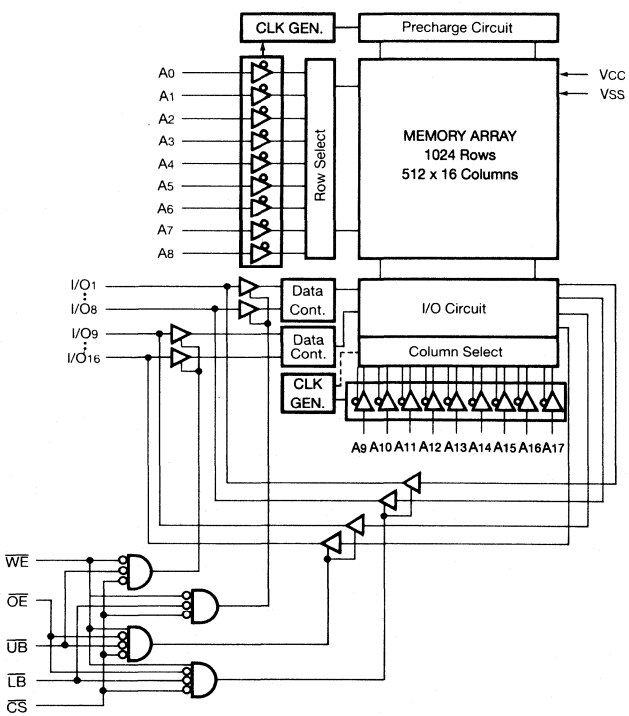
GENERAL DESCRIPTION

The KM616BV4002 is a 4,194,304 bit high speed Static Random Access Memory organization as 262,144 words by 16-bits.

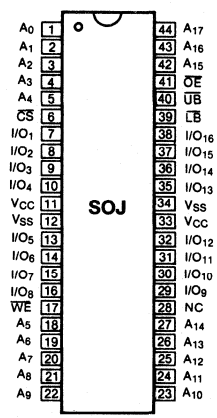
The KM616BV4002 uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control($\overline{LB}$,$\overline{UB}$).The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology.
The KM616B4002 is designed to operate at 3.3 volts. It is particularly well suited for use in high-density high-speed system application.

The KM616BV4002 is packaged in a 400mil 44-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



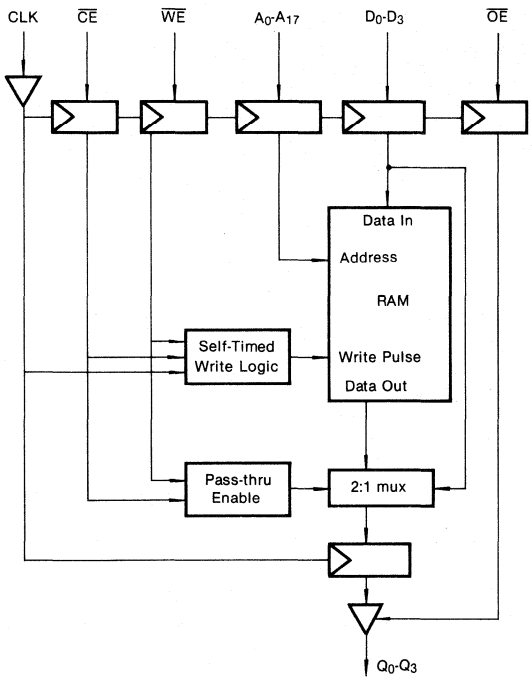
Pin Name	Pin Function
A0-A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(IO1~I/O8)
$\overline{UB}$	Upper-byte Control(IO9~I/O16)
I/O1~I/O16	Data Input/Output
VCC	Power(+3.3V)
VSS	Ground
NC	No Connection

262,144 Words x 4-Bit Synchronous Static Random Access Memory

FEATURES

- **Fast Cycle Time: 10, 12.5, 15ns (Max.)**
- **Low Power Dissipation**
  - **KM741006J-10: 190mA (Max.)**
  - **KM741006J-12: 180mA (Max.)**
  - **KM741006J-15: 150mA (Max.)**
- **Single 5V ± 5% Power Supply**
- **TTL compatible inputs and outputs**
- **All Inputs and Outputs Registered with Clock**
- **Three State Outputs**
- **Available in Plastic 36 Pin 400mil SOJ**

FUNCTIONAL BLOCK DIAGRAM



Pin Name	Timing Reference	Pin Function
A_0-A_{17}	A	Address Input
$\overline{WE}$	W	Write Enable Input
$\overline{CE}$	E	Chip Enable Input
$\overline{OE}$	G	Output Enable Input
D_0-D_3	D	Data Input
Q_0-Q_3	Q	Data Output
CLK	C	Clock Input
V_{CC}	—	+5V Power Supply
V_{SS}	—	Ground
NC	—	No Connection

GENERAL DESCRIPTION

The KM741006J is a 1,048,576 bit synchronous high-speed SRAM organized as a 262,144 words by 4 bits. The device integrates a 256K x 4 bits SRAM core with advanced synchronous peripheral circuitry, which includes input registers, output registers, address registers and control registers.

All signals pass thru registers triggered by a positive-edge of clock input(K).

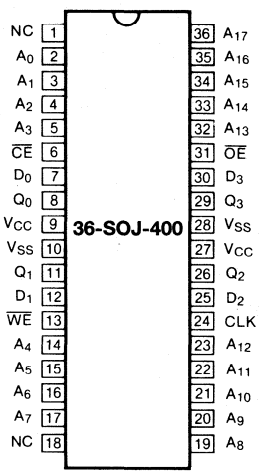
In read operation, the data of cell array accessed by the current address, registered in the address registers by the positive edge of K, are carried to the Data-out registers by the next positive edge of K. The data, registered in the Data-out registers, are projected to the output pins.

In write operation, the write data, registered in the Data-in registers, are stored in both the cell array and the Data-out registeres.

This operation is fully self-timed and exclude the complexity of the write control of general SRAM. Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$.

Note that this device does not need any intervening recovery cycles in a sequential operation of arbitrary read, write, and pass-thru cycles.

PIN CONFIGURATIONS (Top View)



ABSOLUTE MAXIMUM RATINGS* (T_A = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	-0.5 to 7.0	V
Input Voltage	V_{IN}	-0.5 to 7.0	V
Allowable Power Dissipation	P_D	1.0	W
Operating Temperature	T_{OPR}	0 to 70	°C
Storage Temperature	T_{STG}	-55 to 150	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0 to 70°C, GND = 0V)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input High Voltage	V_{IH}	2.20	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.80	V

* V_{IL} = −1V Min, for 3ns per cycle.

ELECTRICAL DC AND OPERATING CHARACTERISTICS

(V_{CC} = 5V ± 5%, GND = 0V, T_A = 0 to 70°C)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = GND to V_{CC}		−2	+2	μA
Output Leakage Current	I_{LO}	$V_{I/O}$ = GND to V_{CC}, $\overline{OE}$ = V_{IH}		−2	+2	μA
Average Operating Current	I_{CC}	Cycle = Min, Duty = 100%, I_{OUT} = 0mA	10ns	—	190	mA
			12.5ns	—	180	mA
			15ns	—	150	mA
Standby Current	I_{SB}	$\overline{CE}$ = $\overline{WE}$ = $\overline{OE}$ = V_{IH} V_{IN} = V_{IH} or V_{IL}		—	40	mA
Output High Voltage	V_{OH}	I_{OH} = −4.0mA		2.4	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		—	0.4	V

TRUTH TABLES

CLK	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Operation
↑	H	H	H	Outputs High-Z, deselect operation
↑	H	H	L	Store D_0 to D_3 in Output Registers, Outputs High-Z
↑	H	L	H	Read from Output Registers
↑	H	L	L	Pass-thru
↑	L	L	H	Read Q_0 to Q_3
↑	L	H	H	Store Q_0 to Q_3 in Output Registers, Outputs High-Z
↑	L	H	L	Write D_0 to D_3 and store in Output Registers, Output High-Z
↑	L	L	L	Write D_0 to D_3 and pass-thru

I/O CAPACITANCE ($T_A = 25°C$, f = 1MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	5	pF
Clock Input Capacitance	C_{CLK}	$V_{IN} = 0V$	—	8	pF
Output Capacitance	C_O	$V_O = 0V$	—	8	pF

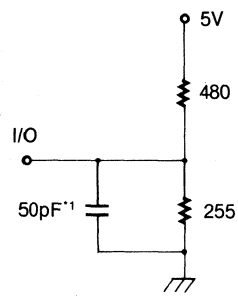
Note: This parameter is sampled and not 100% tested.

AC CHARACTERISTICS
TEST CONDITIONS

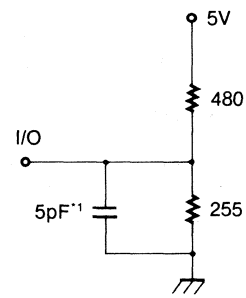
($V_{CC} = 5V \pm 5\%$, $T_A = 0$ to $+70°C$)

Item	Conditions
Input Pulse High Level	$V_{IH} = 3.0V$
Input Pulse Low Level	$V_{IL} = 0V$
Input Rise Time	$t_R = 3.0ns$
Input Fall Time	$t_F = 3.0ns$
Input Reference Level	1.5V
Output Reference Level, V_{OH}/V_{OL}	2.0/0.8V
Output Load (See test circuit in the right)	Fig. 1

Output Load (1)



Output Load (2)*2



*1 including scope and jig capacitance
*2 for T_{CHQHZ}, T_{CHQLZ}

Fig. 1

READ CYCLE

Item	Symbol	KM741006J-10		KM741006J-12		KM741006J-15		Unit
		Min	Max	Min	Max	Min	Max	
Clock Cycle Time	t_{CHCH}	10	—	12.5	—	15	—	ns
Clock High Pulse Width	t_{CH}	4.0	—	4.0	—	5.0	—	ns
Clock Low Pulse Width	t_{CL}	4.0	—	4.0	—	5.0	—	ns
Clock High to Data Valid	t_{CHQV}	2.0	6.5	2.0	7	2.0	8	ns
Address Setup to Clock High	t_{AVCH}	2.0	—	2.0	—	2.5	—	ns
Address Hold from Clock High	t_{CHAX}	1.0	—	1.0	—	1.5	—	ns
Chip Enable Setup to Clock High	t_{EVCH}	2.0	—	2.0	—	2.5	—	ns
Chip Enable Hold from Clock High	t_{CHEX}	1.0	—	1.0	—	1.5	—	ns
Write Enable Setup to Clock High	t_{WVCH}	2.0	—	2.0	—	2.5	—	ns
Write Enable Hold from Clock High	t_{CHWX}	1.0	—	1.0	—	1.5	—	ns
Output Enable Setup to Clock High	t_{GVCH}	2.0	—	2.0	—	2.5	—	ns
Output Enable Hold from Clock High	t_{CHGX}	1.0	—	1.0	—	1.5	—	ns
Output Hold from Clock High	t_{CHQX}	2.0	—	2.0	—	2.5	—	ns
*Clock High to Output Low-Z	t_{CHQLZ}	2.0	6.5	2.0	7	2.0	8	ns
*Clock High to Output High-Z	t_{CHQHZ}	2.0	10	2.0	10	2.0	10	ns

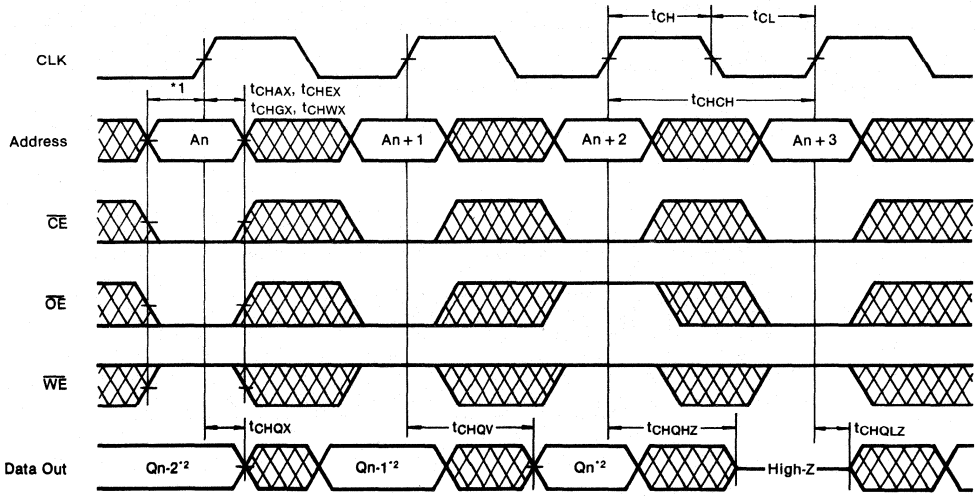
*Transition is measured ±200mW from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and not 100% tested.

WRITE CYCLE

Parameter	Symbol	KM741006J-10		KM741006J-12		KM741006J-15		Unit
		Min	Max	Min	Max	Min	Max	
Clock Cycle Time	t_{CHCH}	10	—	12.5	—	15	—	ns
Clock High Pulse Width	t_{CH}	4.0	—	4.0	—	5.0	—	ns
Clock Low Pulse Width	t_{CL}	4.0	—	4.0	—	5.0	—	ns
Address Set-up to Clock High	t_{AVCH}	2.0	—	2.0	—	2.5	—	ns
Address Hold from Clock High	t_{CHAX}	1.0	—	1.0	—	1.5	—	ns
Chip Enable Setup to Clock High	t_{EVCH}	2.0	—	2.0	—	2.5	—	ns
Chip Enable Hold from Clock High	t_{CHEX}	1.0	—	1.0	—	1.5	—	ns
Write Enable Setup to Clock High	t_{WVCH}	2.0	—	2.0	—	2.5	—	ns
Write Enable Hold from Clock High	t_{CHWX}	1.0	—	1.0	—	1.5	—	ns
Input Data Setup to Clock High	t_{DVCH}	2.0	—	2.0	—	2.5	—	ns
Input Data Hold from Clock High	t_{CHDX}	1.0	—	1.0	—	1.5	—	ns

TIMING WAVEFORM

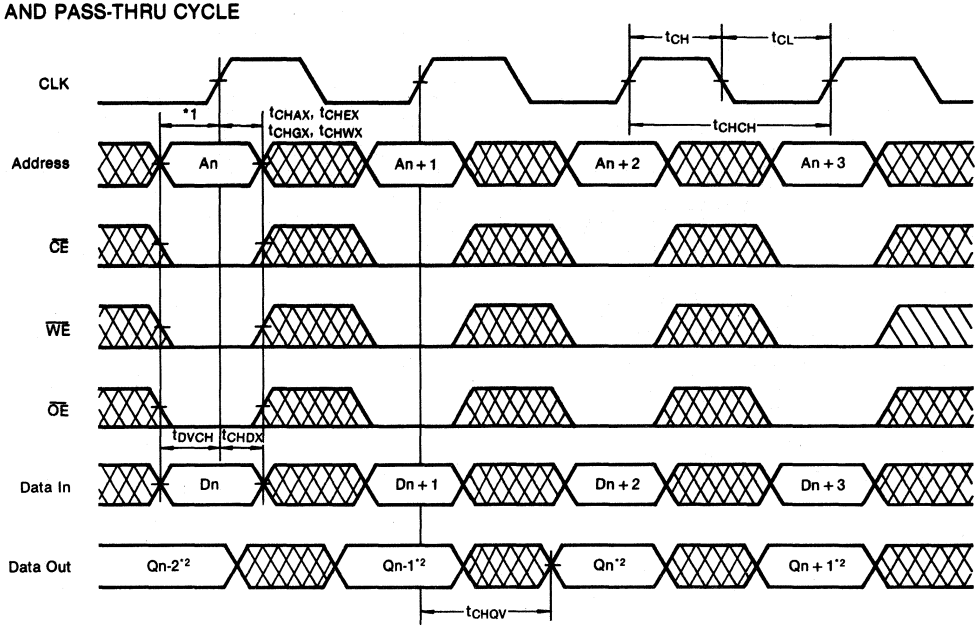
READ CYCLE:



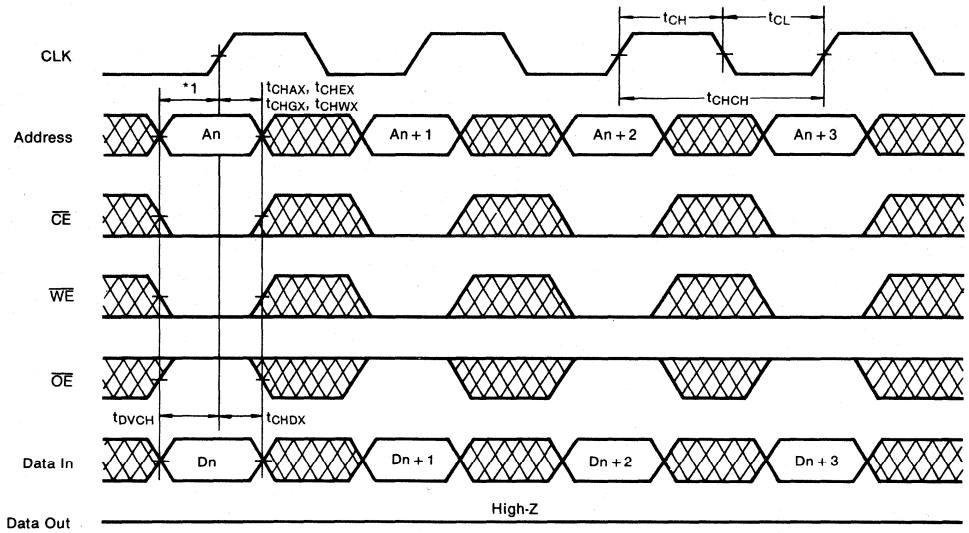
*1 : tAVCH, tEVCH, tGVCH, tWVCH

*2 : Valid data from CLK high is the data from the previous cycle.

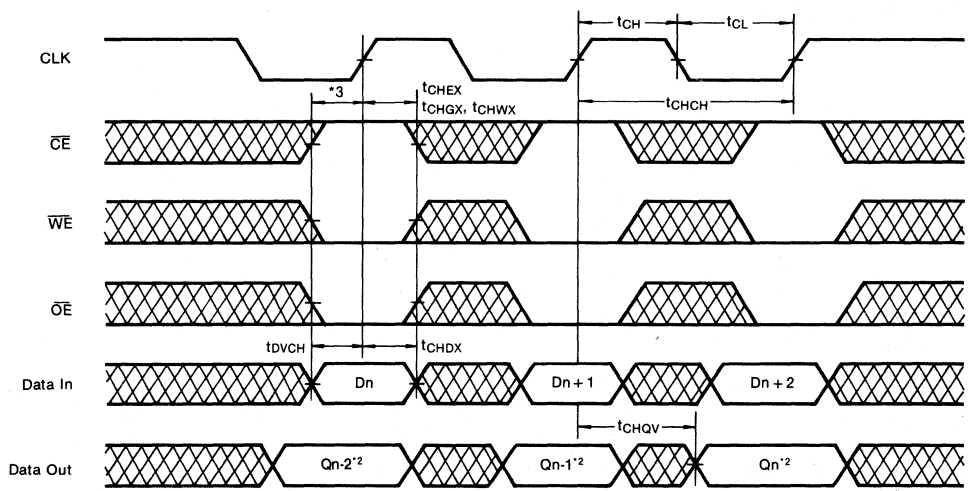
WRITE AND PASS-THRU CYCLE



WRITE CYCLE



PASS-THRU CYCLE



* 1 t_{AVCH}, t_{EVCH}, t_{GVCH}, t_{WVCH}
* 2 Valid data from CLK high is the data from the previous cycle
* 3 t_{EVCH}, t_{WVCH}, t_{GVCH}

64K x 18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On- Chip Address and Control Registers.
- Single 5V±5% Power Supply.
- Byte Writable Function.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$,$\overline{ADSC}$,$\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Outputs.
- 3.3V I/O Compatible.
- 52-Pin PLCC Package.

FAST ACCESS TIMES

Parameter	Symbol	-9	-10	-12	Unit
Cycle Time	tCYC	15	17	20	ns
Clock Access Time	tCD	9	10	12	ns
Output Enable Access Time	tOE	5	5	6	ns

GENERAL DESCRIPTION

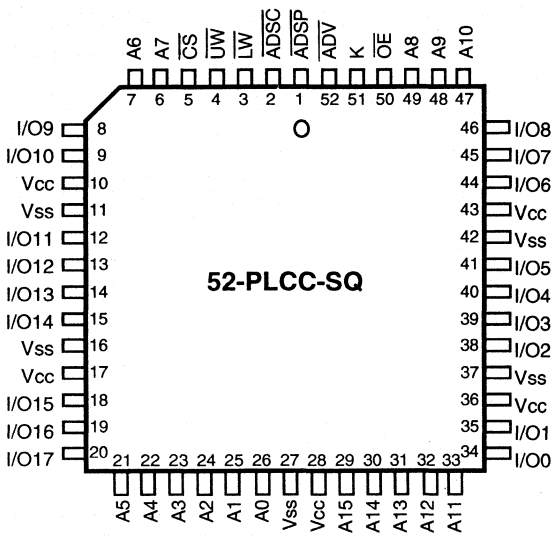
The KM718B86 is a 1,179,648 bit Synchronous Static Random Access Memory designed to support 66MHz of Intel secondary caches. It is organized as 65,536 words of 18 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced component count implementations of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous. The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Bursts can be initiated with either the address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance ($\overline{ADV}$) input.

The KM718B86 is implemented in Samsung's high performance BiCMOS technology and is available in a 52 pin PLCC package. Multiple power and ground pins are utilized to minimize ground bounce

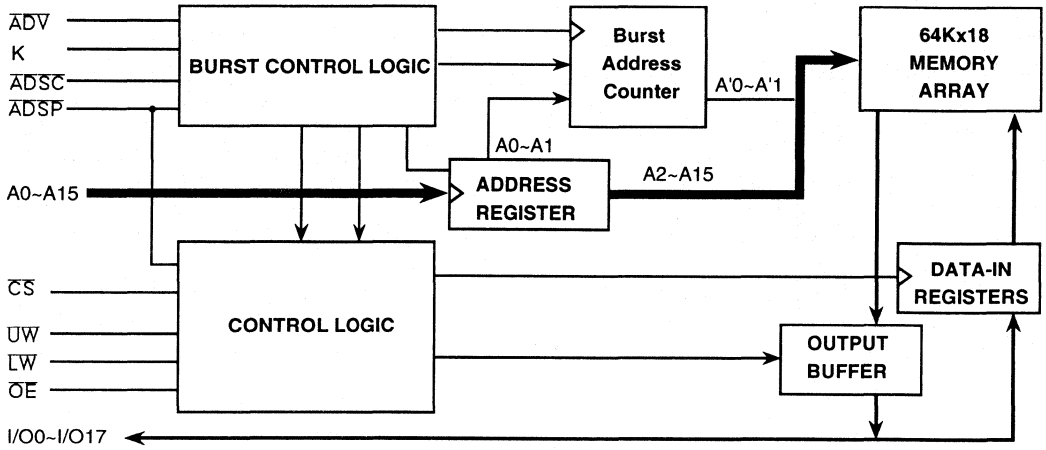
PIN CONFIGURATION(*Top View*)



PIN DESCRIPTION

Pin Name	Pin Function
A0~A15	Address Inputs
K	Clock
$\overline{LW}$,$\overline{UW}$	Write Enable
$\overline{CS}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{ADV}$	Burst Address Advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status
I/O0~I/O17	Data Inputs/Outputs
Vcc	+5V Power Supply
Vss	Ground

LOGIC BLOCK DIAGRAM



FUNCTION DESCRIPTION

The KM718B86 is a synchronous SRAM designed to support the burst address accessing sequence of the i486/586 microprocessor. All inputs (with the exception of $\overline{OE}$) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$ and $\overline{ADSP}$. The accesses are enabled with the chip select signals and output enable. Wait states are inserted into the access with $\overline{ADV}$.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{LW}$,$\overline{UW}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the next and subsequent clock edges. The address is incremented internally for the next access of the burst when $\overline{LW}$,$\overline{UW}$ is sampled HIGH and $\overline{ADV}$ is sampled low.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{LW}$,$\overline{UW}$. $\overline{LW}$,$\overline{UW}$ is ignored on the clock edge that samples $\overline{ADSP}$ low, but is sampled on the next and subsequent clock edges. The output buffers are disabled when $\overline{LW}$,$\overline{UW}$ is sampled low (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{LW}$,$\overline{UW}$ is sampled low. The address is incremented internally to the next address of burst if both $\overline{LW}$,$\overline{UW}$ and $\overline{ADV}$ are sampled low. Individual byte write cycles are performed by sampling low only one byte write signal ($\overline{LW}$ or $\overline{UW}$), and $\overline{LW}$ controls I/O0 - I/O7 and $\overline{UW}$ controls I/O8 - I/O17.
Read or write cycles (depending on $\overline{LW}$,$\overline{UW}$) may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ are as follows;

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{LW}$,$\overline{UW}$ is sampled on the same clock edge that samples $\overline{ADSC}$ low (and $\overline{ADSP}$ high).

Address are generated for the burst accesses as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

BURST SEQUENCE TABLE

	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	0	0	1	1	1	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{LW}$/$\overline{UW}$	K	Address Accessed	Operation
H	L	X	X	X	↑	N/A	Not Selected
H	X	L	X	X	↑	N/A	Not Selected
L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE 1 : X means "Don't Care"
NOTE 2 : The rising edge of clock is symbolized by ↑

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{OE}$	Operation
L	Read I/O0~I/O17
H	Outputs High-Z
X	Not Selected, Outputs High-Z

NOTE 1 : X means "Don't Care"
NOTE 2 : For write cycles that follow read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.5 to 7.0	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to +150	°C
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to +85	°C

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc	4.75	5.0	5.25	V
Ground	Vss	0	0	0	V

CAPACITANCE* (T_A=25°C, f=1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	8	pF

***NOTE** : Sampled not 100% tested.

TEST CONDITIONS (T_A=0°C to 70°C, Vcc=5V±5%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS (Vcc=5V±5%, T_A=0°C to +70°C)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	Iil	Vcc=Max; V_{IN}=Vss to Vcc		-2	+2	μA
Output Leakage Current	Iol	Output Disabled		-2	+2	μA
Operating Current	Icc	Vcc=Max	15ns	-	250	mA
		I_{OUT}=0mA	17ns	-	240	
		Cycle Time ≥ tCYC min	20ns	-	220	
Standby Current	Isb	$\overline{CS}$=V_{IH}, I_{OUT}=0mA, Min Cycle		-	80	mA
Output Low Voltage	Vol	Iol=8.0mA		-	0.4	V
Output High Voltage	Voh	Ioh=-4.0mA		2.4	3.3	V
Input Low Voltage	Vil			-0.5*	0.8	V
Input High Voltage	Vih			2.2	Vcc+0.5	V

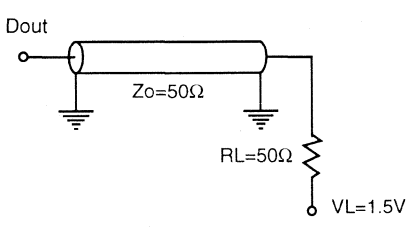
* Vil(min)=-3.0 (Pulse Width ≤20ns)

AC TIMING CHARACTERISTICS (Vcc=5V±5%, TA=0°C to +70°C)

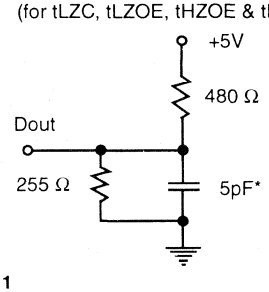
Parameter	Symbol	KM718B86-9		KM718B86-10		KM718B86-12		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	15		17		20		ns
Clock Access Time	tCD		9		10		12	ns
Output Enable to Data Valid	tOE		5		5		6	ns
Clock High to Output Low-Z	tLZC	6		6		6		ns
Output Hold from Clock High	tOH	3		3		3		ns
Output Enable Low to Output Low-Z	tLZOE	0		0		0		ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC		6		6		6	ns
Clock High Pulse Width	tCH	5		5		6		ns
Clock Low Pulse Width	tCL	5		5		6		ns
Address Setup to Clock High	tAS	2.5		2.5		2.5		ns
Address Status Setup to Clock High	tSS	2.5		2.5		2.5		ns
Data Setup to Clock High	tDS	2.5		2.5		2.5		ns
Write Setup to Clock High	tWS	2.5		2.5		2.5		ns
Address Advance Setup to Clock High	tADVS	2.5		2.5		2.5		ns
Chip Select Setup to Clock High	tCSS	2.5		2.5		2.5		ns
Address Hold from Clock High	tAH	0.5		0.5		0.5		ns
Address Status Hold from Clock High	tSH	0.5		0.5		0.5		ns
Data Hold from Clock High	tDH	0.5		0.5		0.5		ns
Write Hold from Clock High	tWH	0.5		0.5		0.5		ns
Address Advance Hold from Clock High	tADVH	0.5		0.5		0.5		ns
Chip Select Hold from Clock High	tCSH	0.5		0.5		0.5		ns

NOTE : All address inputs must meet the specified setup and hold times for all rising clock (K) edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

Output Load (A)



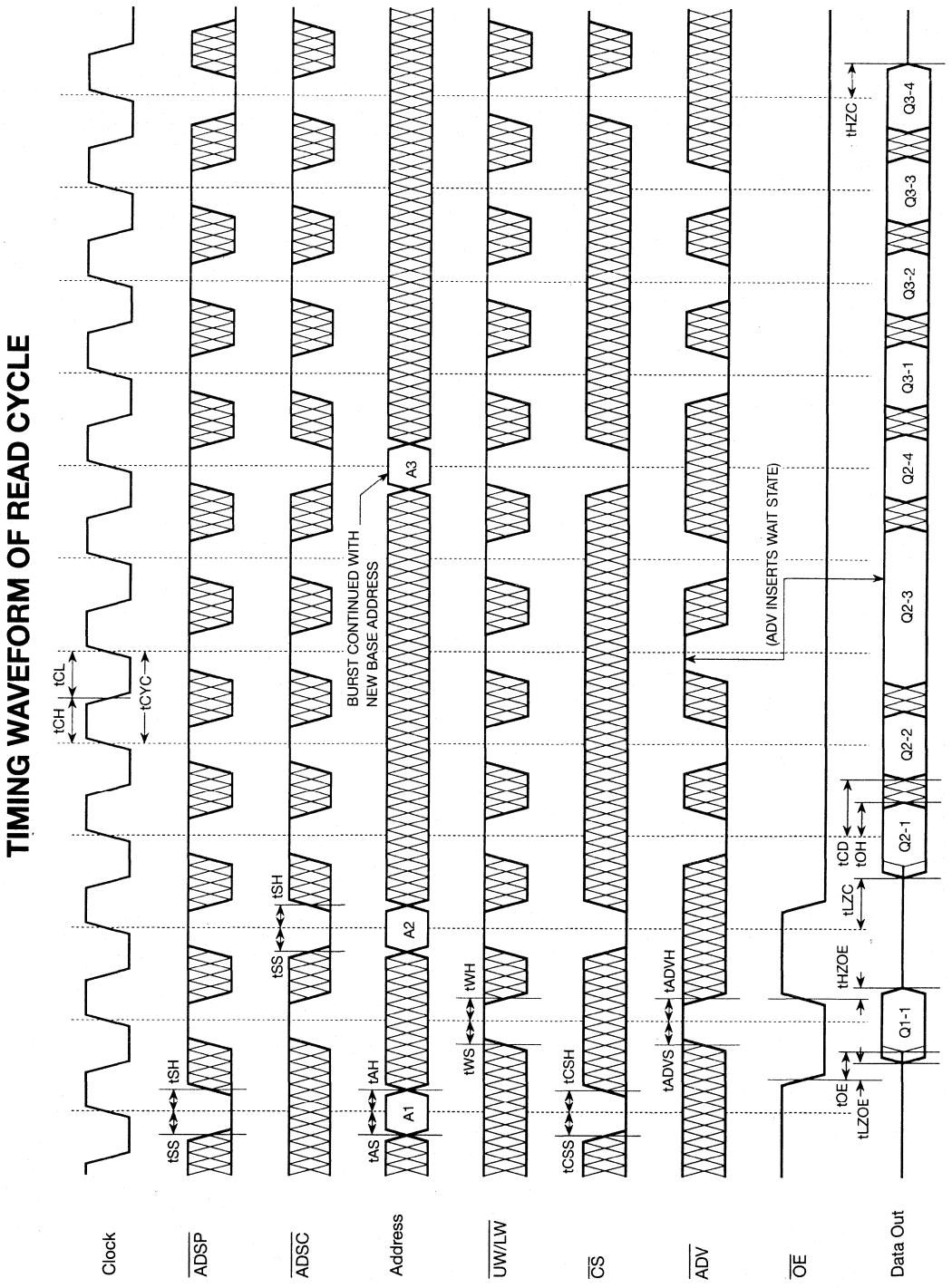
Output Load (B)
(for tLZC, tLZOE, tHZOE & tHZC)



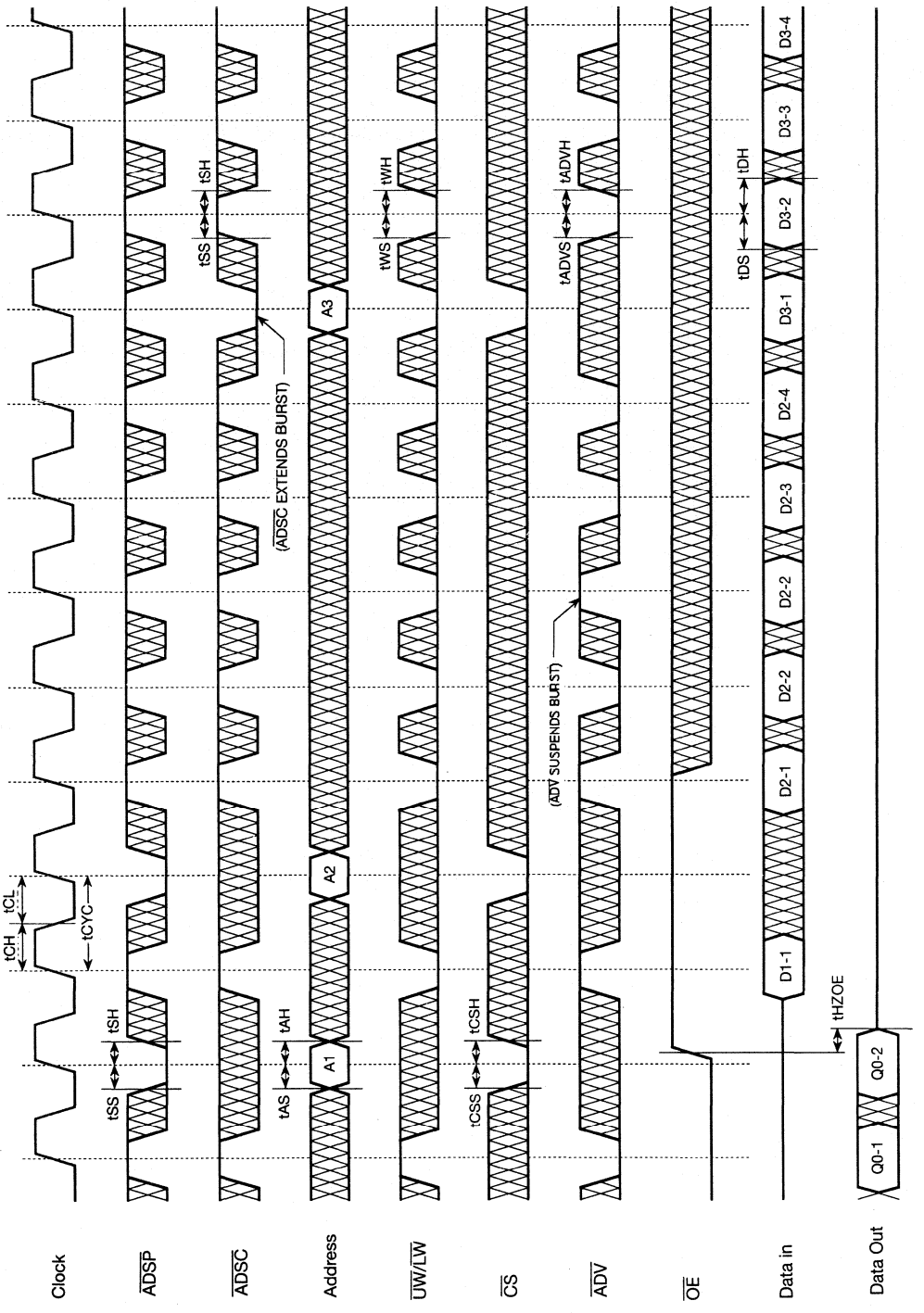
* Including Scope and Jig Capacitance

Fig. 1

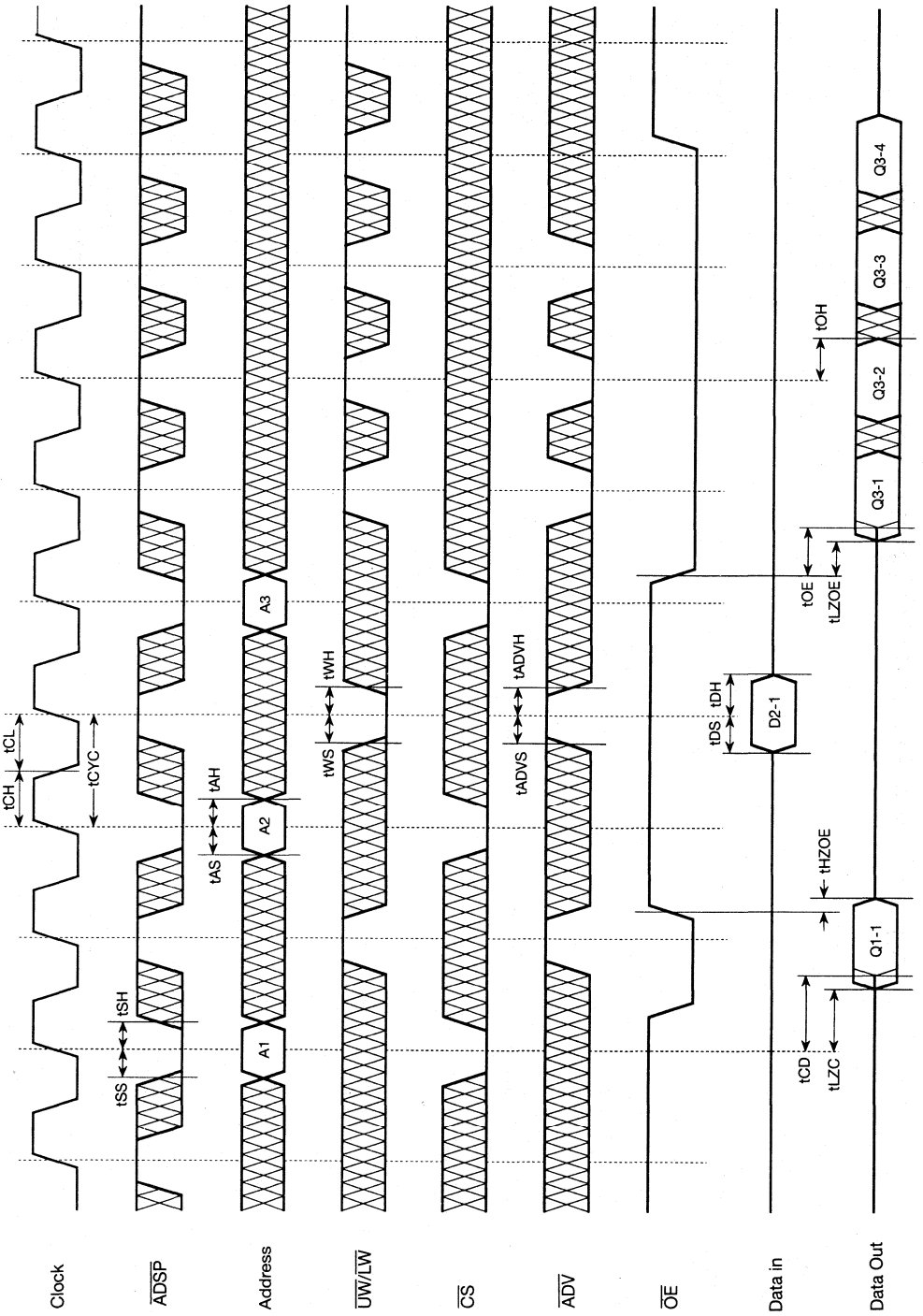
TIMING WAVEFORM OF READ CYCLE



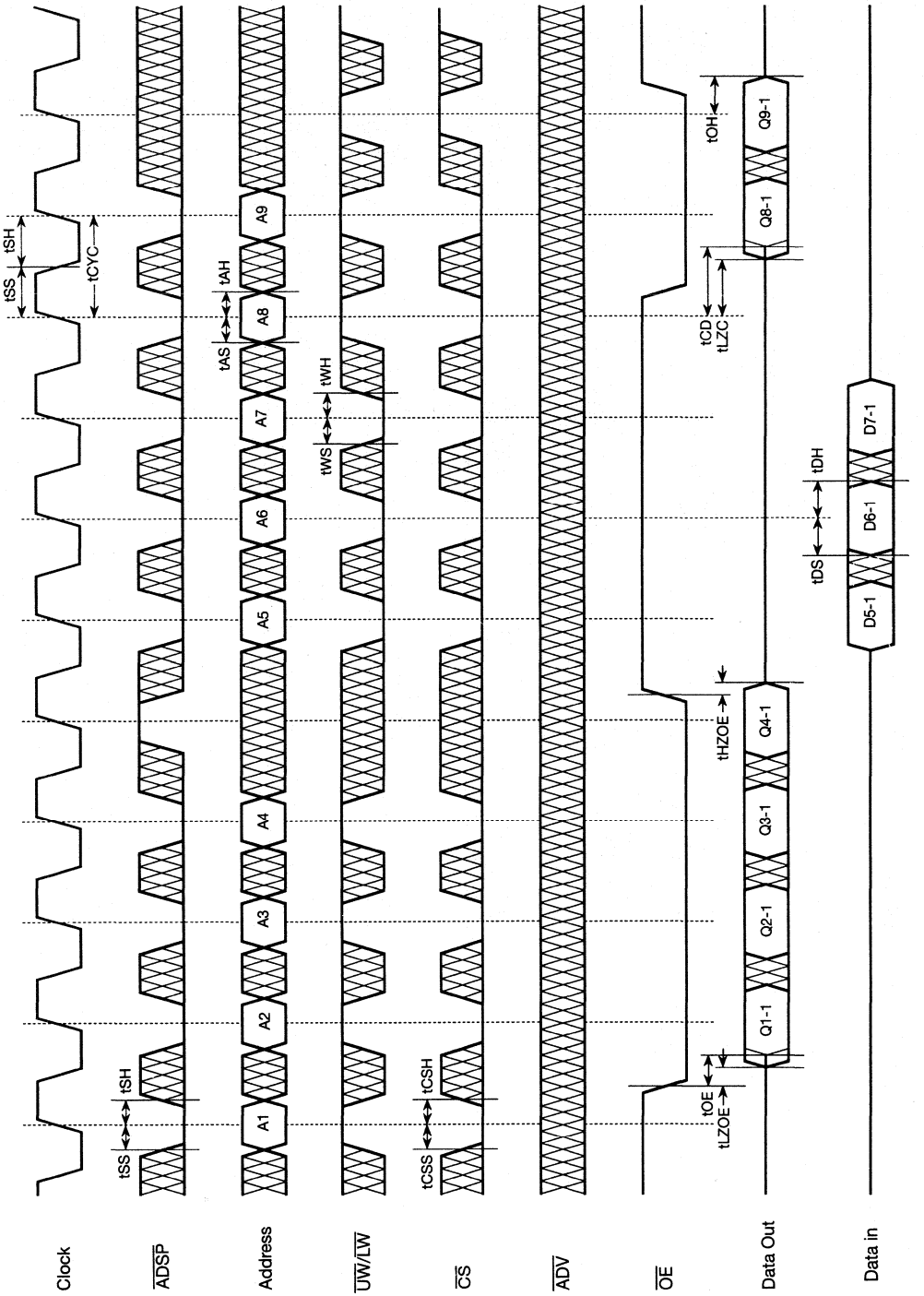
TIMING WAVEFORM OF WRITE CYCLE



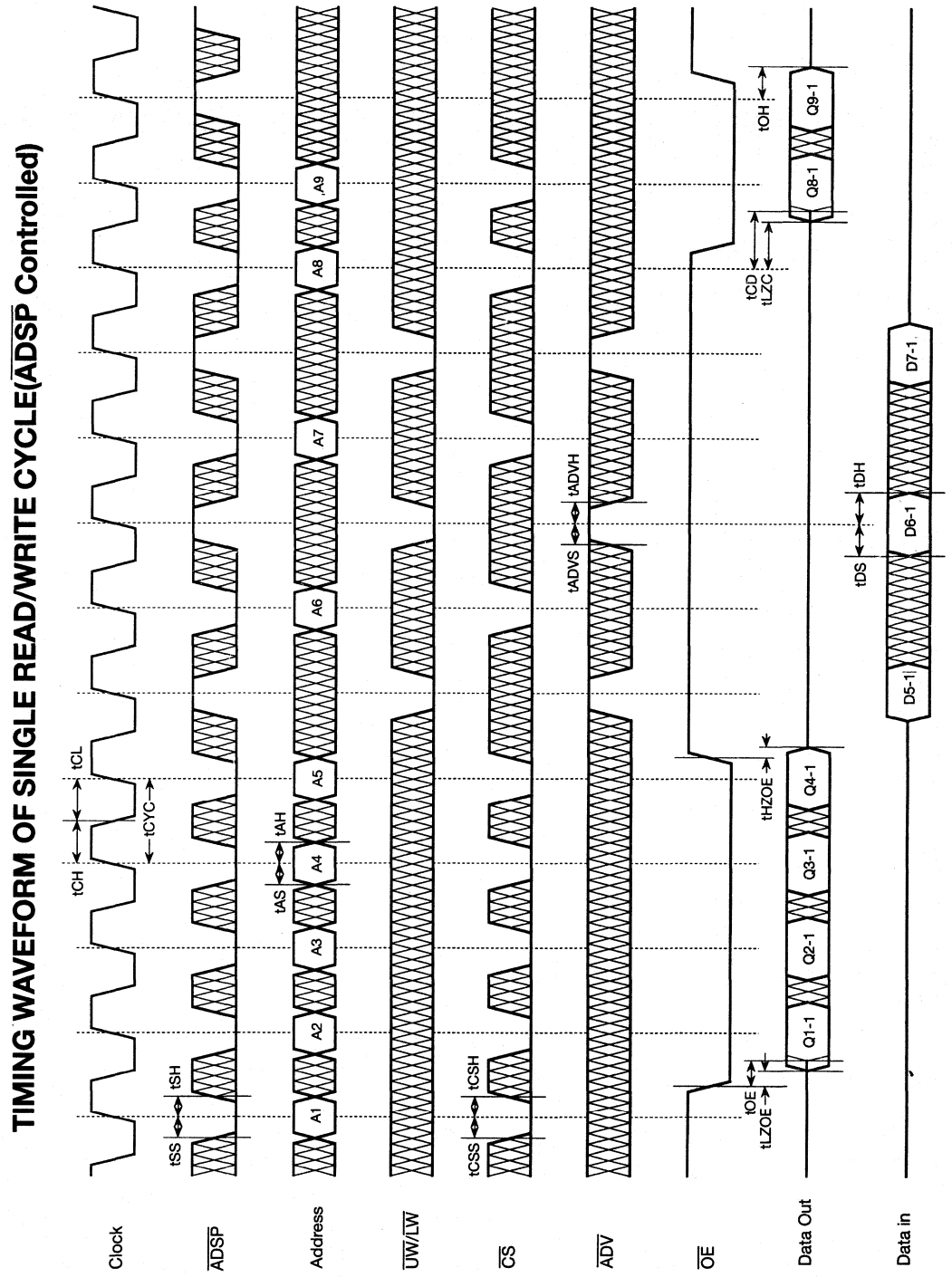
TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC Controlled)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSP}$ Controlled)



64K x 18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On- Chip Address and Control Registers.
- Single 5V±5% Power Supply.
- Byte Writable Function.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$,$\overline{ADSC}$,$\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Outputs.
- 3.3V I/O Compatible.
- 52-Pin PLCC Package.

FAST ACCESS TIMES

Parameter	Symbol	-9	-10	-12	Unit
Cycle Time	tCYC	15	17	20	ns
Clock Access Time	tCD	9	10	12	ns
Output Enable Access Time	tOE	5	5	6	ns

GENERAL DESCRIPTION

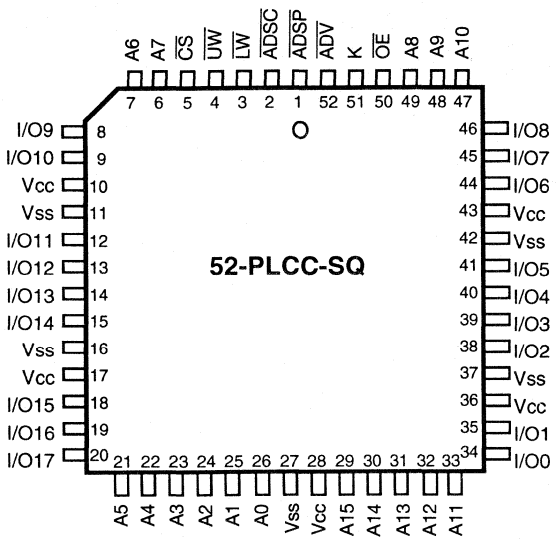
The KM718B90 is a 1,179,648 bit Synchronous Static Random Access Memory designed to support 66MHz of Intel secondary caches. It is organized as 65,536 words of 18 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced component count implementations of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous. The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Bursts can be initiated with either the address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance ($\overline{ADV}$) input.

The KM718B90 is implemented in Samsung's high performance BiCMOS technology and is available in a 52 pin PLCC package. Multiple power and ground pins are utilized to minimize ground bounce

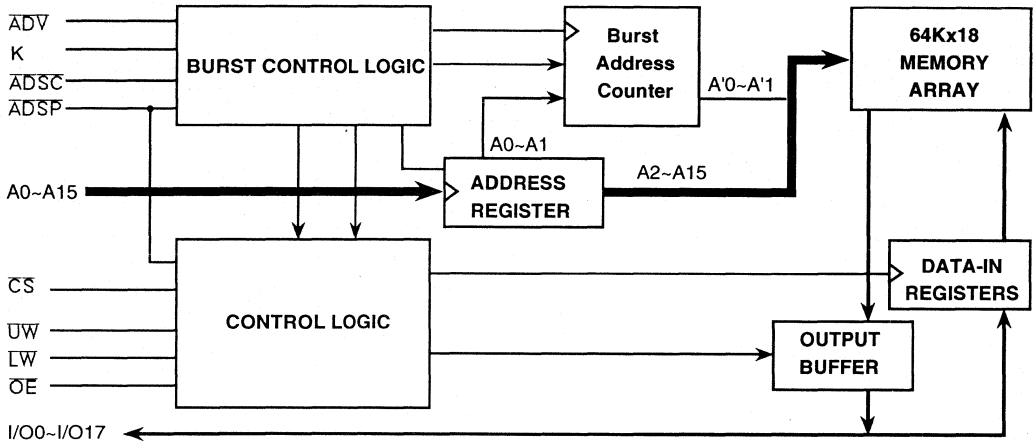
PIN CONFIGURATION(*Top View*)



PIN DESCRIPTION

Pin Name	Pin Function
A0~A15	Address Inputs
K	Clock
$\overline{LW}$,$\overline{UW}$	Write Enable
$\overline{CS}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{ADV}$	Burst Address Advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status
I/O0~I/O17	Data Inputs/Outputs
Vcc	+5V Power Supply
Vss	Ground

LOGIC BLOCK DIAGRAM



FUNCTION DESCRIPTION

The KM718B90 is a synchronous SRAM designed to support the burst address accessing sequence of the POWER microprocessor. All inputs (with the exception of $\overline{OE}$) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$ and $\overline{ADSP}$. The accesses are enabled with the chip select signals and output enable. Wait states are inserted into the access with $\overline{ADV}$.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{LW}$,$\overline{UW}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the next and subsequent clock edges. The address is incremented internally for the next access of the burst when $\overline{LW}$,$\overline{UW}$ is sampled HIGH and $\overline{ADV}$ is sampled low.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{LW}$,$\overline{UW}$. $\overline{LW}$,$\overline{UW}$ is ignored on the clock edge that samples $\overline{ADSP}$ low, but is sampled on the next and subsequent clock edges. The output buffers are disabled when $\overline{LW}$,$\overline{UW}$ is sampled low (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{LW}$,$\overline{UW}$ is sampled low. The address is incremented internally to the next address of burst if both $\overline{LW}$,$\overline{UW}$ and $\overline{ADV}$ are sampled low. Individual byte write cycles are performed by sampling low only one byte write signal ($\overline{LW}$ or $\overline{UW}$), and $\overline{LW}$ controls I/O0 - I/O7 and $\overline{UW}$ controls I/O8 - I/O17.
Read or write cycles (depending on $\overline{LW}$,$\overline{UW}$) may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ are as follows;

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{LW}$,$\overline{UW}$ is sampled on the same clock edge that samples $\overline{ADSC}$ low (and $\overline{ADSP}$ high).

Address are generated for the burst accesses as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

BURST SEQUENCE TABLE

	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	1	0	1	1	0	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{LW}$/$\overline{UW}$	K	Address Accessed	Operation
H	L	X	X	X	↑	N/A	Not Selected
H	X	L	X	X	↑	N/A	Not Selected
L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE 1 : X means "Don't Care"
NOTE 2 : The rising edge of clock is symbolized by ↑

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{OE}$	Operation
L	Read I/O0~I/O17
H	Outputs High-Z
X	Not Selected, Outputs High-Z

NOTE 1 : X means "Don't Care"
NOTE 2 : For write cycles that follow read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.5 to 7.0	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to +150	°C
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to +85	°C

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc	4.75	5.0	5.25	V
Ground	Vss	0	0	0	V

CAPACITANCE* (T_A=25°C, f=1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	8	pF

***NOTE** : Sampled not 100% tested.

TEST CONDITIONS (T_A=0°C to 70°C, Vcc=5V±5%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS (Vcc=5V±5%, T_A=0°C to +70°C)

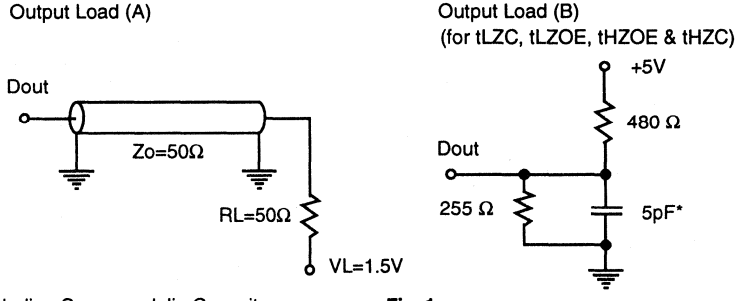
Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	Iil	Vcc=Max; V_{IN}=Vss to Vcc		-2	+2	µA
Output Leakage Current	Iol	Output Disabled		-2	+2	µA
Operating Current	Icc	Vcc=Max	15ns	-	250	mA
		I_{OUT}=0mA	17ns	-	240	
		Cycle Time ≥ tCYC min	20ns	-	220	
Standby Current	Isb	$\overline{CS}$=V_{IH}, I_{OUT}=0mA, Min Cycle		-	80	mA
Output Low Voltage	Vol	Iol=8.0mA		-	0.4	V
Output High Voltage	Voh	Ioh=-4.0mA		2.4	3.3	V
Input Low Voltage	Vil			-0.5*	0.8	V
Input High Voltage	Vih			2.2	Vcc+0.5	V

* Vil(min)=-3.0 (Pulse Width ≤20ns)

AC TIMING CHARACTERISTICS (Vcc=5V±5%, TA=0°C to +70°C)

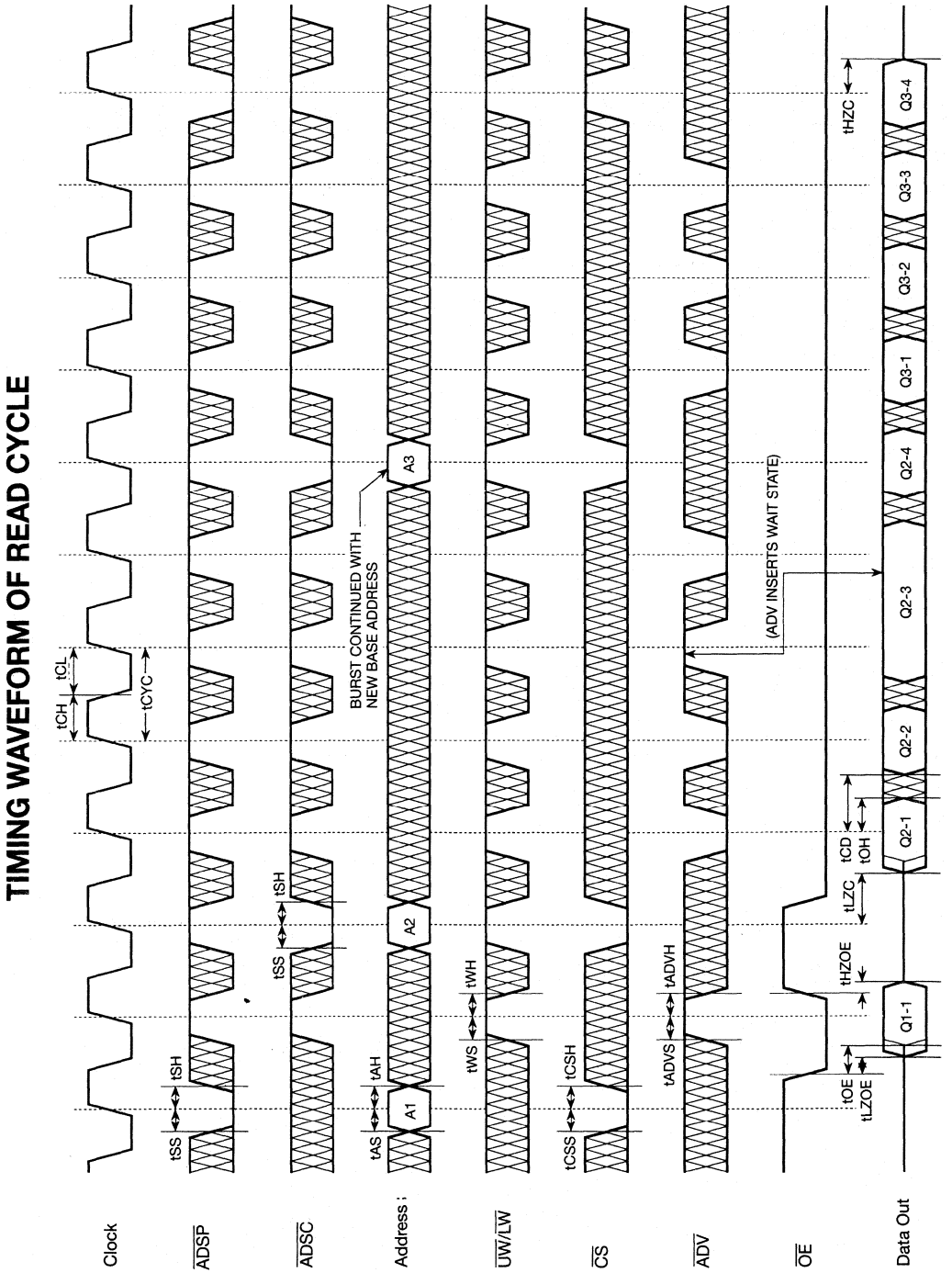
Parameter	Symbol	KM718B90-9		KM718B90-10		KM718B90-12		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	15		17		20		ns
Clock Access Time	tCD		9		10		12	ns
Output Enable to Data Valid	tOE		5		5		6	ns
Clock High to Output Low-Z	tLZC	6		6		6		ns
Output Hold from Clock High	tOH	3		3		3		ns
Output Enable Low to Output Low-Z	tLZOE	0		0		0		ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC		6		6		6	ns
Clock High Pulse Width	tCH	5		5		6		ns
Clock Low Pulse Width	tCL	5		5		6		ns
Address Setup to Clock High	tAS	2.5		2.5		2.5		ns
Address Status Setup to Clock High	tSS	2.5		2.5		2.5		ns
Data Setup to Clock High	tDS	2.5		2.5		2.5		ns
Write Setup to Clock High	tWS	2.5		2.5		2.5		ns
Address Advance Setup to Clock High	tADVS	2.5		2.5		2.5		ns
Chip Select Setup to Clock High	tCSS	2.5		2.5		2.5		ns
Address Hold from Clock High	tAH	0.5		0.5		0.5		ns
Address Status Hold from Clock High	tSH	0.5		0.5		0.5		ns
Data Hold from Clock High	tDH	0.5		0.5		0.5		ns
Write Hold from Clock High	tWH	0.5		0.5		0.5		ns
Address Advance Hold from Clock High	tADVH	0.5		0.5		0.5		ns
Chip Select Hold from Clock High	tCSH	0.5		0.5		0.5		ns

NOTE : All address inputs must meet the specified setup and hold times for all rising clock (K) edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

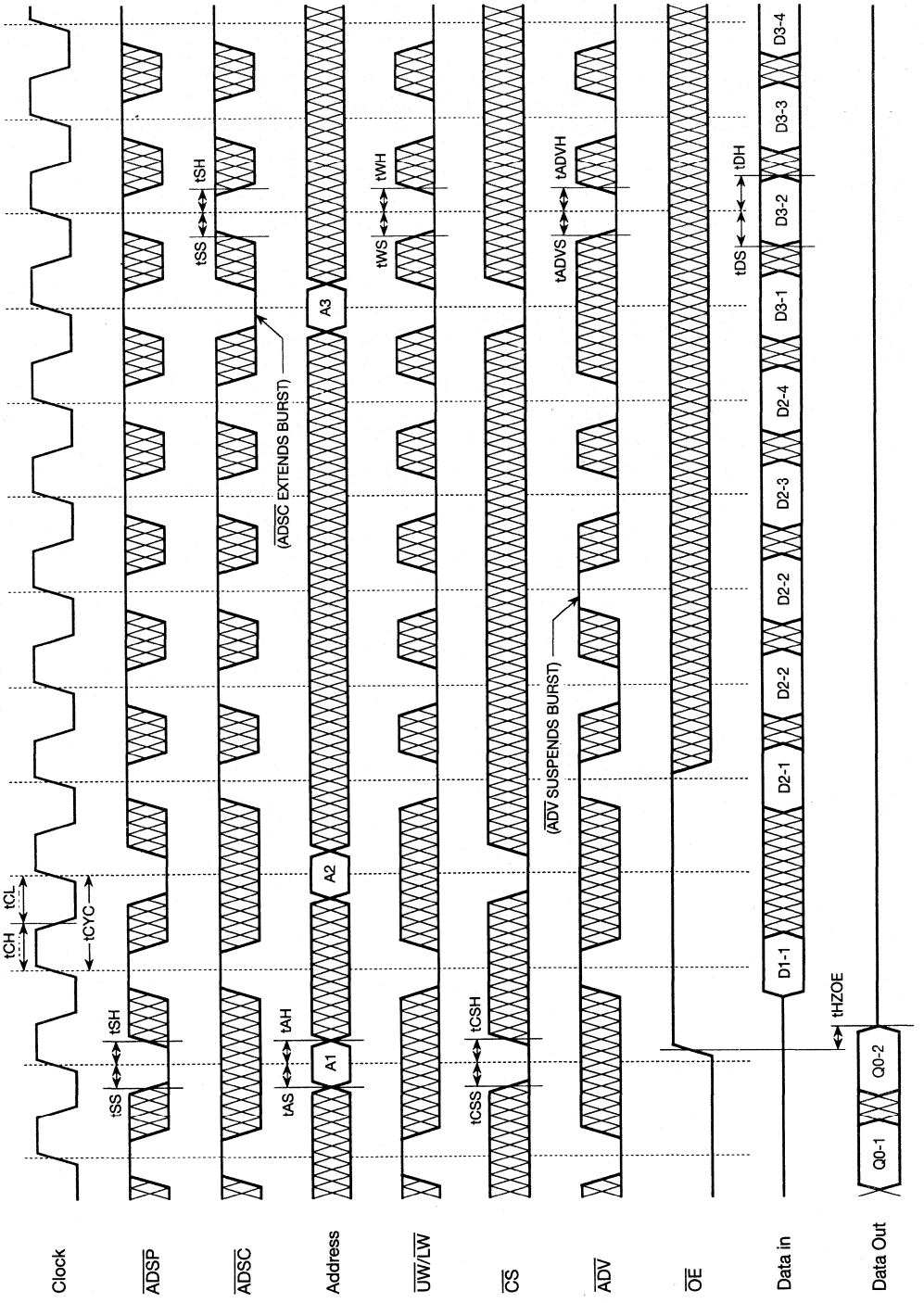


* Including Scope and Jig Capacitance **Fig. 1**

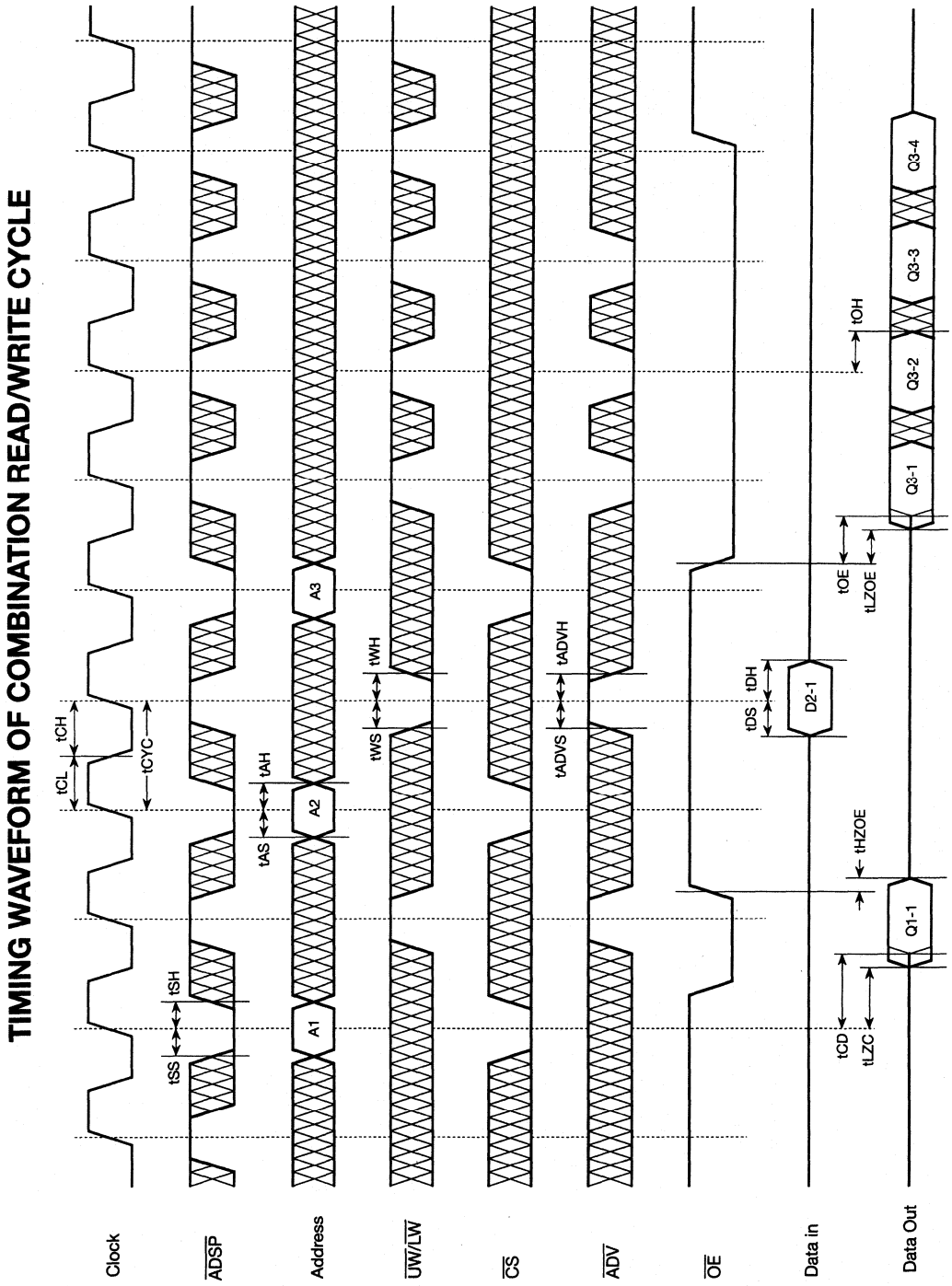
TIMING WAVEFORM OF READ CYCLE



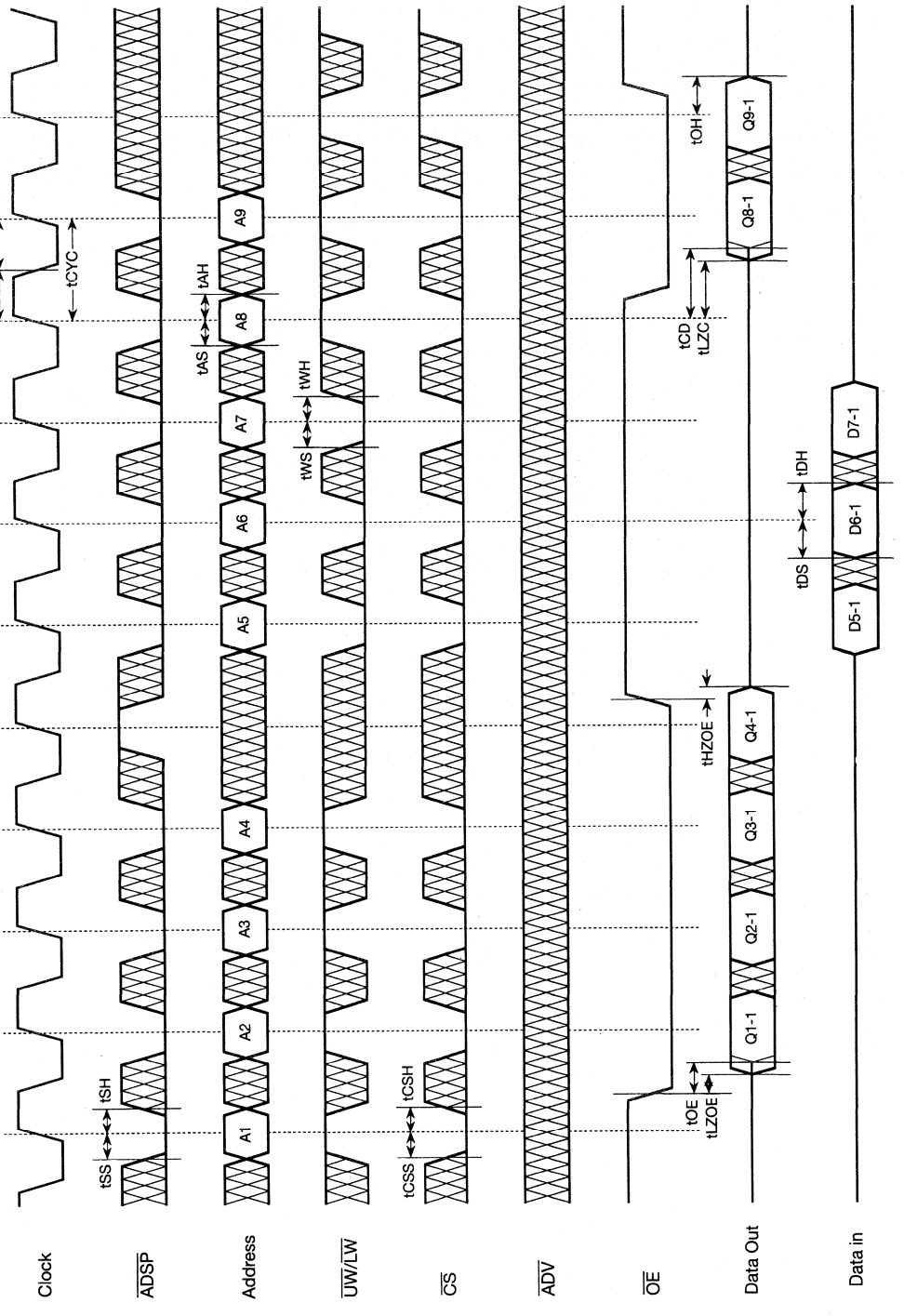
TIMING WAVEFORM OF WRITE CYCLE



TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE

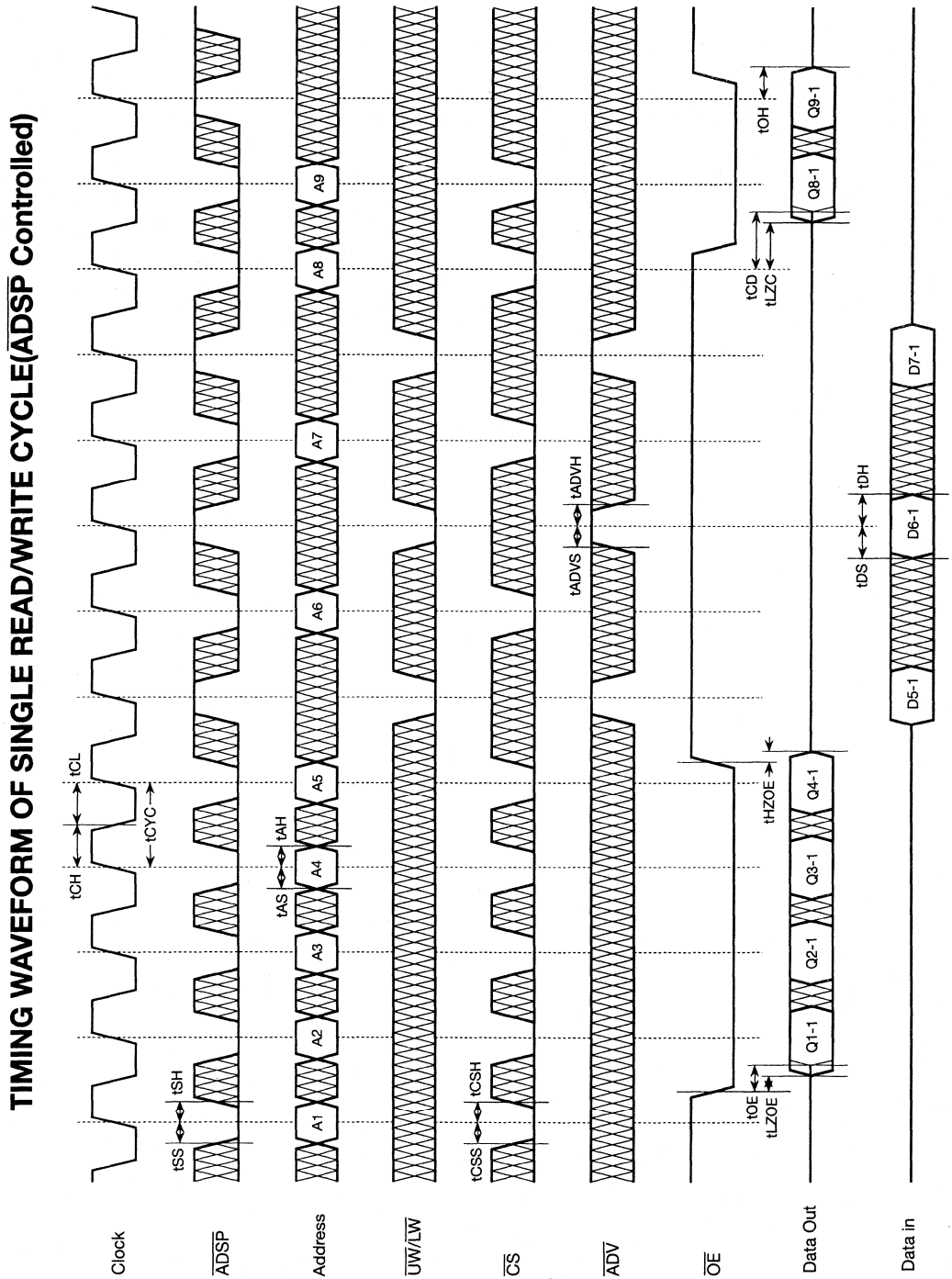


TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC Controlled)



SAMSUNG ELECTRONICS

TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSP Controlled)

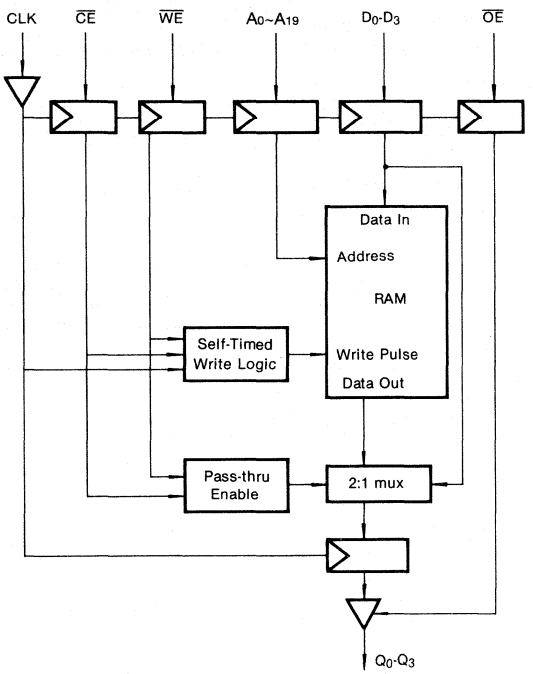


1,048,576 Words x 4-Bit Synchronous Static Random Access Memory

FEATURES

- **Fast Cycle Time : 10, 12, 15ns (Max.)**
- **Low Power Dissipation**
  KM74B4006-10 : 190mA (Max.)
  KM74B4006-12 : 185mA (Max.)
  KM74B4006-15 : 180mA (Max.)
- **Single 5±10%V Power Supply**
- **TTL Compatible inputs and outputs**
- **All Inputs and Outputs Registered with Clock**
- **Three State Outputs**
- **Available in Plastic 36 Pin 400mil SOJ**

FUNCTIONAL BLOCK DIAGRAM



Pin Name	Timing Reference	Pin Function
A_0-A_{19}	A	Address Input
$\overline{WE}$	W	Write Enable Input
$\overline{CE}$	E	Chip Enable Input
$\overline{OE}$	G	Output Enable Input
D_0-D_3	D	Data Input
Q_0-Q_3	Q	Data Output
CLK	C	Clock Input
V_{CC}	—	+5V Power Supply
V_{SS}	—	Ground

GENERAL DESCRIPTION

The KM74B4006 is a 4,194,304 bit synchronous high-speed SRAM organized as a 1,048,576 words by 4 bits. The device integrates a 1M x 4 bits SRAM core with advanced synchronous peripheral circuitry, which includes input registers, output registers, address registers and control registers.

All signals pass thru registers triggered by a positive-edge of clock input(K).

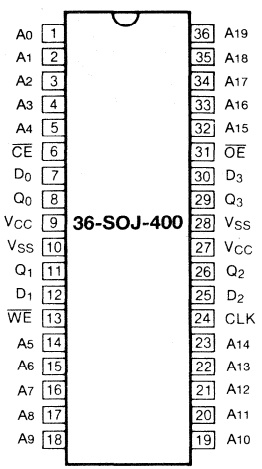
In read operation, the data of cell array accessed by the current address, registered in the address registers by the positive edge of K, are carried to the Data-out registers by the next positive edge of K. The data, registered in the Data-out registers, are projected to the output pins.

In write operation, the write data, registered in the Data-in registers, are stored in both the cell array and the Data-out registers.

This operation is fully self-timed and exclude the complexity of the write control of general SRAM. Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$.

Note that this device does not need any intervening recovery cycles in a sequential operation of arbitary read, write, and pass-thru cycles.

PIN CONFIGURATIONS (Top View)



64K x 18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On- Chip Address and Control Registers.
- Single 3.3V±5% Power Supply.
- Byte Writable Function.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$,$\overline{ADSC}$,$\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Outputs.
- 5V Tolerant I/O.
- 52-Pin PLCC Package.

FAST ACCESS TIMES

Parameter	Symbol	-9	-10	-12	Unit
Cycle Time	tCYC	15	17	20	ns
Clock Access Time	tCD	9	10	12	ns
Output Enable Access Time	tOE	5	5	6	ns

GENERAL DESCRIPTION

The KM718BV87 is a 1,179,648 bit Synchronous Static Random Access Memory designed to support zero wait state performance with advanced i486/Pentium address pipelining.

When $\overline{CS}$ is high, $\overline{ADSP}$ is blocked to control signals.

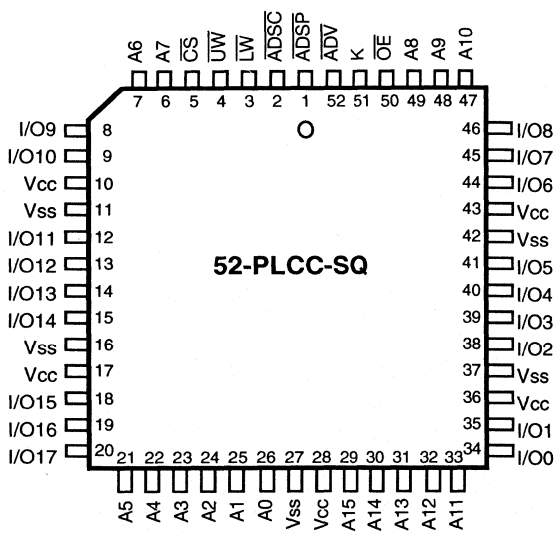
It is organized as 65,536 words of 18 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced component count implementations of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous. The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Bursts can be initiated with either the address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance ($\overline{ADV}$) input.

The KM718BV87 is implemented in Samsung's high performance BiCMOS technology and is available in a 52 pin PLCC package. Multiple power and ground pins are utilized to minimize ground bounce

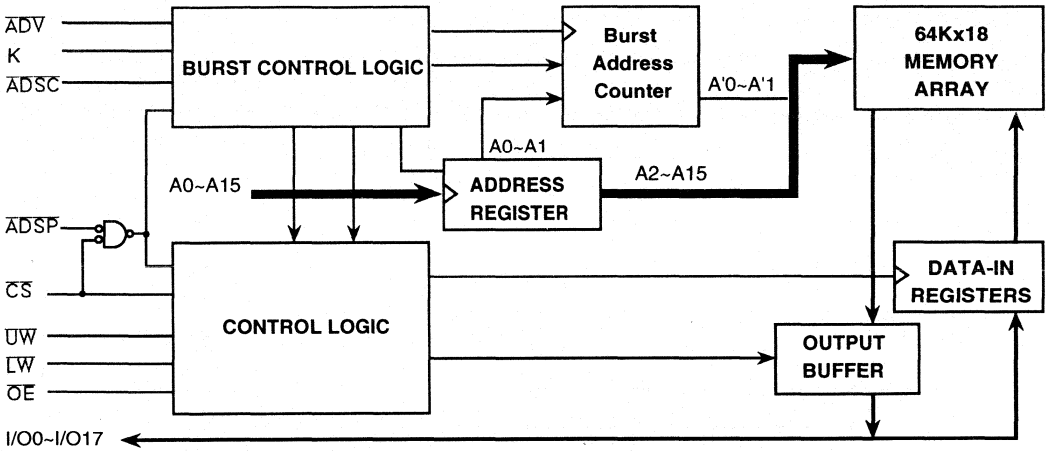
PIN CONFIGURATION(*Top View*)



PIN DESCRIPTION

Pin Name	Pin Function
A0~A15	Address Inputs
K	Clock
$\overline{LW}$,$\overline{UW}$	Write Enable
$\overline{CS}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{ADV}$	Burst Address Advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status
I/O0~I/O17	Data Inputs/Outputs
Vcc	+3.3V Power Supply
Vss	Ground

LOGIC BLOCK DIAGRAM



FUNCTION DESCRIPTION

The KM718BV87 is a synchronous SRAM designed to support the burst address accessing sequence of the i486/586 microprocessor. All inputs (with the exception of $\overline{OE}$) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$ and $\overline{ADSP}$. The accesses are enabled with the chip select signals and output enable. Wait states are inserted into the access with $\overline{ADV}$.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{LW}$,$\overline{UW}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the next and subsequent clock edges. The address is incremented internally for the next access of the burst when $\overline{LW}$,$\overline{UW}$ is sampled HIGH and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS}$.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{LW}$,$\overline{UW}$. $\overline{LW}$,$\overline{UW}$ is ignored on the clock edge that samples $\overline{ADSP}$ low, but is sampled on the next and subsequent clock edges. The output buffers are disabled when $\overline{LW}$,$\overline{UW}$ is sampled low (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{LW}$,$\overline{UW}$ is sampled low. The address is incremented internally to the next address of burst if both $\overline{LW}$,$\overline{UW}$ and $\overline{ADV}$ are sampled low. Individual byte write cycles are performed by sampling low only one byte write signal ($\overline{LW}$ or $\overline{UW}$), and $\overline{LW}$ controls I/O0 - I/O7 and $\overline{UW}$ controls I/O8 - I/O17.
Read or write cycles (depending on $\overline{LW}$,$\overline{UW}$) may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ are as follows;

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{LW}$,$\overline{UW}$ is sampled on the same clock edge that samples $\overline{ADSC}$ low (and $\overline{ADSP}$ high).

Address are generated for the burst accesses as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

BURST SEQUENCE TABLE

	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	0	0	1	1	1	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	LW/UW	K	Address Accessed	Operation
L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
H	X	L	X	X	↑	N/A	Not Selected
H	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle

NOTE 1 : X means "Don't Care"
NOTE 2 : The rising edge of clock is symbolized by ↑

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{OE}$	Operation
L	Read I/O0~I/O17
H	Outputs High-Z
X	Not Selected, Outputs High-Z

NOTE 1 : X means "Don't Care"
NOTE 2 : For write cycles that follow read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.3 to 4.6	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to +150	°C
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to +85	°C

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0°C \le T_A \le 70°C$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Ground	Vss	0	0	0	V

CAPACITANCE* (T_A=25°C, f=1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	8	pF

***NOTE** : Sampled not 100% tested.

TEST CONDITIONS (T_A=0°C to 70°C, Vcc=3.3V±5%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS (Vcc=3.3V±5%, T_A=0°C to +70°C)

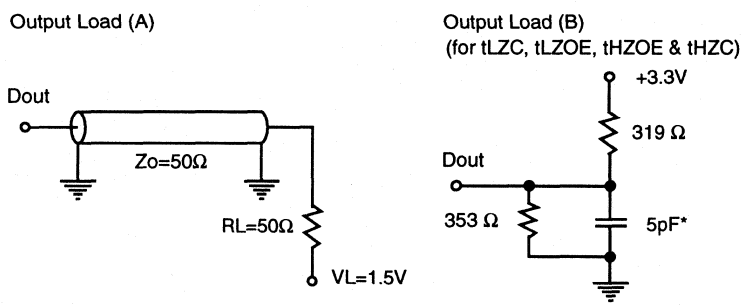
Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	Iil	Vcc=Max; V_{IN}=Vss to Vcc		-2	+2	μA
Output Leakage Current	Iol	Output Disabled		-2	+2	μA
Operating Current	Icc	Vcc=Max	15ns	-	250	mA
		I_{OUT}=0mA	17ns	-	240	
		Cycle Time ≥ tCYC min	20ns	-	220	
Standby Current	Isb	$\overline{CS}$=V_{IH}, I_{OUT}=0mA, Min Cycle		-	80	mA
Output Low Voltage	Vol	Iol=8.0mA		-	0.4	V
Output High Voltage	Voh	Ioh=-4.0mA		2.4	-	V
Input Low Voltage	Vil			-0.5*	0.8	V
Input High Voltage	Vih			2.2	5.5	V

* Vil(min)=-3.0 (Pulse Width ≤20ns)

AC TIMING CHARACTERISTICS (Vcc=3.3V±5%, TA=0°C to +70°C)

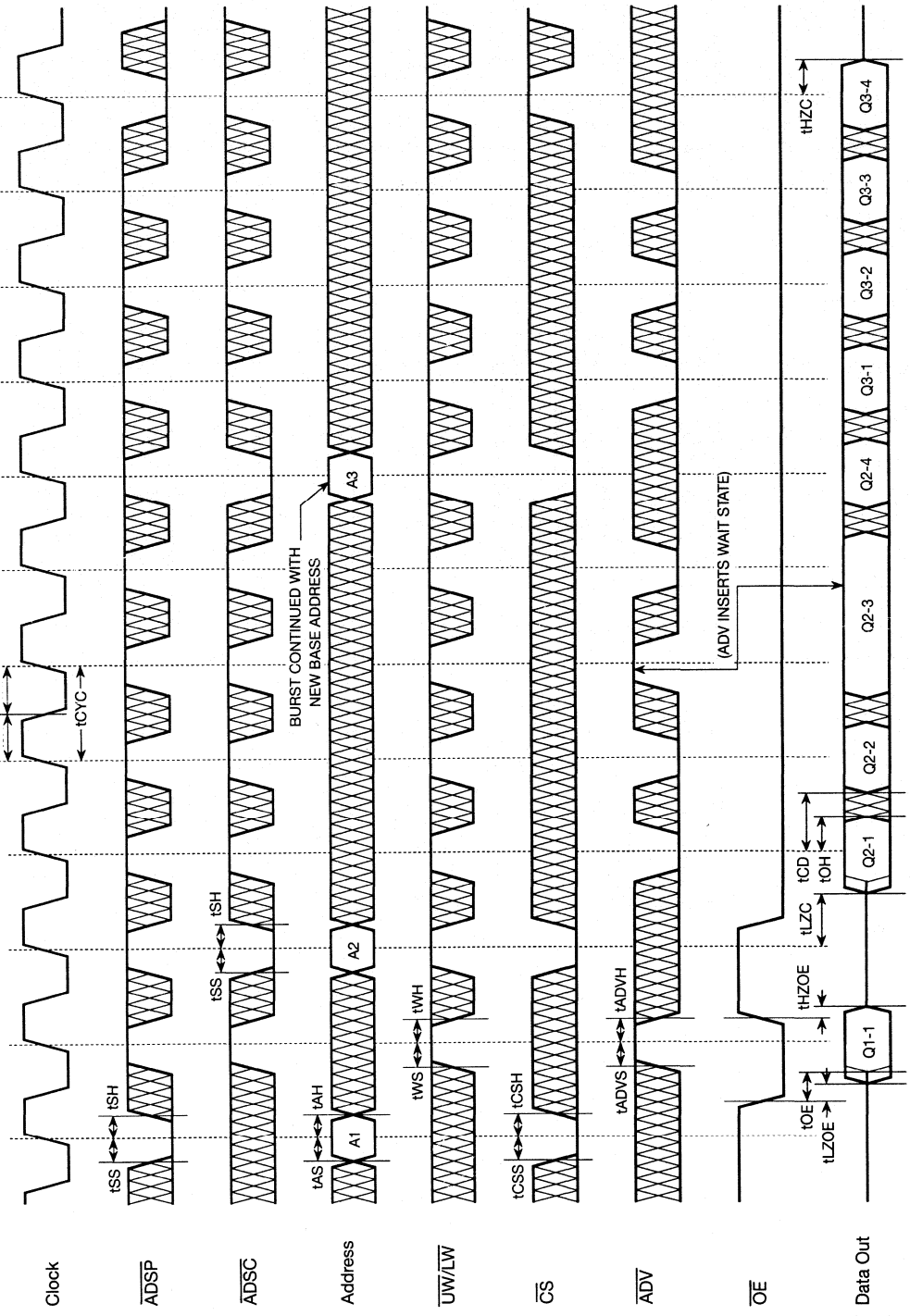
Parameter	Symbol	KM718BV87-9		KM718BV87-10		KM718BV87-12		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	15		17		20		ns
Clock Access Time	tCD		9		10		12	ns
Output Enable to Data Valid	tOE		5		5		6	ns
Clock High to Output Low-Z	tLZC	6		6		6		ns
Output Hold from Clock High	tOH	3		3		3		ns
Output Enable Low to Output Low-Z	tLZOE	0		0		0		ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC		6		6		6	ns
Clock High Pulse Width	tCH	5		5		6		ns
Clock Low Pulse Width	tCL	5		5		6		ns
Address Setup to Clock High	tAS	2.5		2.5		2.5		ns
Address Status Setup to Clock High	tSS	2.5		2.5		2.5		ns
Data Setup to Clock High	tDS	2.5		2.5		2.5		ns
Write Setup to Clock High	tWS	2.5		2.5		2.5		ns
Address Advance Setup to Clock High	tADVS	2.5		2.5		2.5		ns
Chip Select Setup to Clock High	tCSS	2.5		2.5		2.5		ns
Address Hold from Clock High	tAH	0.5		0.5		0.5		ns
Address Status Hold from Clock High	tSH	0.5		0.5		0.5		ns
Data Hold from Clock High	tDH	0.5		0.5		0.5		ns
Write Hold from Clock High	tWH	0.5		0.5		0.5		ns
Address Advance Hold from Clock High	tADVH	0.5		0.5		0.5		ns
Chip Select Hold from Clock High	tCSH	0.5		0.5		0.5		ns

NOTE : All address inputs must meet the specified setup and hold times for all rising clock (K) edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.



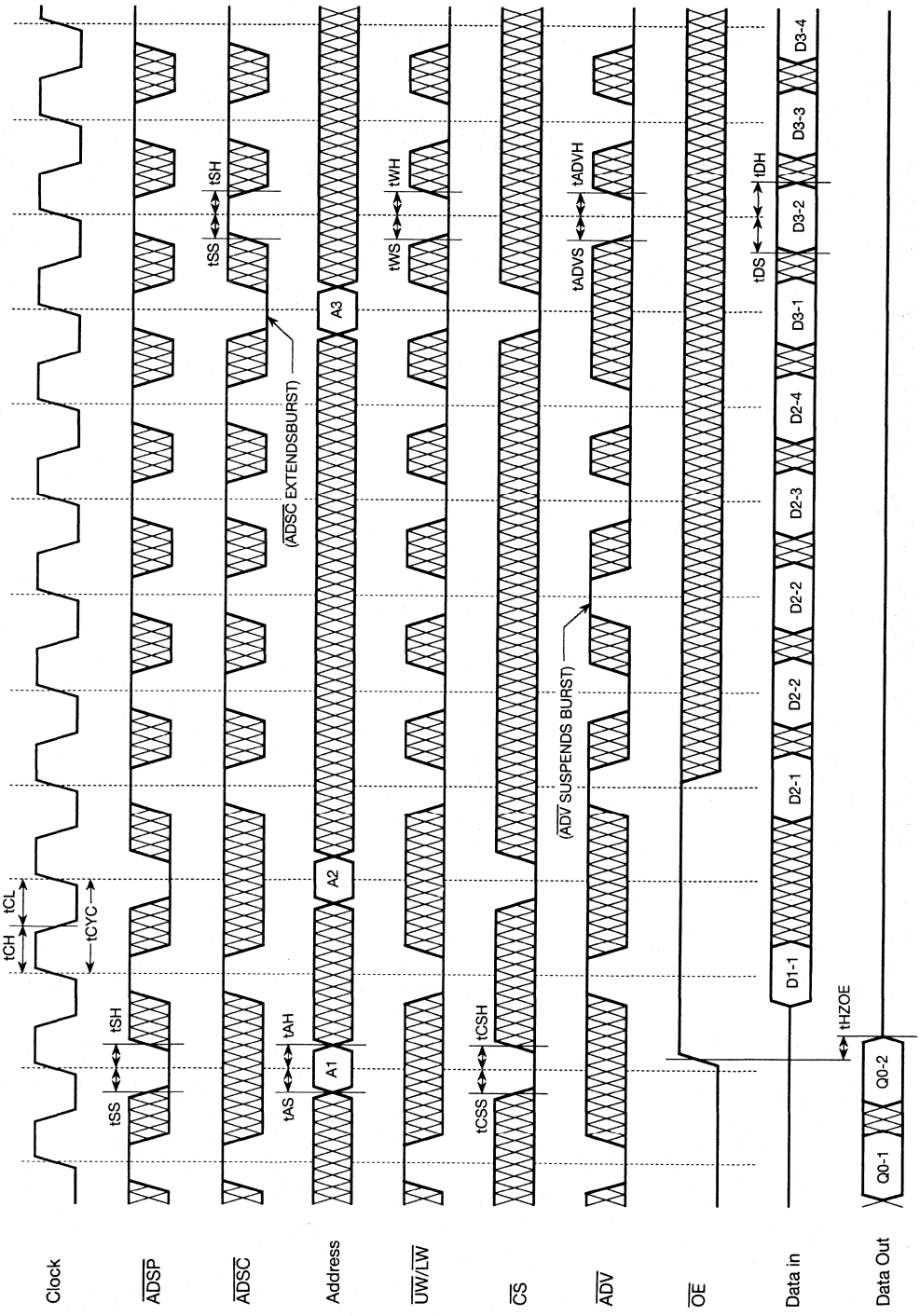
* Including Scope and Jig Capacitance **Fig. 1**

TIMING WAVEFORM OF READ CYCLE

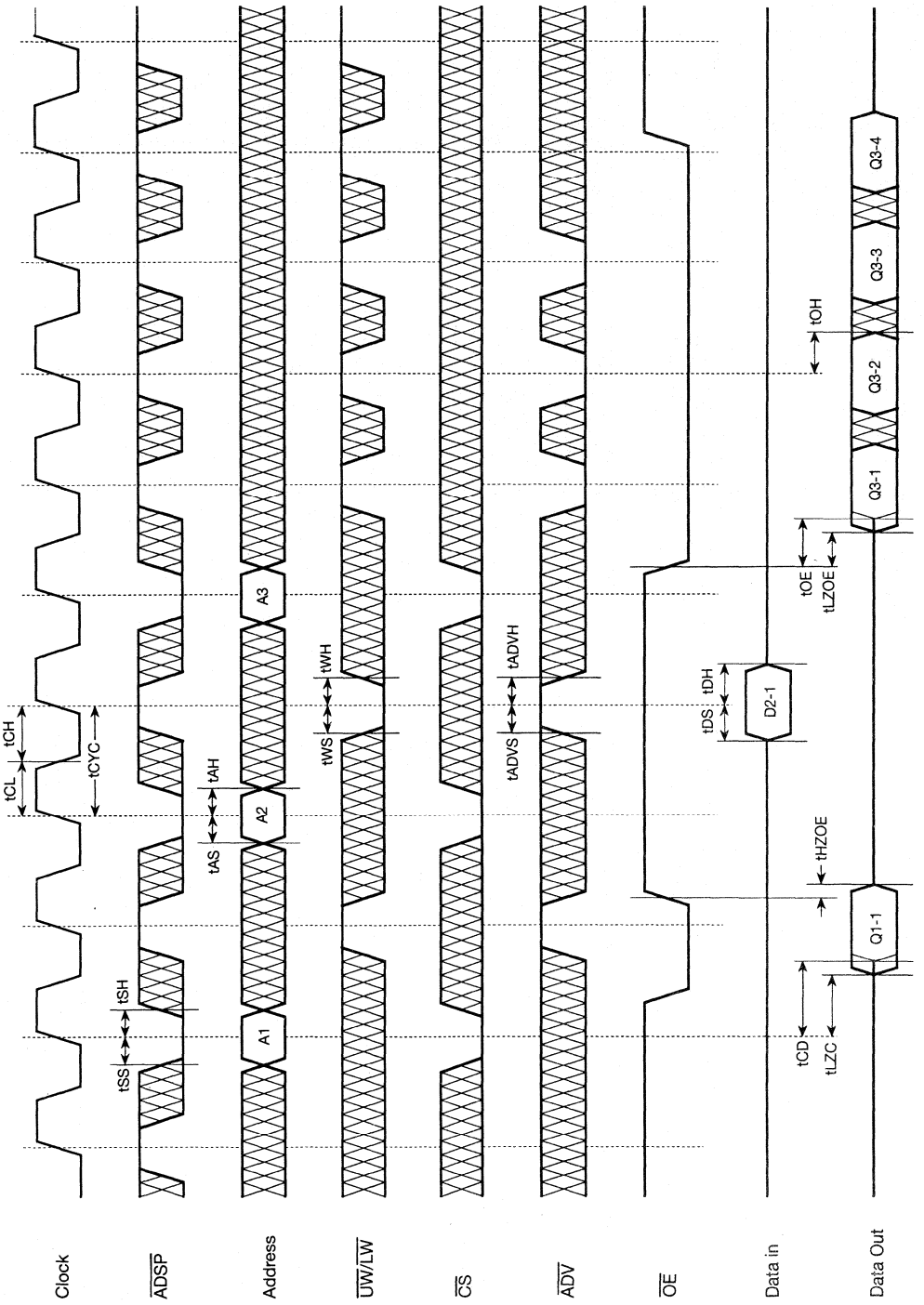


2

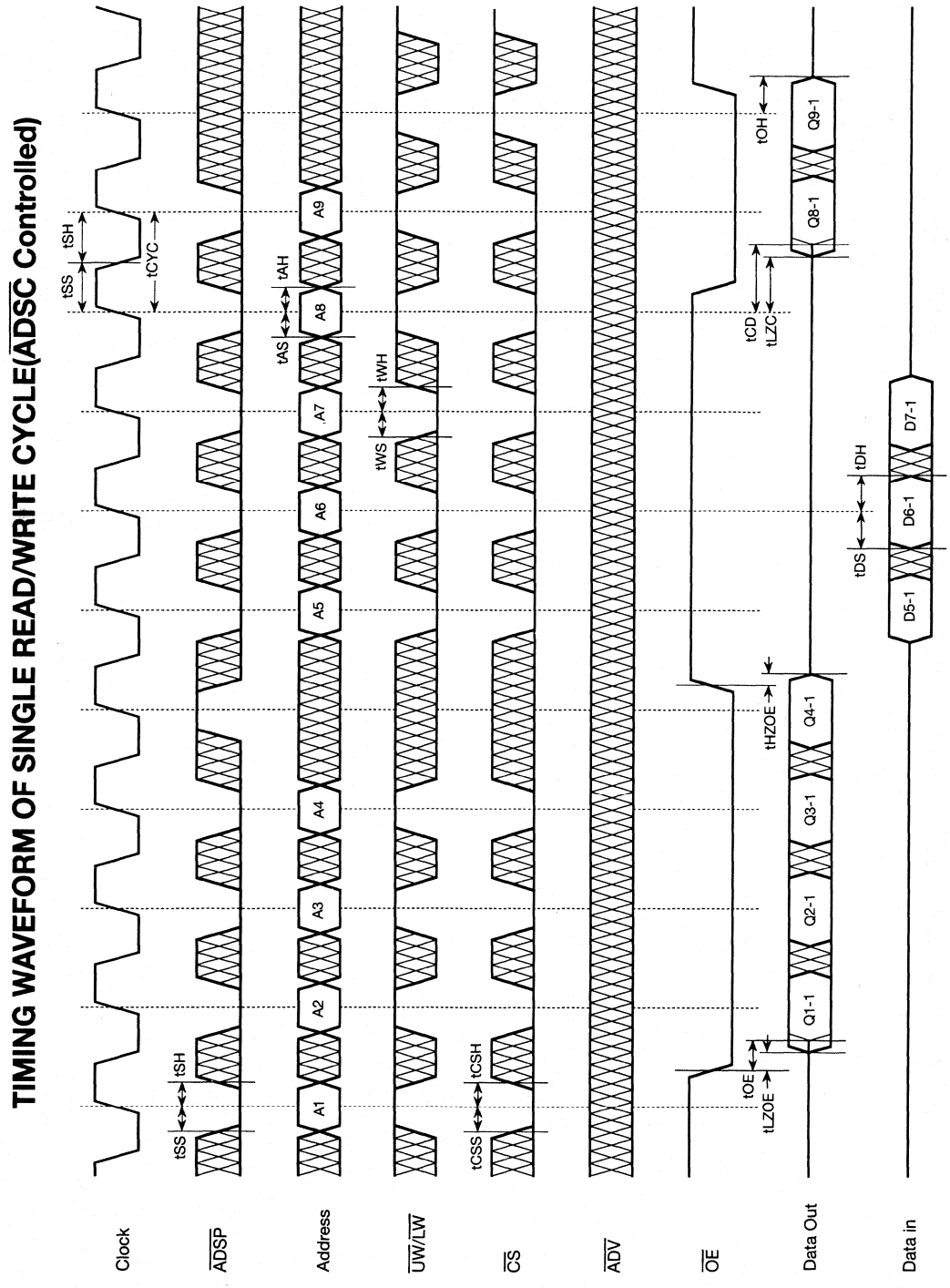
TIMING WAVEFORM OF WRITE CYCLE



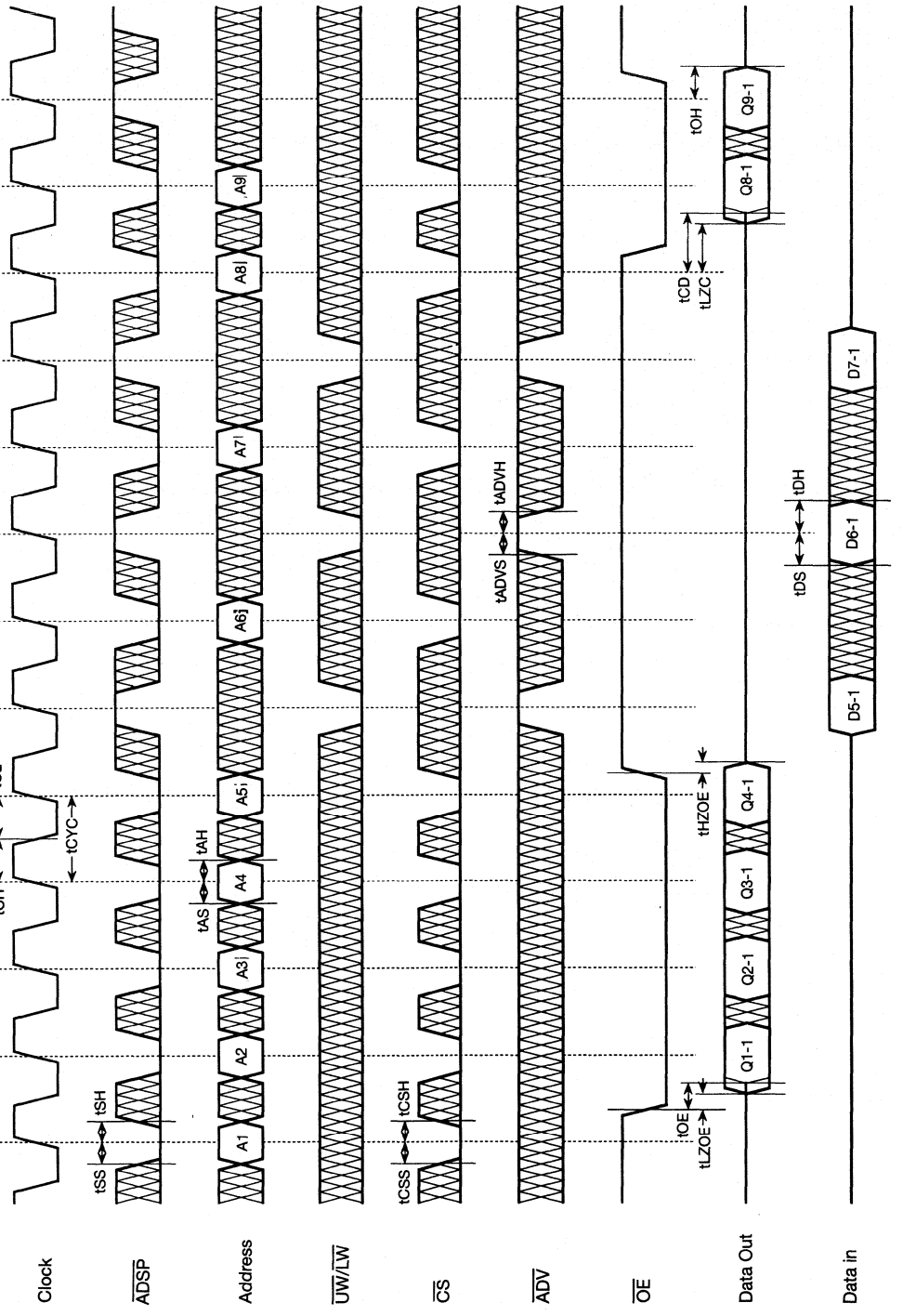
TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSC}$ Controlled)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSP}$ Controlled)



64K x 18-Bit Syncronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On- Chip Address and Control Registers.
- Single 3.3V±5% Power Supply.
- Byte Writable Function.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$,$\overline{ADSC}$,$\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Outputs.
- 5V Tolerant I/O.
- 52-Pin PLCC Package.

GENERAL DESCRIPTION

The KM718BV90 is a 1,179,648 bit Synchronous Static Random Access Memory designed to support 66MHz of Intel secondary caches. It is organized as 65,536 words of 18 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced component count implementations of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous. The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

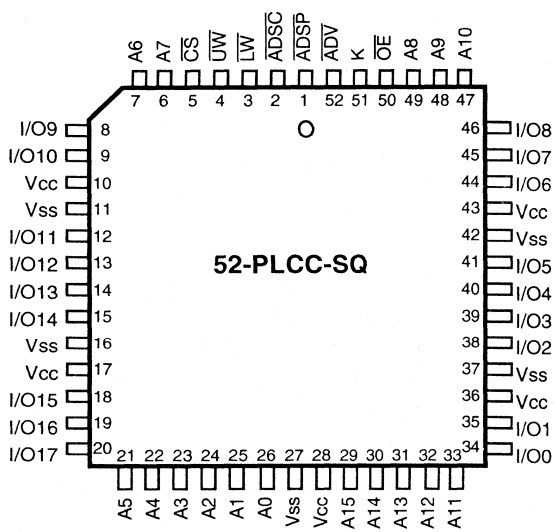
Bursts can be initiated with either the address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance ($\overline{ADV}$) input.

The KM718BV90 is implemented in Samsung's high performance BiCMOS technology and is available in a 52 pin PLCC package. Multiple power and ground pins are utilized to minimize ground bounce

FAST ACCESS TIMES

Parameter	Symbol	-9	-10	-12	Unit
Cycle Time	tCYC	15	17	20	ns
Clock Access Time	tCD	9	10	12	ns
Output Enable Access Time	tOE	5	5	6	ns

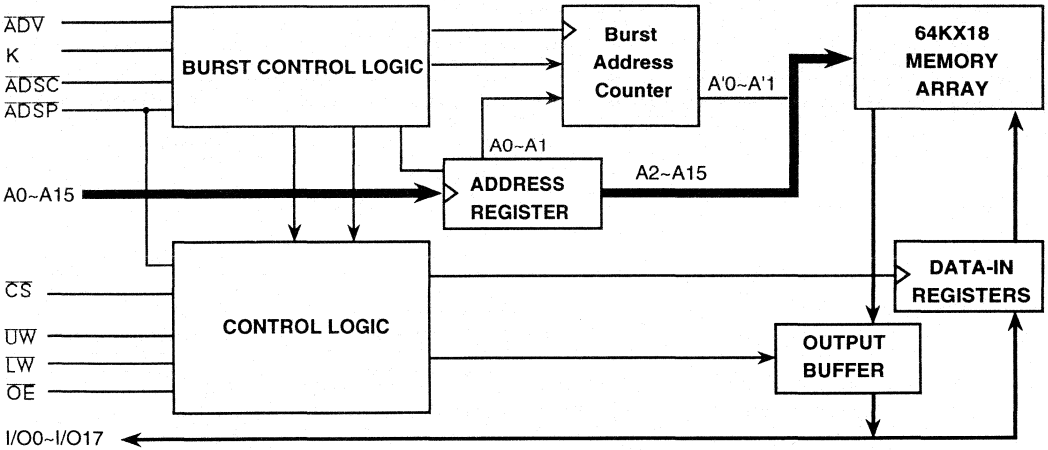
PIN CONFIGURATION(*Top View*)



PIN DESCRIPTION

Pin Name	Pin Function
A0~A15	Address Inputs
K	Clock
$\overline{LW}$,$\overline{UW}$	Write Enable
$\overline{CS}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{ADV}$	Burst Address Advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status
I/O0~I/O17	Data Inputs/Outputs
Vcc	+3.3V Power Supply
Vss	Ground

LOGIC BLOCK DIAGRAM



FUNCTION DESCRIPTION

The KM718BV90 is a synchronous SRAM designed to support the burst address accessing sequence of the MCM68040 microprocessor. All inputs (with the exception of $\overline{OE}$) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$ and $\overline{ADSP}$. The accesses are enabled with the chip select signals and output enable. Wait states are inserted into the access with $\overline{ADV}$.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{LW}$,$\overline{UW}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the next and subsequent clock edges. The address is incremented internally for the next access of the burst when $\overline{LW}$,$\overline{UW}$ is sampled HIGH and $\overline{ADV}$ is sampled low.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{LW}$,$\overline{UW}$. $\overline{LW}$,$\overline{UW}$ is ignored on the clock edge that samples $\overline{ADSP}$ low, but is sampled on the next and subsequent clock edges. The output buffers are disabled when $\overline{LW}$,$\overline{UW}$ is sampled low (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{LW}$,$\overline{UW}$ is sampled low. The address is incremented internally to the next address of burst if both $\overline{LW}$,$\overline{UW}$ and $\overline{ADV}$ are sampled low. Individual byte write cycles are performed by sampling low only one byte write signal ($\overline{LW}$ or $\overline{UW}$), and $\overline{LW}$ controls I/O0 - I/O7 and $\overline{UW}$ controls I/O8 - I/O17.
Read or write cycles (depending on $\overline{LW}$,$\overline{UW}$) may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ are as follows;

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{LW}$,$\overline{UW}$ is sampled on the same clock edge that samples $\overline{ADSC}$ low (and $\overline{ADSP}$ high).

Address are generated for the burst accesses as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

BURST SEQUENCE TABLE

	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	1	0	1	1	0	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{LW}$/$\overline{UW}$	K	Address Accessed	Operation
H	L	X	X	X	↑	N/A	Not Selected
H	X	L	X	X	↑	N/A	Not Selected
L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE 1 : X means "Don't Care"
NOTE 2 : The rising edge of clock is symbolized by ↑

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{OE}$	Operation
L	Read I/O0~I/O17
H	Outputs High-Z
X	Not Selected, Outputs High-Z

NOTE 1 : X means "Don't Care"
NOTE 2 : For write cycles that follow read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.3 to 4.6	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to +150	°C
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to +85	°C

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Ground	Vss	0	0	0	V

CAPACITANCE* (T_A=25°C, f=1Mhz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	8	pF

***NOTE** : Sampled not 100% tested.

TEST CONDITIONS (T_A=0°C to 70°C, Vcc=3.3V±5%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS (Vcc=3.3V±5%, T_A=0°C to +70°C)

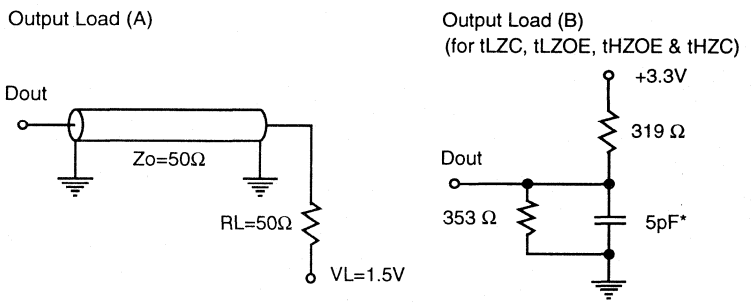
Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	Iil	Vcc=Max; V_{IN}=Vss to Vcc		-2	+2	μA
Output Leakage Current	Iol	Output Disabled		-2	+2	μA
Operating Current	Icc	Vcc=Max	15ns	-	250	mA
		I_{OUT}=0mA	17ns	-	240	
		Cycle Time ≥ tCYC min	20ns	-	220	
Standby Current	Isb	$\overline{CS}$=V_{IH}, I_{OUT}=0mA, Min Cycle		-	80	mA
Output Low Voltage	Vol	Iol=8.0mA		-	0.4	V
Output High Voltage	Voh	Ioh=-4.0mA		2.4	-	V
Input Low Voltage	Vil			-0.5*	0.8	V
Input High Voltage	Vih			2.2	5.5	V

* Vil(min)=-3.0 (Pulse Width ≤20ns)

AC TIMING CHARACTERISTICS (Vcc=3.3V±5%, TA=0°C to +70°C)

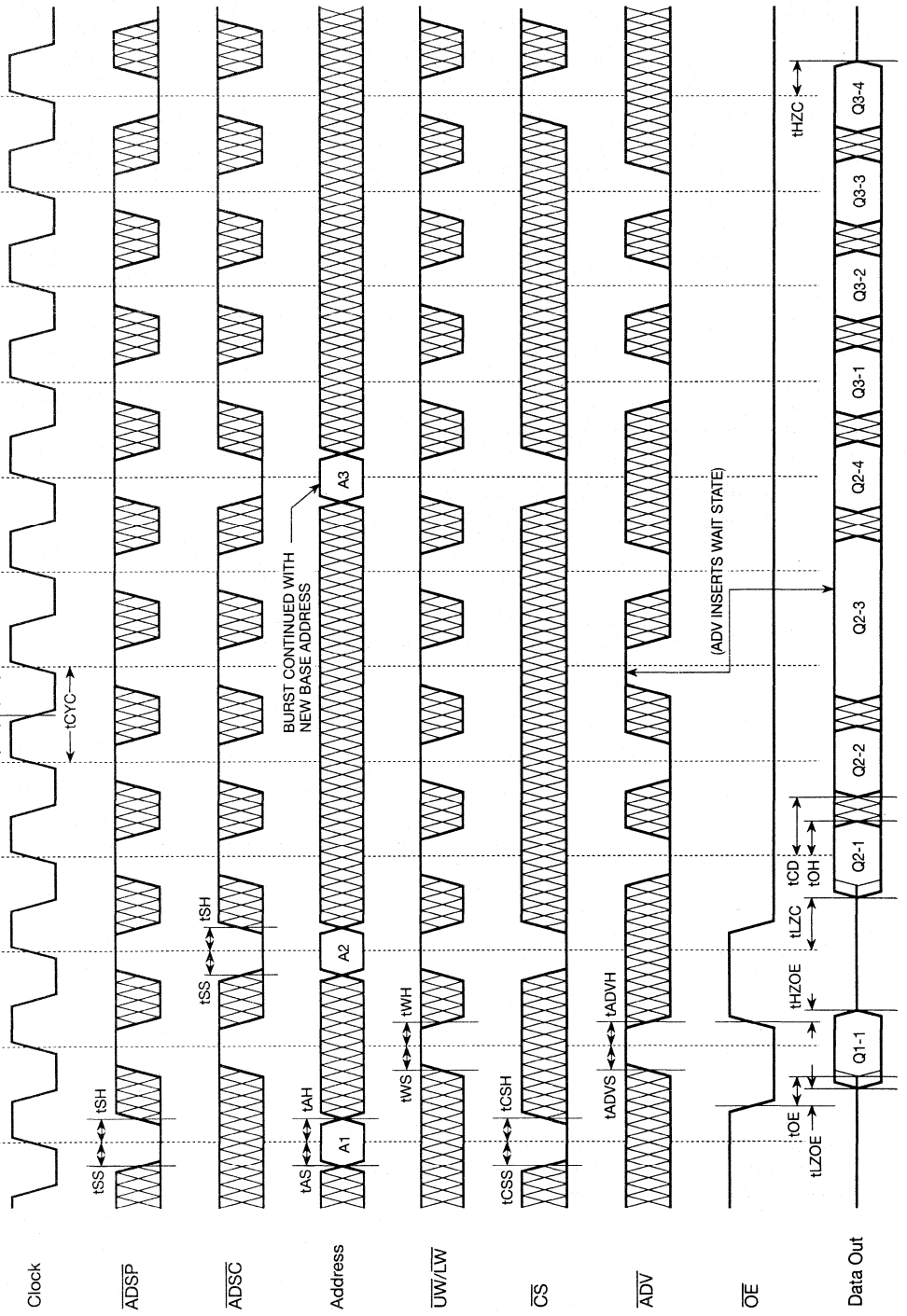
Parameter	Symbol	KM718BV90-9		KM718BV90-10		KM718BV90-12		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	15		17		20		ns
Clock Access Time	tCD		9		10		12	ns
Output Enable to Data Valid	tOE		5		5		6	ns
Clock High to Output Low-Z	tLZC	6		6		6		ns
Output Hold from Clock High	tOH	3		3		3		ns
Output Enable Low to Output Low-Z	tLZOE	0		0		0		ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC		6		6		6	ns
Clock High Pulse Width	tCH	5		5		6		ns
Clock Low Pulse Width	tCL	5		5		6		ns
Address Setup to Clock High	tAS	2.5		2.5		2.5		ns
Address Status Setup to Clock High	tSS	2.5		2.5		2.5		ns
Data Setup to Clock High	tDS	2.5		2.5		2.5		ns
Write Setup to Clock High	tWS	2.5		2.5		2.5		ns
Address Advance Setup to Clock High	tADVS	2.5		2.5		2.5		ns
Chip Select Setup to Clock High	tCSS	2.5		2.5		2.5		ns
Address Hold from Clock High	tAH	0.5		0.5		0.5		ns
Address Status Hold from Clock High	tSH	0.5		0.5		0.5		ns
Data Hold from Clock High	tDH	0.5		0.5		0.5		ns
Write Hold from Clock High	tWH	0.5		0.5		0.5		ns
Address Advance Hold from Clock High	tADVH	0.5		0.5		0.5		ns
Chip Select Hold from Clock High	tCSH	0.5		0.5		0.5		ns

NOTE : All address inputs must meet the specified setup and hold times for all rising clock (K) edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

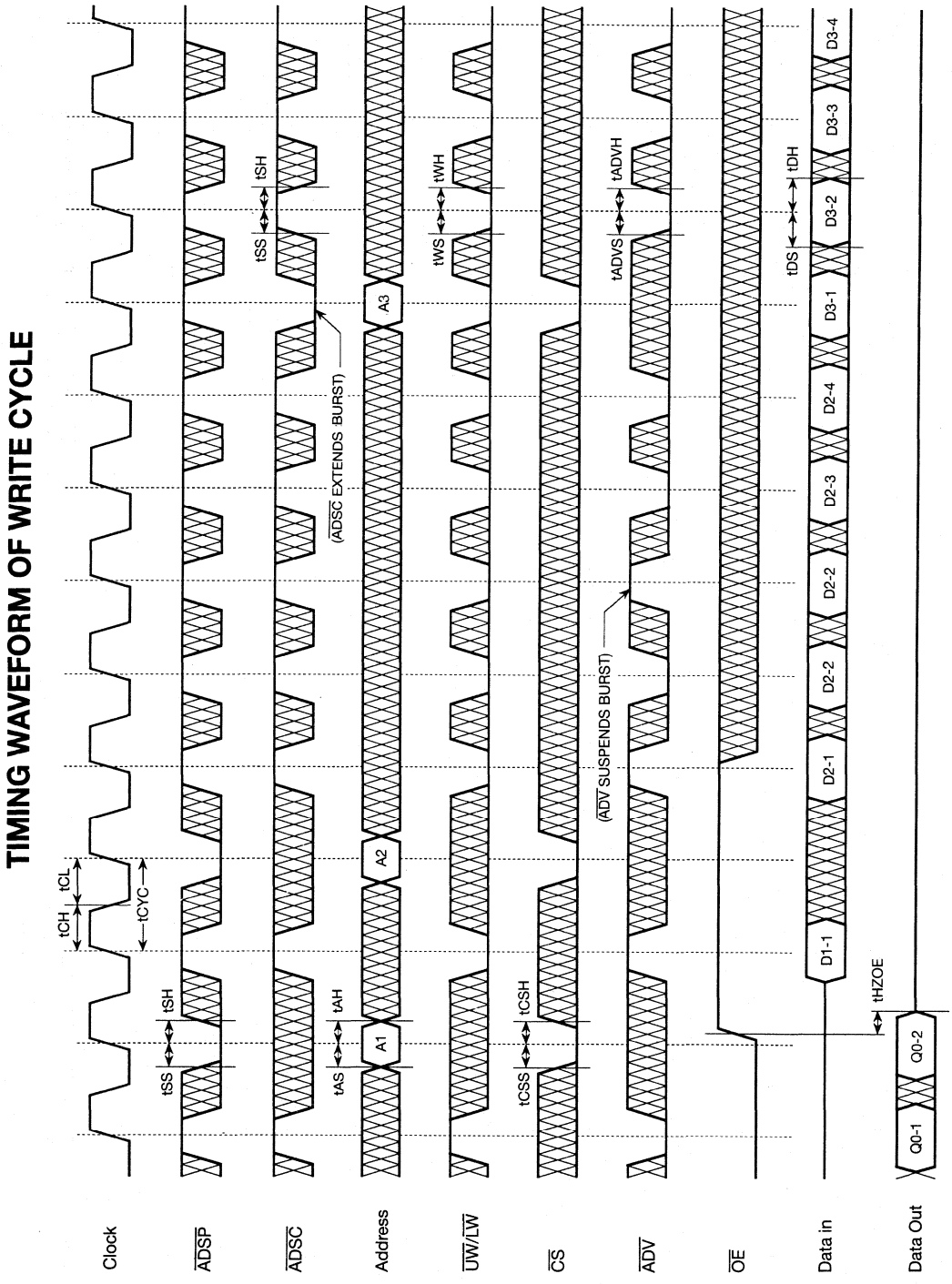


* Including Scope and Jig Capacitance **Fig. 1**

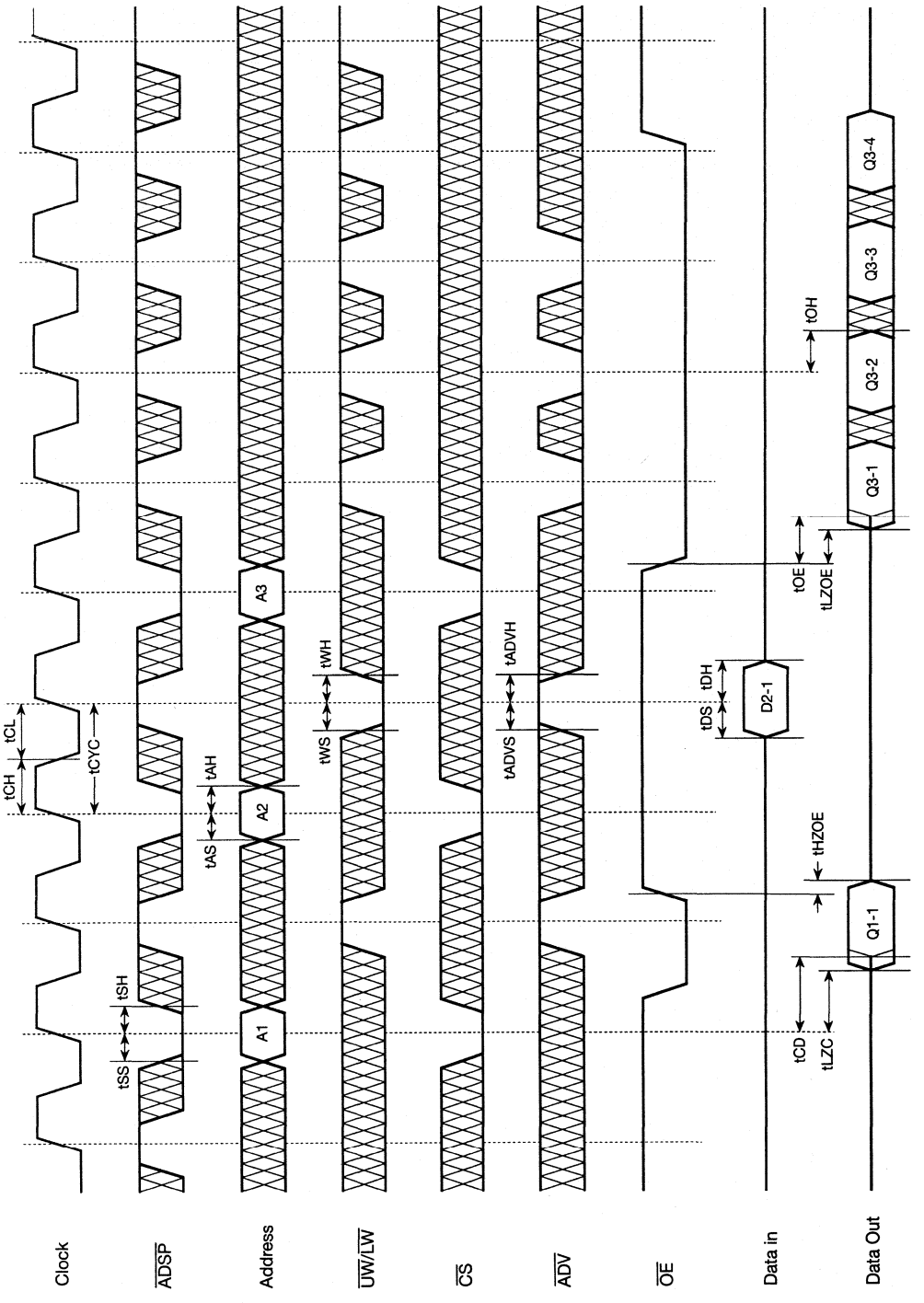
TIMING WAVEFORM OF READ CYCLE



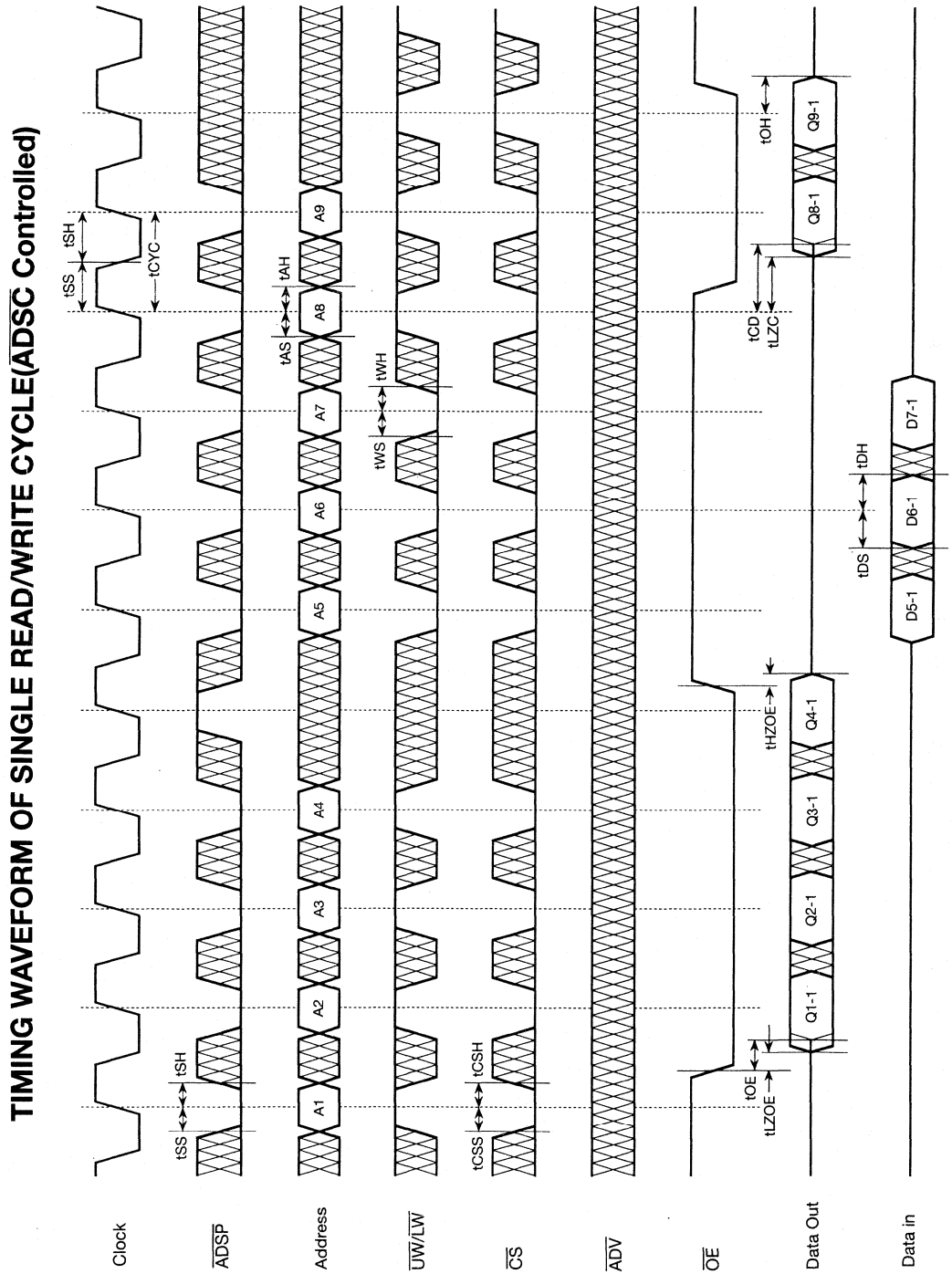
TIMING WAVEFORM OF WRITE CYCLE



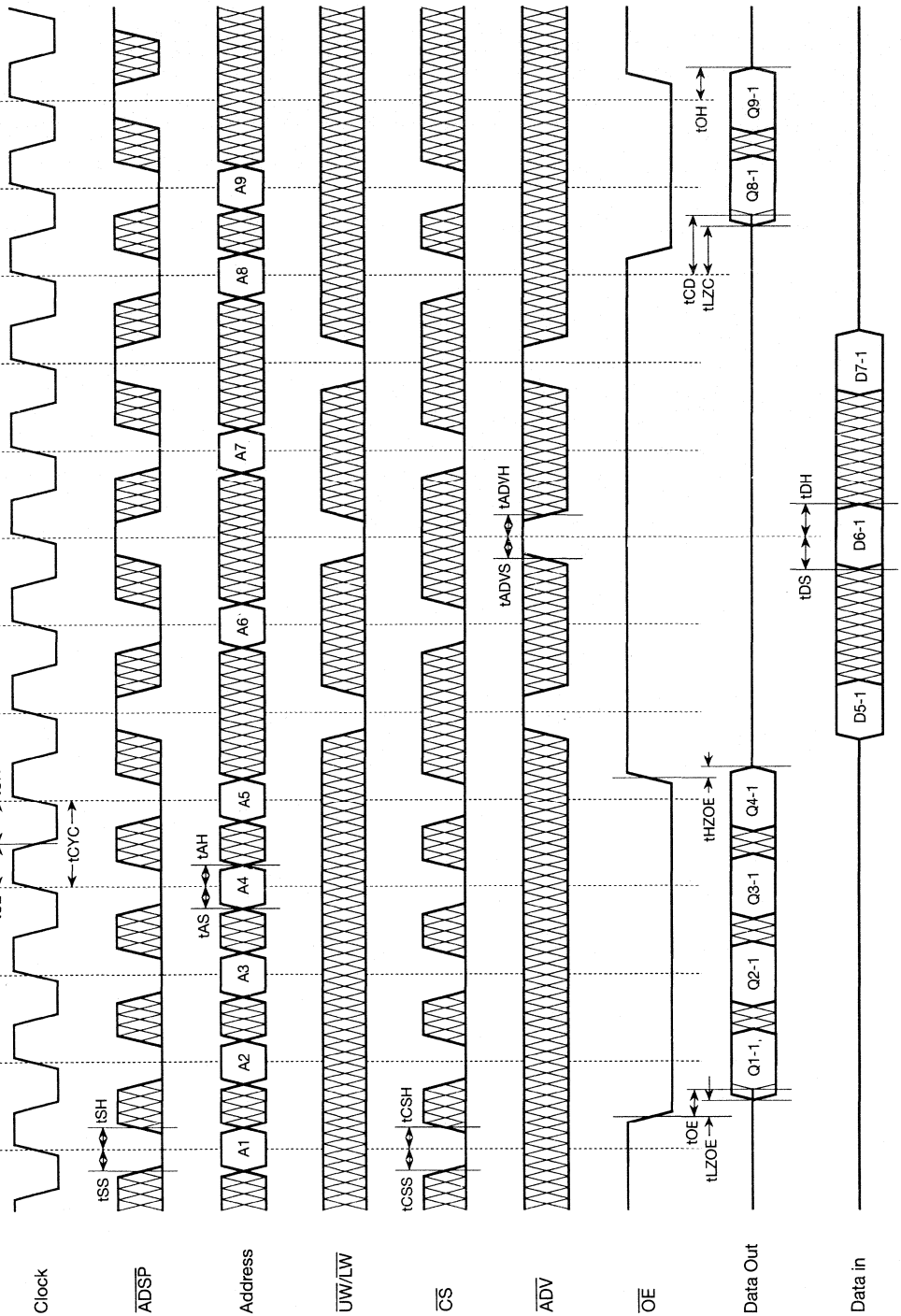
TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSC}$ Controlled)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSP Controlled)



64KX4 Bit High-Speed CMOS Static RAM (With $\overline{OE}$)

FEATURES

- **Fast Access Time: 15, 20, 25ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 40mA (max.)**
  - **(CMOS): 2mA (max)**
  - **Operating KM64258B-15: 140mA (max.)**
  - **KM64258B-20: 130mA (max.)**
  - **KM64258B-25: 120mA (max.)**
- **Single 5V±10% Power Supply**
- **TTL Compatible inputs and outputs**
- **Fully Static Operation**
  - **—No clock or refresh required**
- **Three state Outputs**
- **Standard Pin Configuration**
  - **KM64258BP: 28-DIP-300**
  - **KM64258BJ: 28-SOJ-300**

GENERAL DESCRIPTION

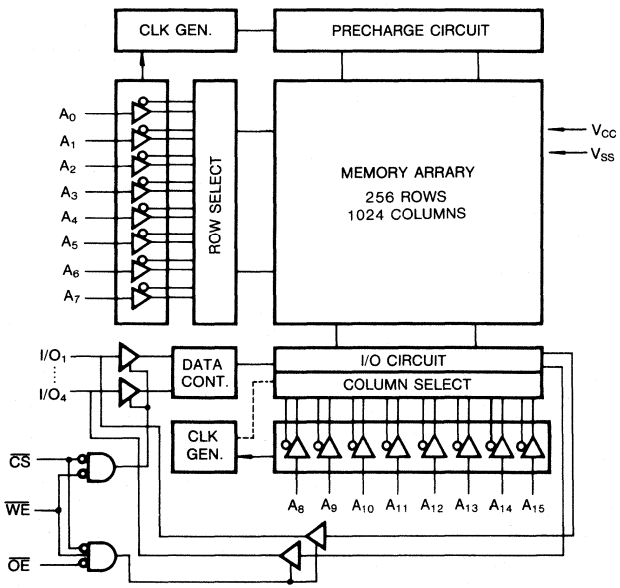
The KM64258B is a 262,144-bit high-speed Static Random Access Memory organized as 65,536 words by 4 bits.

The KM64258B uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology.

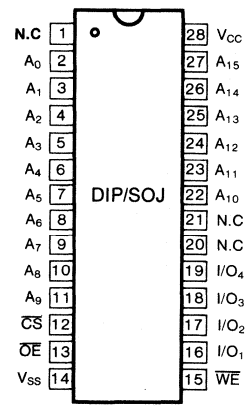
It is particularly well suited for use in high-density high-speed system applications.

The KM64258B is packaged in a 300 mil 28-pin plastic DIP or SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Pin Name	Pin Function
A_0-A_{15}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1~I/O_4	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260°C, 10sec (Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.)=−3.0V for ≤10ns pulse.

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		—	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}		—	2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty, $\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	15ns	—	140	mA
			20ns	—	130	mA
			25ns	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min Cycle		—	40	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, f=0 V_{IN}≥V_{CC}-0.2V or V_{IN}≤0.2V		—	2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4mA		2.4	—	V

CAPACITANCE* (f=1MHz, T_A=25°C)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	7	pF

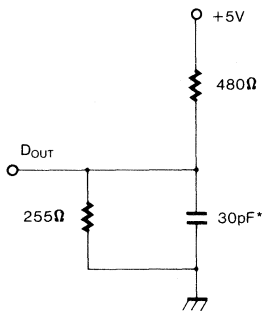
* Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

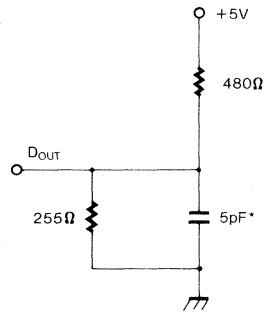
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B) (for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM64258BP-15 KM64258BJ-15		KM64258BP-20 KM64258BJ-20		KM64258BP-25 KM64258BJ-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		20		25		ns
Address Access Time	t_{AA}		15		20		25	ns
Chip Select to Output	t_{CO}		15		20		25	ns
Output Enable to Valid Output	t_{OE}		8		10		12	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	10	0	10	0	10	ns
Output Disable to High-Z Output	t_{OHZ}	0	8	0	8	0	10	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Chip Select to Power Up Time	t_{PU}	0		0		0		ns
Chip Disable to Power Down Time	t_{PD}		15		20		25	ns

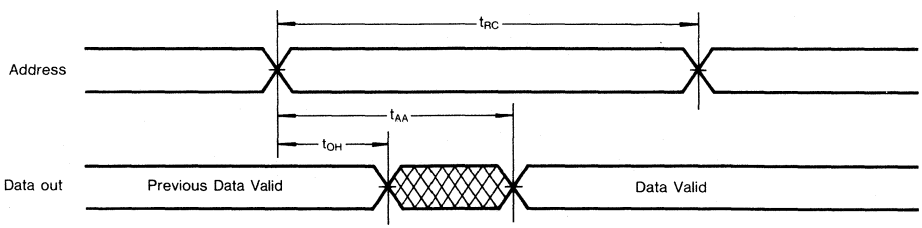
WRITE CYCLE

Parameter	Symbol	KM64258BP-15 KM64258BJ-15		KM64258BP-20 KM64258BJ-20		KM64258BP-25 KM64258BJ-25		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		20		25		ns
Chip Select to End of Write	t_{CW}	12		13		15		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	12		13		15		ns
Write Pulse Width	t_{WP}	12		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	8	0	8	0	10	ns
Data to Write Time Overlap	t_{DW}	9		10		12		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		ns

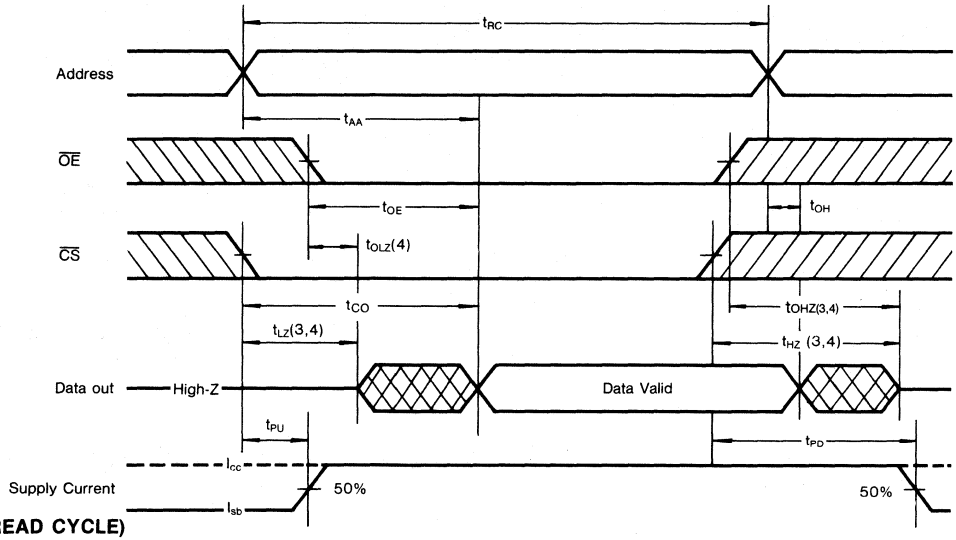
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)



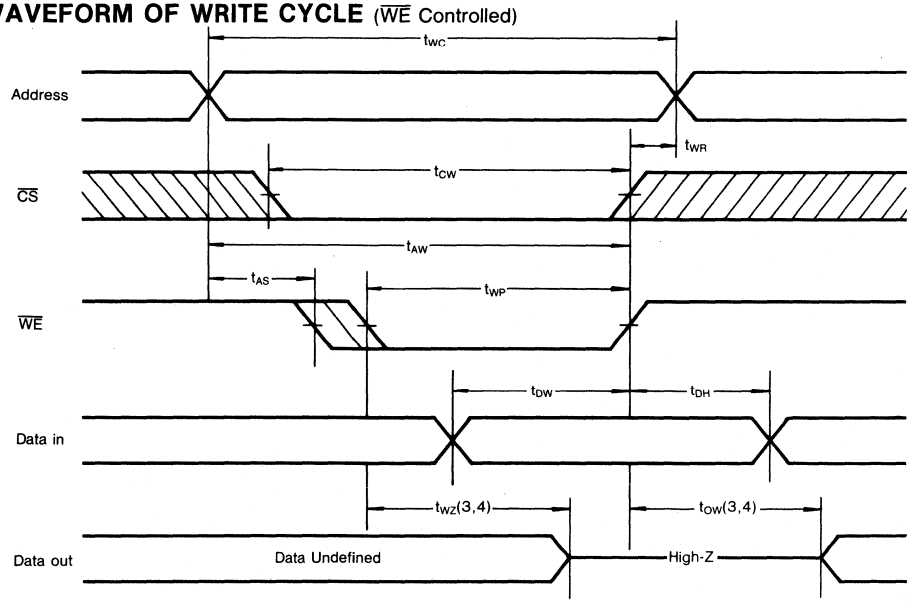
TIMING WAVEFORM OF READ CYCLE



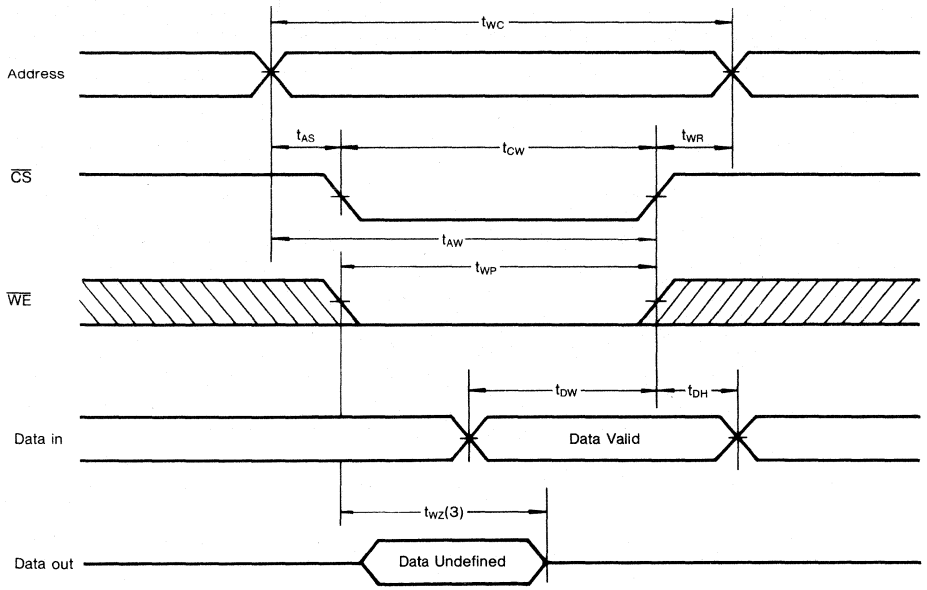
Notes (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Address valid prior to or coincident with $\overline{CS}$ transition low.
6. Device is continuously selected with $\overline{CS}$=V_{IL}.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care

32KX8 Bit High-Speed CMOS Static RAM

FEATURES

- **Fast Access Time: 15, 20, 25ns (max)**
- **Low Power Dissipation**
  - **Standby (TTL) : 40mA (max.)**
  - **2mA(Max.)**
  - **Operating KM68257B-15 : 150mA (max.)**
  - **KM68257B-20 : 140mA (max.)**
  - **KM68257B-25 : 130mA (max.)**
- **Single 5V±10% Power Supply**
- **TTL Compatible inputs and outputs**
- **Fully Static Operation**
  - **—No clock or refresh required**
- **Three State Outputs**
- **Standard Pin Configuration**
  - **KM68257BP : 28-DIP-300**
  - **KM68257BJ : 28-SOJ-300**

GENERAL DESCRIPTION

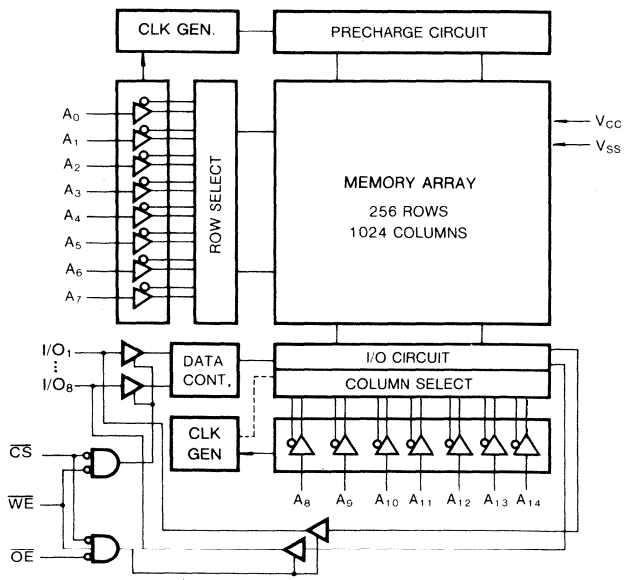
The KM68257B is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.

The KM68257B uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology.

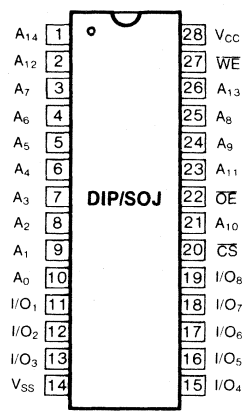
It is particularly well suited for use in high-density high-speed system applications.

The KM68257B is packaged in a 300 mil. 28-pin plastic DIP or SOJ

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1~I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260°C, 10sec (Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.)=−3.0V for ≤10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IN} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, or $V_{I/O}$=Vss to Vcc		-	2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	15ns	-	150	mA
			20ns	-	140	mA
			25ns	-	130	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min Cycle.		-	40	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f= o V_{IN}≥Vcc-0.2 or V_{IN}≤0.2V		-	2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE* (f=1MHz, T_A=25°C)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	7	pF

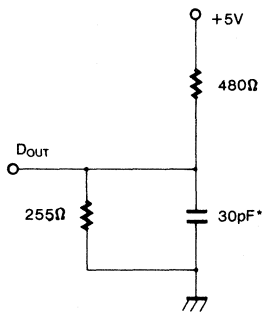
* Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

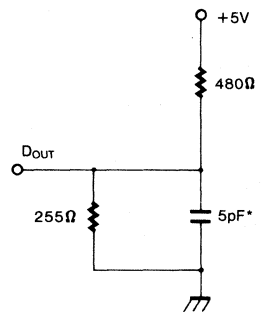
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68257BP-15 KM68257BJ-15		KM68257BP-20 KM68257BJ-20		KM68257BP-25 KM68257BJ-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		20		25		ns
Address Access Time	t_{AA}		15		20		25	ns
Chip Select to Output	t_{CO}		15		20		25	ns
Output Enable to Valid Output	t_{OE}		8		10		12	ns
Chip Enable to Low-Z Output	t_{LZ}	3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	10	0	10	0	10	ns
Chip Disable to High-Z Output	t_{OHZ}	0	8	0	8	0	10	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Chip Select to Power Up Time	t_{PU}	0		0		0		ns
Chip Disable to Power Down Time	t_{PD}		15		20		25	ns

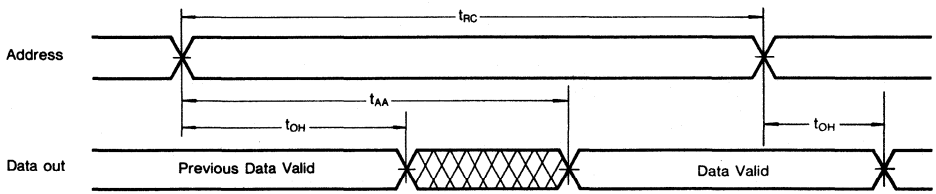
WRITE CYCLE

Parameter	Symbol	KM68257BP-15 KM68257BJ-15		KM68257BP-20 KM68257BJ-20		KM68257BP-25 KM68257BJ-25		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		20		25		ns
Chip Select to End of Write	t_{CW}	12		13		15		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	12		13		15		ns
Write Pulse Width	t_{WP}	12		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	8	0	8	0	10	ns
Data to Write Time Overlap	t_{DW}	9		10		12		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		ns

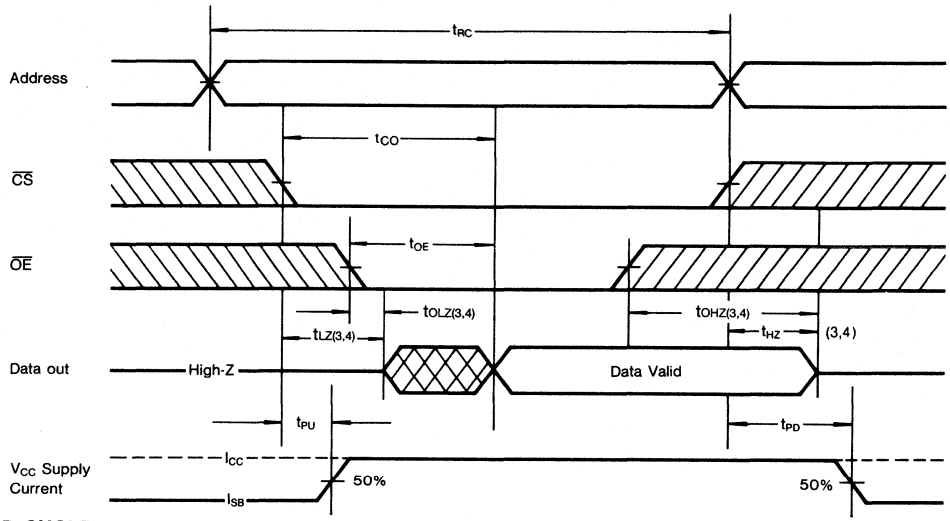
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



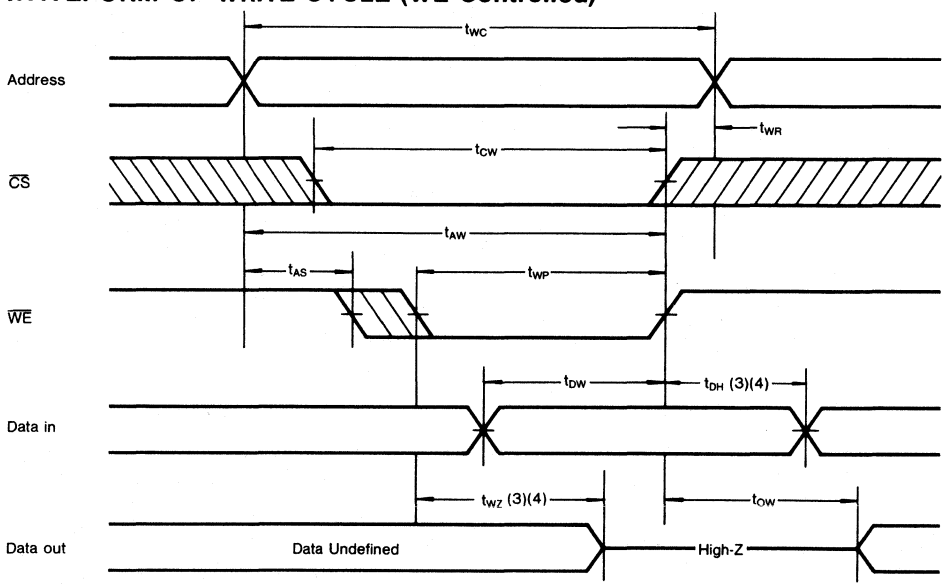
TIMING WAVEFORM OF READ CYCLE



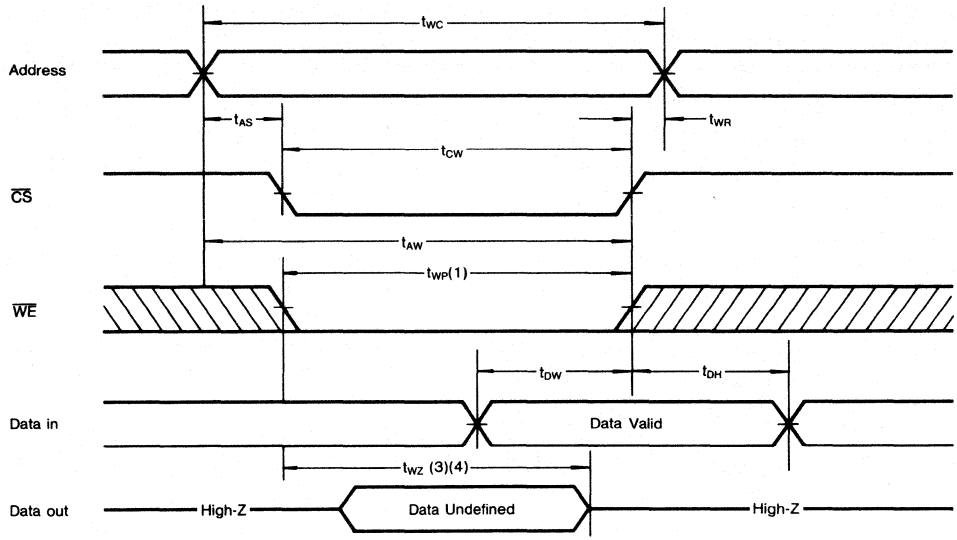
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Address valid prior to or conincident with $\overline{CS}$ transition low
6. Device is continuously selected with $\overline{CS}$=VIL.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X *	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care

32K×8 Bit High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

- **Fast Access Time : 15, 17, 20, 25ns (Max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 30mA (MaX.)**
  - **(CMOS) : 100μA (Max.)**
  - **Operating : KM68V257 -15 : 110mA (Max.)**
  - **KM68V257 -17 : 100mA (Max.)**
  - **KM68V257 -20 : 90mA (Max.)**
  - **KM68V257 -25 : 80mA (Max.)**
- **Single 3.3V±0.3V power supply**
- **TTL compatible inputs and outputs**
- **2V Minimum Data Retention**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three State Output**
- **Standard Pin Configuration**
  - **KM68V257P : 28-DIP-300**
  - **KM68V257J : 28-SOJ-300**

GENERAL DESCRIPTION

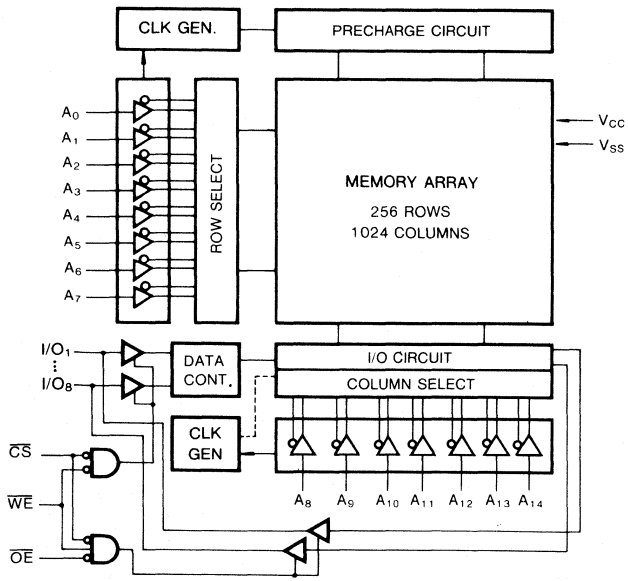
The KM68V257 is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.

The KM68V257 uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.

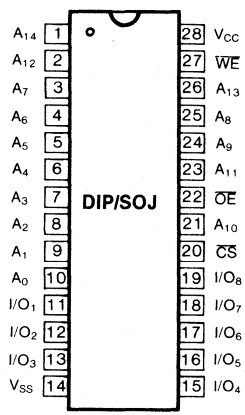
The KM68V257 is designed to operate at 3.3 volts. It is particularly well suited for use in high-density high-speed system applications.

The KM68V257 is packaged in a 300mil 28-pin plastic DIP or SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1~I/O_8	Data Inputs/Outputs
V_{CC}	Power (+3.3V)
V_{SS}	Ground

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 4.6	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 5.5	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

*V_{IL}(min.) = −3.0V for ≤10 ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=3.3±0.3V, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IN} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}		-	2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{out}=0mA	15ns	-	110	mA
			17ns	-	100	mA
			20ns	-	90	mA
			25ns	-	80	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min Cycle.		-	30	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, f= oMHz V_{IN}≥V_{CC}-0.2 or V_{IN}≤0.2V		-	100	μA
Output Low Voltage	V_{OL}	I_{OL}=8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4.0mA		2.4	-	

CAPACITANCE (f=1MHz, T_A=25°C)*

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	6	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	8	pF

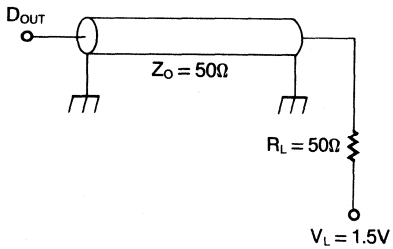
*Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

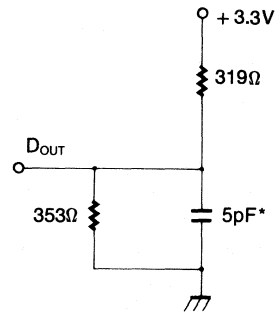
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=3.3±0.3V, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68V257P-15 KM68V257J-15		KM68V257P-17 KM68V257J-17		KM68V257P-20 KM68V257J-20		KM68V257P-25 KM68V257J-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		25		ns
Address Access Time	t_{AA}		15		17		20		25	ns
Chip Select to Output	t_{CO}		15		17		20		25	ns
Output Enable to Valid Output	t_{OE}		8		8		10		12	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	10	0	10	0	10	0	10	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	6	0	8	0	10	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		0		ns
Chip Selection to Power Down Time	t_{PD}		15		17		20		25	ns

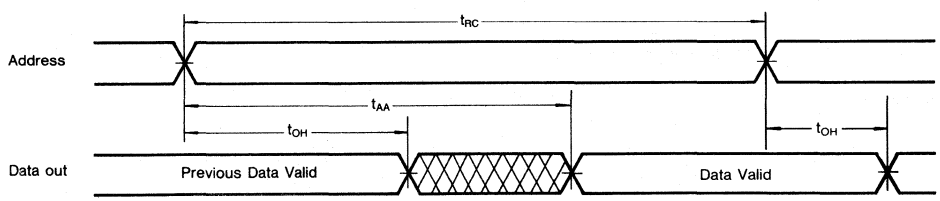
WRITE CYCLE

Parameter	Symbol	KM68V257P-15 KM68V257J-15		KM68V257P-17 KM68V257J-17		KM68V257P-20 KM68V257J-20		KM68V257P-25 KM68V257J-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		25		ns
Chip Select to End of Write	t_{CW}	12		12		13		14		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AW}	12		12		13		14		ns
Write Pulse Width	t_{WP}	12		12		13		14		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WZ}	0	6	0	6	0	8	0	10	ns
Data to Write Time Overlap	t_{DW}	8		8		10		12		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		0		ns

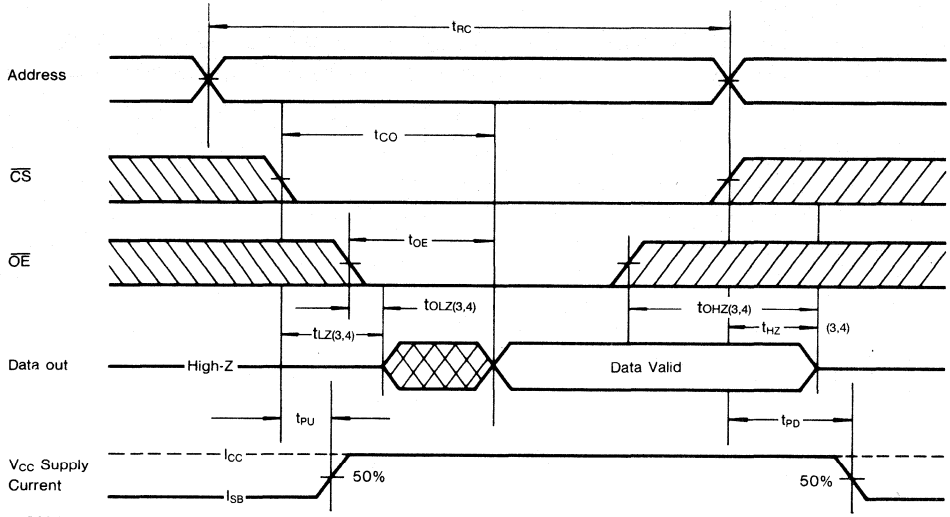
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



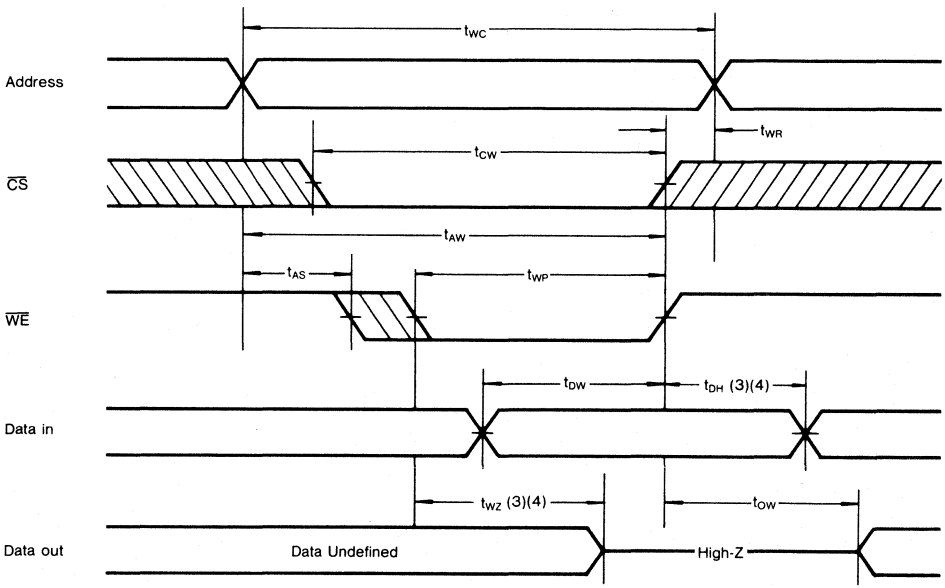
TIMING WAVEFORM OF READ CYCLE



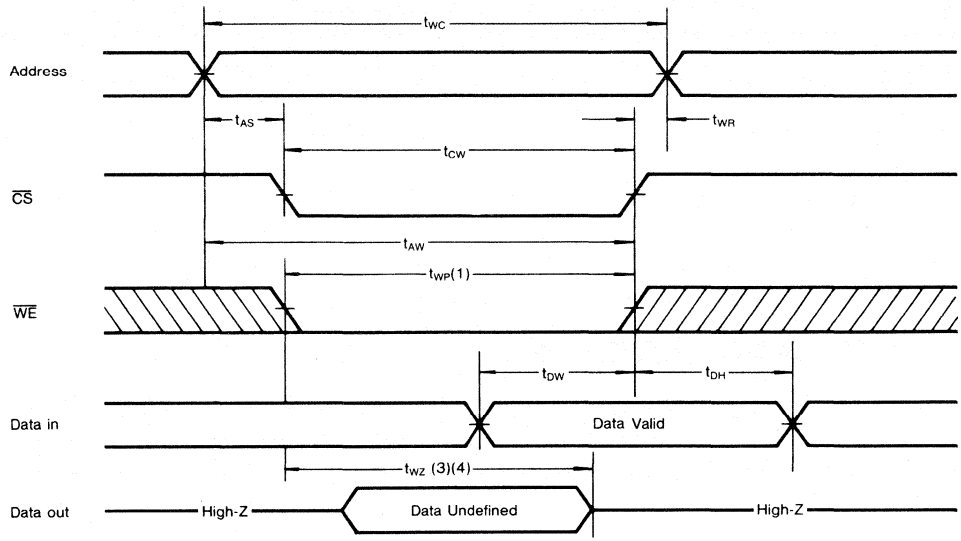
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Address valid prior to or conincident with $\overline{CS}$ transition low
6. Device is continuously selected with $\overline{CS}$=V_{IL}.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X *	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

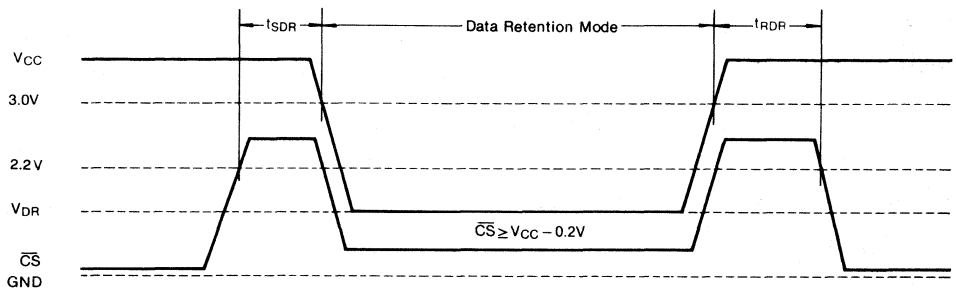
* Note: X means Don't Care

DATA RETENTION CHARACTERISTICS* (T_A=0 to 70°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}-0.2V$	2	-	3.6	V
Data Retention Current	I_{DR}	V_{CC}=0.3V, $\overline{CS} \geq V_{CC}-0.2V$ $V_{IN} \geq 0.2V$ or $V_{IN} \leq 0.2V$	-	1**	50	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention	0	-	-	ns
Recovery Time	t_{RDR}	Wave forms(below)	t_{RC}*	-	-	ns

* t_{RC}=Read Cycle time
**Temp=25° C

DATA RETENTION WAVEFORM



32,768 WORD x 16 BIT High-Speed CMOS Static RAM

FEATURES

- **Fast Access Time : 15, 17, 20, 25ns(max.)**
- **Low Power Dissipation**

Standby	**(TTL)**	**: 50mA (max.)**
	(CMOS)	**: 1mA (max.)**
Operating	**KM616513-15**	**: 210mA (max.)**
	KM616513-17	**: 200mA (max.)**
	KM616513-20	**: 190mA (max.)**
	KM616513-25	**: 180mA (max.)**

- **Single 5V±10% power supply**
- **TTL compatible inputs and outputs**
- **Data Byte Control($\overline{LB}$: I/O1~I/O8, $\overline{UB}$: I/O9~I/O16)**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three state Output**
- **Center Power/Ground Pin Configuration**
- **Standard Pin Configuration**
  KM616513J : 40-Pin SOJ(400mil)

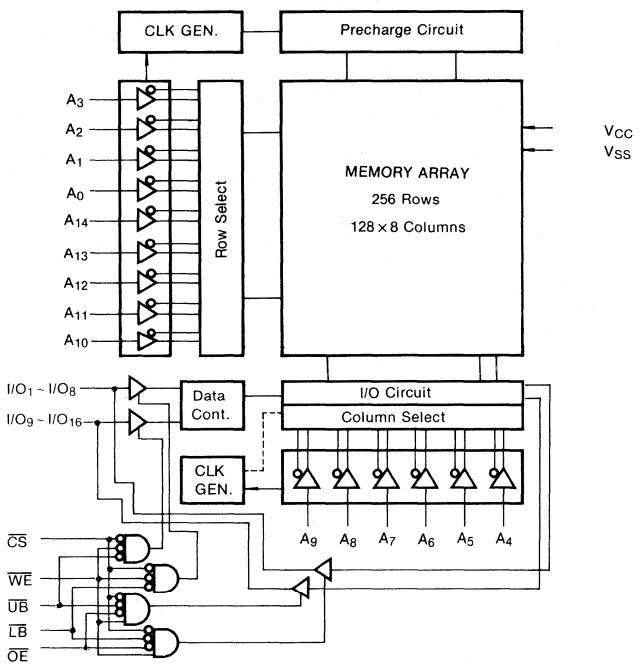
GENERAL DESCRIPTION

The KM616513 is a 524,288-bit high speed static random access memory organized as 32,768 words by 16 bits.

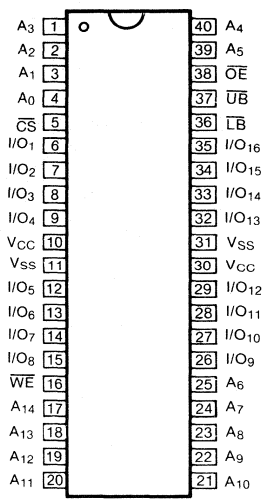
The KM616513 uses sixteen common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM616513 is packaged in a 400 mil. 40-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Input
I/O_1-I/O_{16}	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.5	W
Storage Temperature	T_{stg}	-65 to +150	°C
Operating Temperature	T_a	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.5*	—	0.8	V

* V_{IL}(min)=-3.0V for≤10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-2	+2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT}=V_{SS} to V_{CC}		-2	+2	μA
Average Operating Current	I_{CC1}	Min Cycle, 100% Duty	15ns	-	210	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0mA	17ns	-	200	
			20ns	-	190	
			25ns	-	180	
	I_{CC2}	Min Cycle, 100% Duty	15ns	-	150	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0mA	17ns	-	140	
		$\overline{UB}$=V_{IL}, $\overline{LB}$=V_{IH} or	20ns	-	130	
		$\overline{UB}$=V_{IH}, $\overline{LB}$=V_{IL}	25ns	-	120	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, V_{IN}=V_{IH}/V_{IL}, Min. Cycle		-	50	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V		-	1	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4.0mA		2.4	-	V

CAPACITANCE (f=1MHz, T_A=25°C)

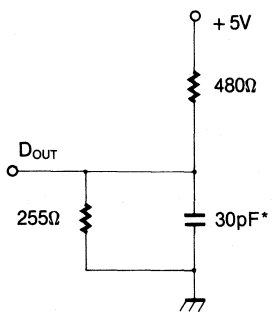
Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Capacitance is sampled and not 100% tested.

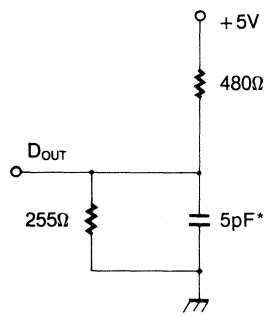
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{OLZ}, t_{OHZ}, t_{HZ}, t_{LZ}, t_{OW} & t_{WZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM616513-15		KM616513-17		KM616513-20		KM616513-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		25		ns
Address Access Time	t_{AA}		15		17		20		25	ns
Chip Select to Output	t_{ACS}		15		17		20		25	ns
Output Enable to Valid Output	t_{OE}		7		9		10		13	ns
$\overline{LB}$,$\overline{UB}$ Access Time	t_{BA}		15		17		20		25	ns
Output Enable to Low-Z Output	t_{OLZ}	2		2		3		3		ns
Chip Enable to Low-Z Output	t_{LZ}	5		5		5		5		ns
$\overline{LB}$,$\overline{UB}$ Enable to Low-Z Output	t_{BLZ}	5		5		5		5		ns
Output Disable to High-Z Output	t_{OHZ}	0	7	0	7	0	8	0	8	ns
Chip Disable to High-Z Output	t_{HZ}	0	8	0	8	0	9	0	9	ns
$\overline{LB}$,$\overline{UB}$ Disable to High-Z Output	t_{BHZ}	0	8	0	8	0	9	0	9	ns
Output Hold from Address Change	t_{OH}	5		5		5		5		ns

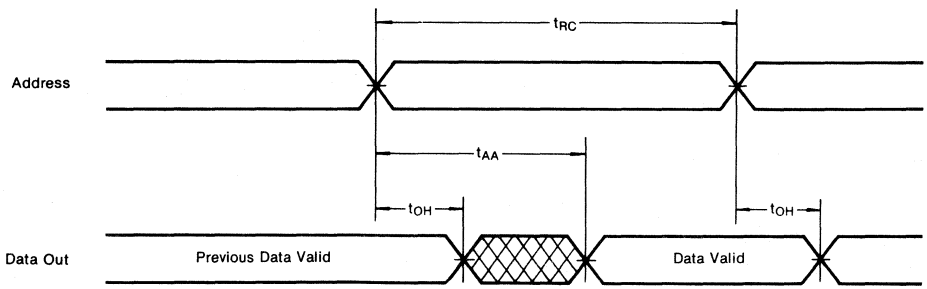
WRITE CYCLE

Parameter	Symbol	KM616513-15		KM616513-17		KM616513-20		KM616513-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		25		ns
Chip Select to End of Write	t_{CW}	11		12		13		15		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AW}	11		12		13		15		ns
Write Pulse Width	t_{WP}	9		9		10		12		ns
$\overline{LB}$,$\overline{UB}$ Valid to End of Write	t_{BW}	10		12		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WZ}	0	9	0	9	0	10	0	10	ns
Data to Write Time Overlap	t_{DW}	6		8		9		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		5		5		ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

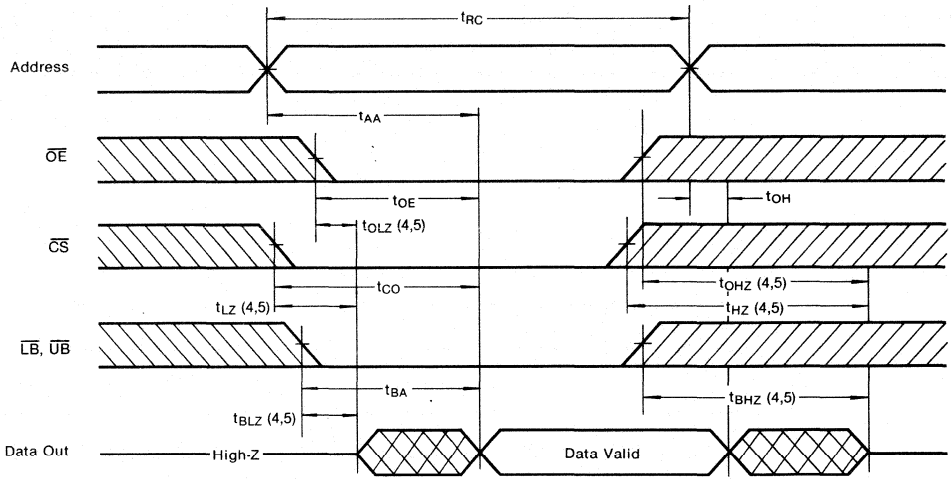
($\overline{CS}$=V_{IL}, $\overline{WE}$=V_{IH})



SAMSUNG ELECTRONICS

TIMING DIAGRAMS

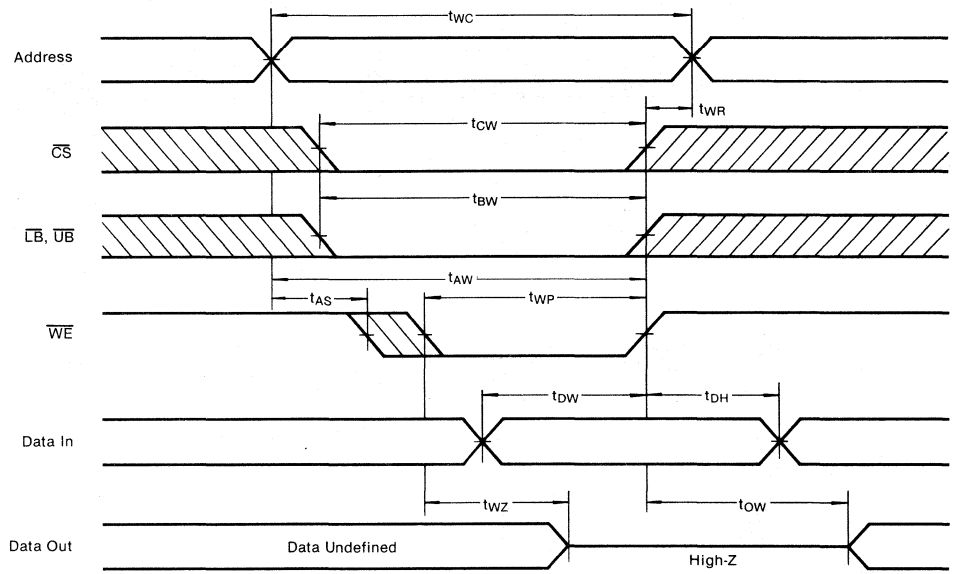
TIMING WAVEFORM OF READ CYCLE



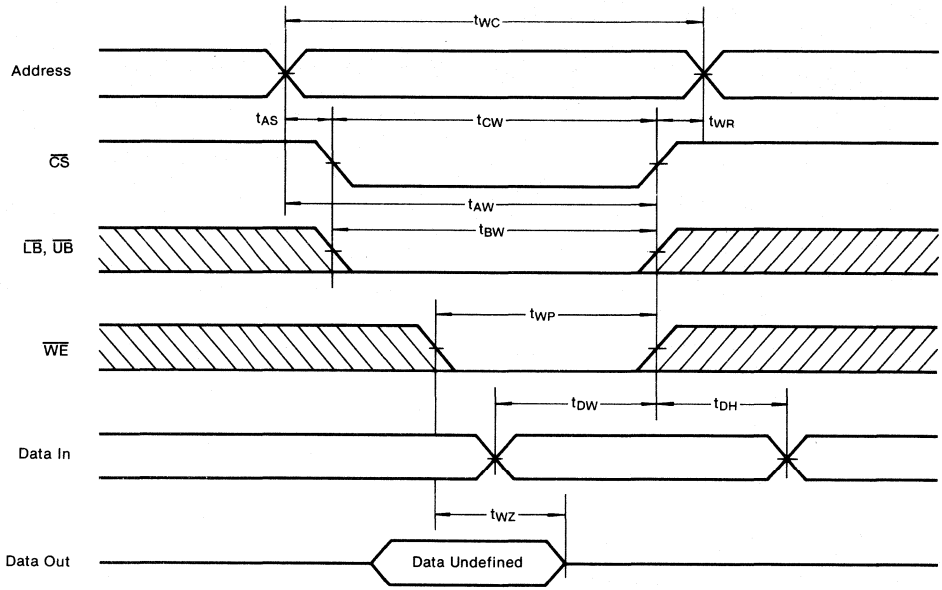
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Device is continuously selected with $\overline{CS} = V_{IL}$.
6. Address valid prior to or coincident with $\overline{CS}$ transition low.

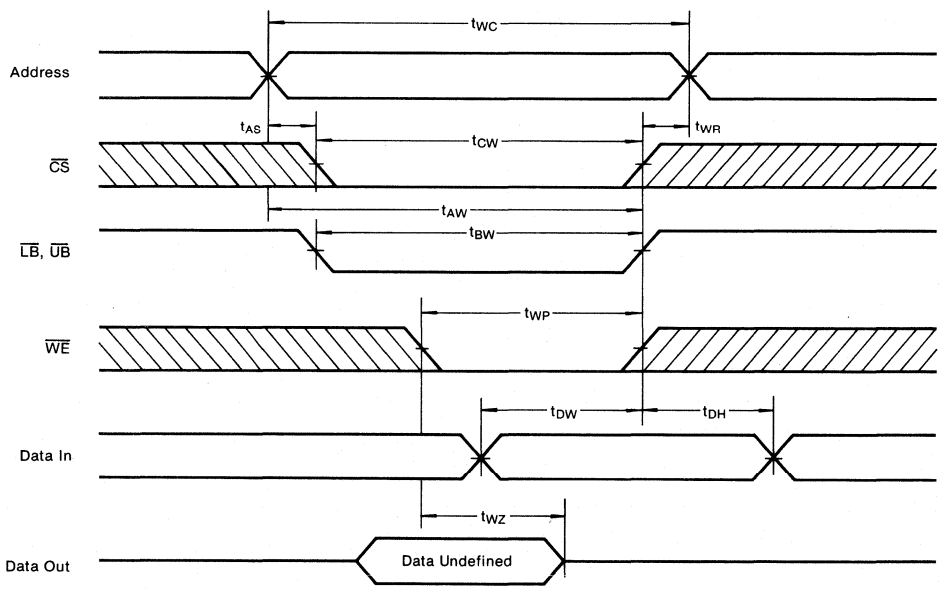
TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{LB}$, $\overline{UB}$ Controlled)



Note(WRITE CYCLE)

1. A write occures during the overlap(t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
   A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low.
   A write end at the earlist transition among $\overline{CS}$ going high and $\overline{WE}$ going high.
2. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
5. If $\overline{OE}$, $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
7. Dout is the read data of the new address.
8. When $\overline{CS}$ is low ; I/O pins are in the output state.
   The input signals in the opposite phase leading to the output should not be applied.

2

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O_1~I/O_8	I/O_9~I/O_{16}	
H	X	X*	X	X	Not Select	High-Z	High-Z	I_{SB}, I_{SB1}
L	X	X	H	H				
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

* Note : X means Don't care

32,768 WORD x 16 Bit High-Speed CMOS Static RAM(3.3V Operating)

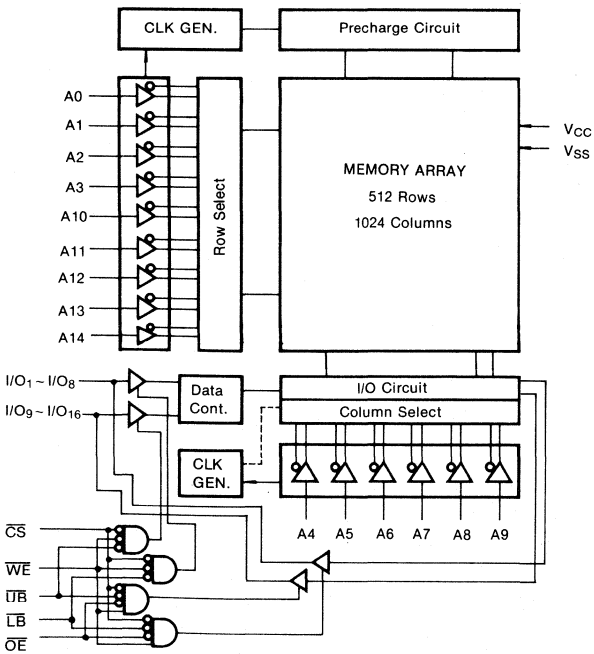
FEATURES

- **Fast Access Time : 17, 20, 25ns(max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 3mA (max.)**
  - **(CMOS) : 100μA (max.)**
  - **Operating KM616V513-17 : 130mA (max.)**
  - **KM616V513-20 : 120mA (max.)**
  - **KM616V513-25 : 110mA (max.)**
- **Single 3.3V±0.3V power supply**
- **TTL compatible inputs and outputs**
- **Data Byte Control($\overline{LB}$: I/O1~I/O8, $\overline{UB}$: I/O9~I/O16)**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three state Output**
- **Center Power/Ground Pin Configuration**
- **Standard Pin Configuration**
  KM616V513J : 40-Pin SOJ(400mil)

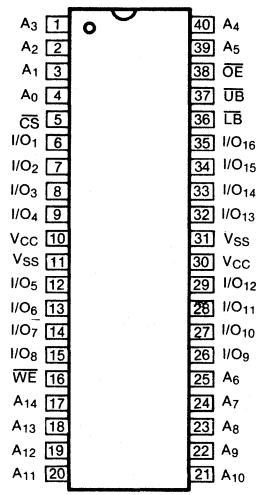
GENERAL DESCRIPTION

The KM616V513 is a 524,288-bit high-speed static random access memory organized as 32,768 words by 16bits.
The KM616V513 uses sixteen common input and output lines and has an output enable pin which operates faster than address access time at read cycle.
The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.
The KM616V513 is designed to operate at 3.3V It is particularly well suited for use in high-density high-speed system applications.
The KM616V513 is packaged in a 400mil 40-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A14	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$, $\overline{UB}$	Data Byte Control Inputs
I/O1~I/O16	Data Input/Outputs
VCC	Power(+3.3V)
VSS	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to V_{CC} + 0.5	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	-65 to + 150	°C
Operating Temperature	T_a	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.3*	—	0.8	V

* V_{IL}(min)=-3.0V for $\leq$ 10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=3.3V $\pm$ 0.3V, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-2	+2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT}=V_{SS} to V_{CC}		-2	+2	μA
Average Operating Current	I_{CC1}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{OUT}=0mA	17ns	-	130	mA
			20ns	-	120	
			25ns	-	110	
	I_{CC2}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{OUT}=0mA $\overline{UB}$=V_{IL}, $\overline{LB}$=V_{IH} or $\overline{UB}$=V_{IH}, $\overline{LB}$=V_{IL}	17ns	-	90	mA
			20ns	-	80	
			25ns	-	70	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, V_{IN}=V_{IH}/V_{IL}, Min Cycle		-	3	mA
	I_{SB1}	$\overline{CS}$ $\geq$ V_{CC}-0.2V, f=0MHz V_{IN} $\leq$ 0.2V or V_{CC} $\geq$ V_{CC}-0.2V		-	100	μA
Output Low Voltage	V_{OL}	I_{OL}=8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4.0mA		2.4	-	V

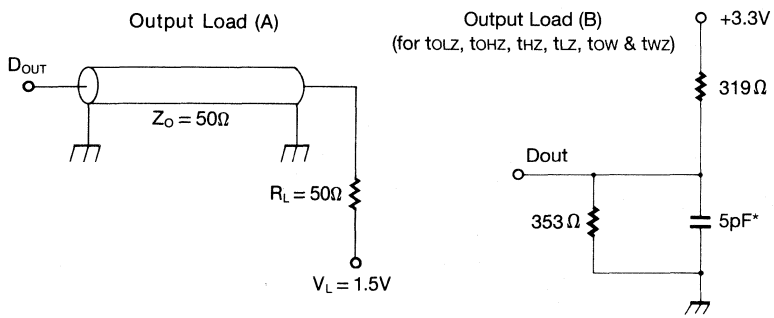
CAPACITANCE (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Capacitance is sampled and not 100% tested.

TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=3.3V±0.3, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	See below



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM616V513-17		KM616V513-20		KM616V513-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	17		20		25		ns
Address Access Time	t_{AA}		17		20		25	ns
chip Select to Output	t_{ACS}		17		20		25	ns
Output Enable to Output	t_{OE}		8		10		13	ns
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}		17		20		25	ns
Output Enable to Low-Z Output	t_{OLZ}	3		3		3		ns
Chip Enable to Low-Z Output	t_{LZ}	5		5		5		ns
$\overline{LB}$, $\overline{UB}$ Enable to Low-Z Output	t_{BLZ}	5		5		5		ns
Output Disable to High-Z Output	t_{OHZ}	0	8	0	8	0	8	ns
Chip Disable to High-Z Output	t_{HZ}	0	9	0	9	0	9	ns
$\overline{LB}$, $\overline{UB}$ Disable to High-Z Output	t_{BHZ}	0	9	0	9	0	9	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns

WRITE CYCLE

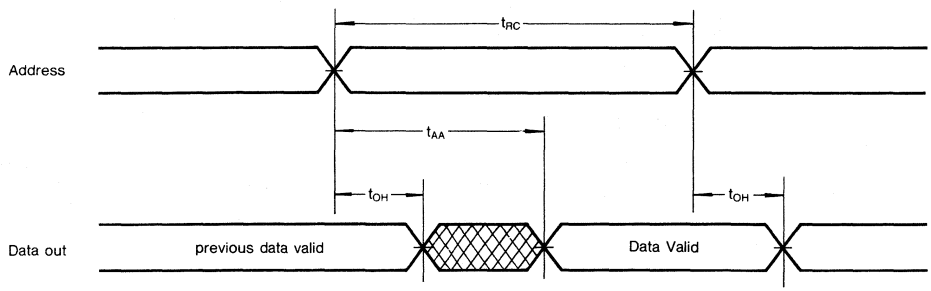
Parameter	Symbol	KM616V513-17		KM616V513-20		KM616V513-25		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	17		20		25		ns
Chip Select to End of Write	t_{CW}	14		15		16		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	14		15		16		ns
Write Pulse Width	t_{WP}	11		13		15		ns
$\overline{LB}$, $\overline{UB}$ Valid to End of Write	t_{BW}	11		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	10	0	10	0	10	ns
Data to Write Time Overlap	t_{DW}	8		9		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End of Write to Output Low-Z	t_{OW}	5		5		5		ns

2

TIMING DIAGRAMS

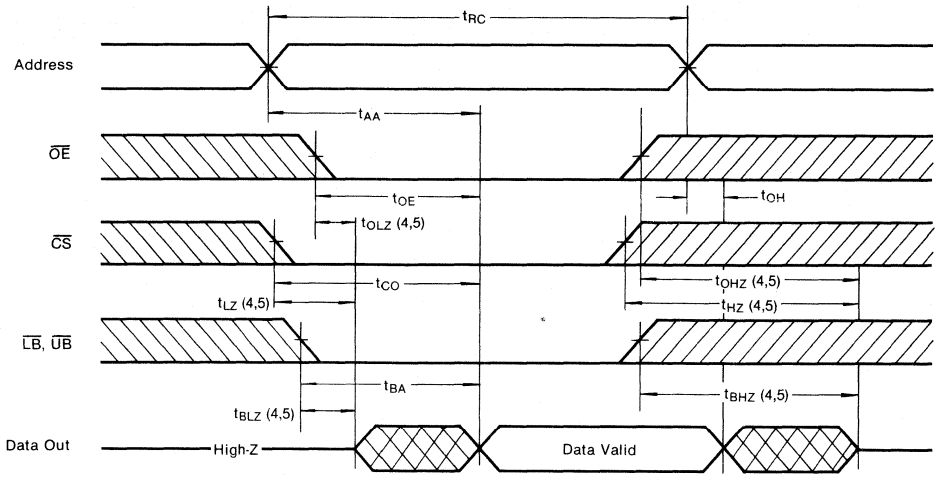
TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



TIMING DIAGRAMS

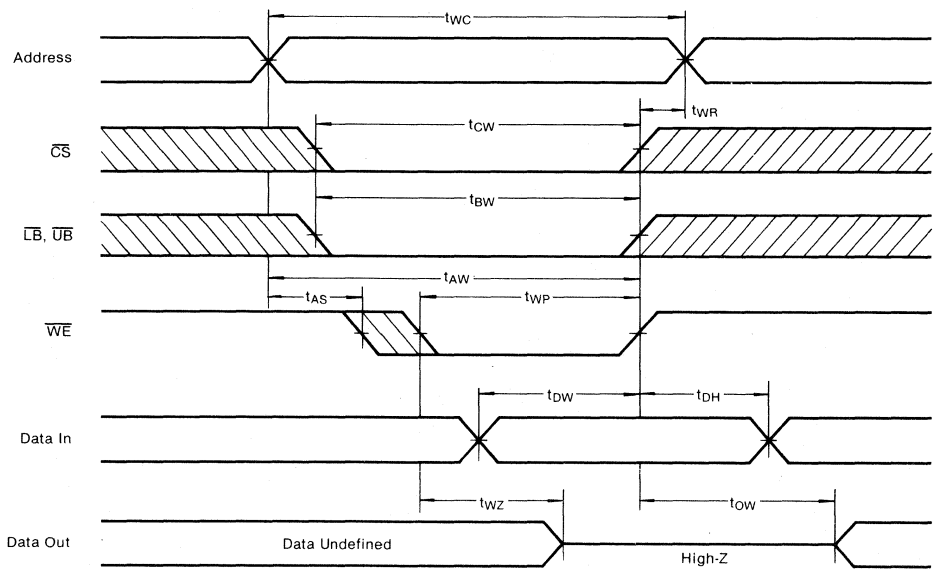
TIMING WAVEFORM OF READ CYCLE



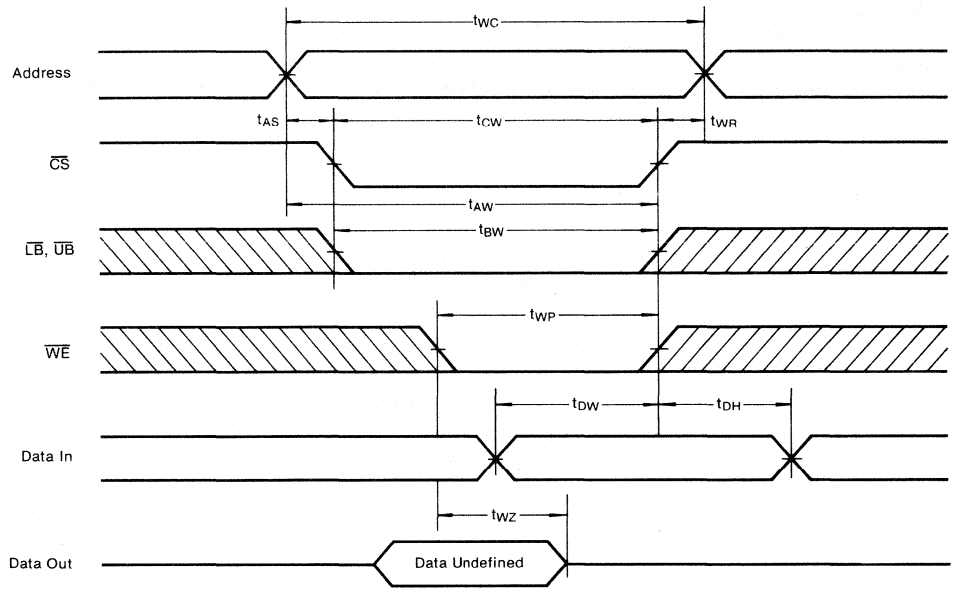
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Device is continuously selected with $\overline{CS} = V_{IL}$.
6. Address valid prior to or coincident with $\overline{CS}$ transition low.

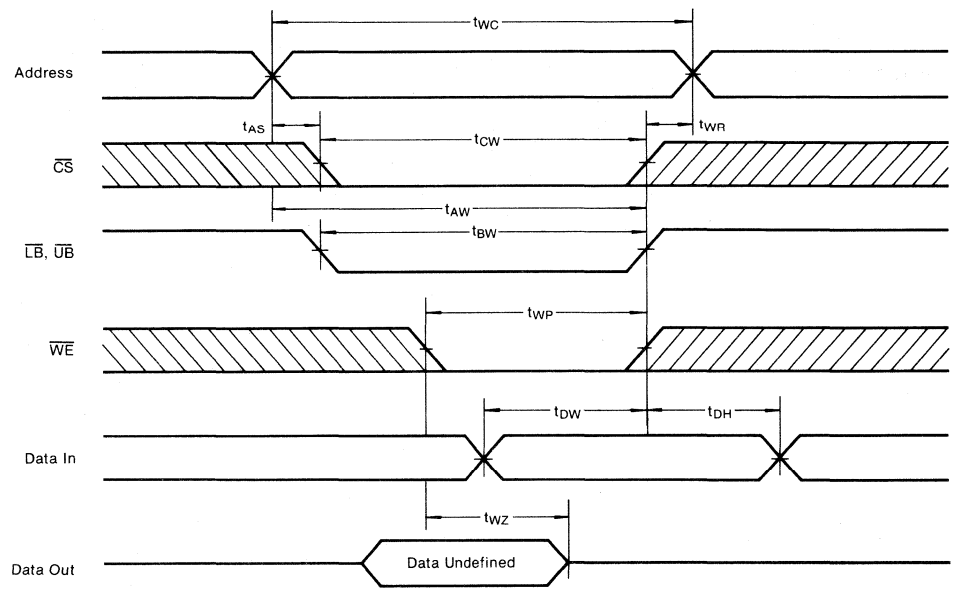
TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{LB}$, $\overline{UB}$ Controlled)



Note(WRITE CYCLE)

1. A write occures during the overlap(t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
   A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low.
   A write end at the earlist transition among $\overline{CS}$ going high and $\overline{WE}$ going high.
2. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
5. If $\overline{OE}$, $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
7. Dout is the read data of the new address.
8. When $\overline{CS}$ is low ; I/O pins are in the output state.
   The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O_1~I/O_8	I/O_9~I/O_{16}	
H	X	X*	X	X	Not Select	High-Z	High-Z	I_{SB}, I_{SB1}
L	X	X	H	H				
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

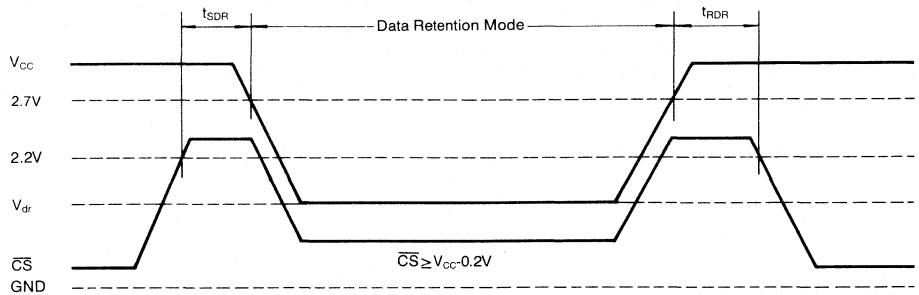
* Note : X means Don't care

DATA RETENTION CHARACTERISTICS (T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V	2		3.6	V
Data Retention Current	I_{DR}	$\overline{CS} \geq V_{CC}$-0.2V		1	100	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Wave forms (below)	0			ns
Recovery Time	t_{RDR}		t_{RC}*			ns

*t_{RC} = Read cycle time

DATA RETENTION WAVEFORM ($\overline{CS}$ Controlled)



1,048,576 WORD x 1 Bit High-Speed CMOS Static RAM

FEATURES

- **Fast Access Time : 20, 25, 35ns(max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 40mA (max.)**
  - **(CMOS) : 100μA (max.) L-ver. only**
  - **2mA (max.)**
  - **Operating KM611001-20 : 130mA (max.)**
  - **KM611001-25 : 110mA (max.)**
  - **KM611001-35 : 100mA (max.)**
- **Single 5V±10% power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three state Output**
- **Low Data Retention Voltage : 2V(min.) L-ver. only**
- **Standard Pin Configuration**
  - **KM611001P/LP : 28-pin DIP(400mil)**
  - **KM611001J/LJ : 28-pin SOJ (400mil)**

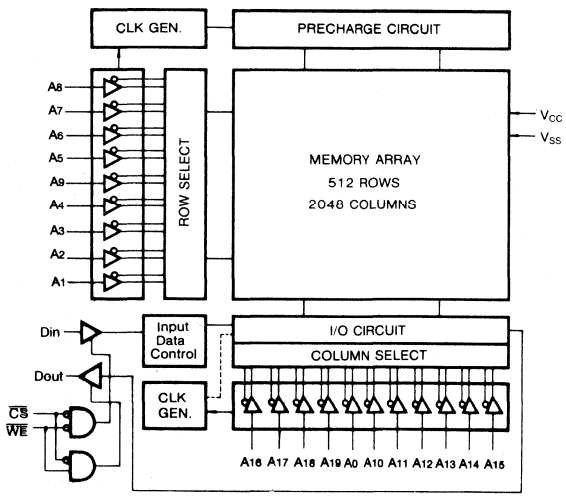
GENERAL DESCRIPTION

The KM611001/L is a 1,048,576-bit high-speed static random access memory organized as 1,048,576 words by 1 bit.

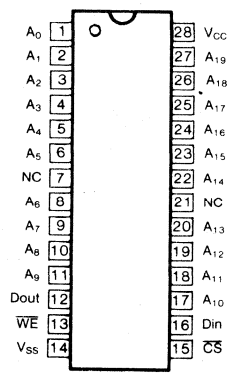
The KM611001/L has separate input and output lines for fast read and write access. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM611001/L packaged in a 400mil 28-pin plastic DIP or SOJ with the conventional power supply paint.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A19	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
DIN	Data Input
DOUT	Data Output
VCC	Power(+5V)
VSS	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	-65 to + 150	°C
Operating Temperature	T_a	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.5*	—	0.8	V

* V_{IL}(min.)=-3.0V for $\leq$ 10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V $\pm$ 10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT}=V_{SS} to V_{CC}		-	2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{OUT}=0mA	20ns	-	130	mA
			25ns	-	110	mA
			35ns	-	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min Cycle		-	40	mA
	I_{SB1}	$\overline{CS}$ $\geq$ V_{CC}-0.2V, f=0MHz V_{IN} $\leq$ 0.2V or V_{IN} $\geq$ V_{CC}-0.2V		-	2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4mA		2.4	-	V

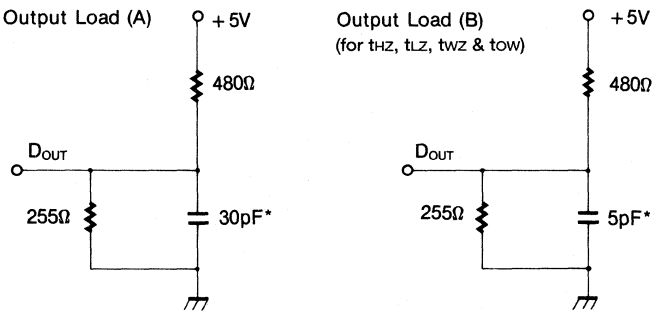
CAPACITANCE (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

* Capacitance is sampled and not 100% tested.

TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	See below



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20		25		35		ns
Address Access Time	t_{AA}		20		25		35	ns
Chip Select to Output	t_{CO}		20		25		35	ns
Chip Select to Low-A Output	t_{LZ}	5		5		5		ns
Chip Disable to High-Z Output	t_{HZ}	0	12	0	15	0	15	ns
Output Hold from Address Change	t_{OH}	3		5		5		ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		ns
Chip Deselection to Power Down Time	t_{PD}		20		25		35	ns

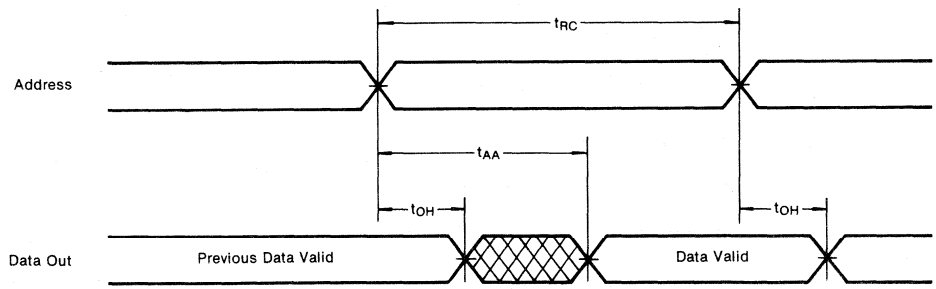
WRITE CYCLE

Parameter	Symbol	-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	20		25		35		ns
Chip Select to End of Write	t_{CW}	17		20		30		ns
Address Valid to End of Write	t_{AW}	17		20		30		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	15		20		25		ns
Write Recovery Time	t_{WR}	2		3		3		ns
Write to Output High-Z	t_{WZ}	0	8	0	10	0	12	ns
Data to Write Time Overlap	t_{DW}	12		15		20		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		ns

TIMING DIAGRAMS

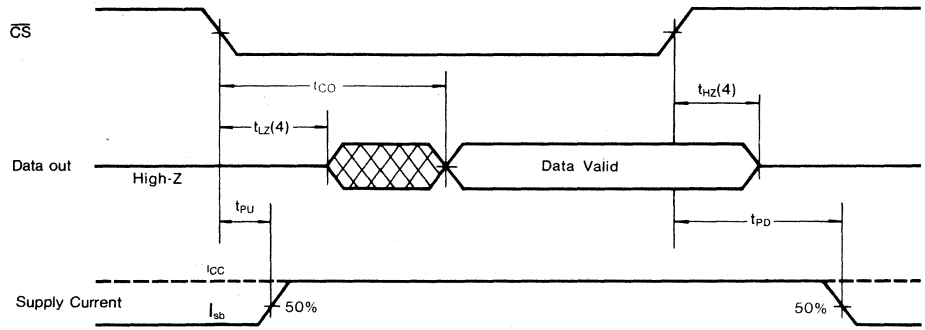
TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CE}$=V_{IL}, $\overline{WE}$=V_{IH})



SAMSUNG ELECTRONICS

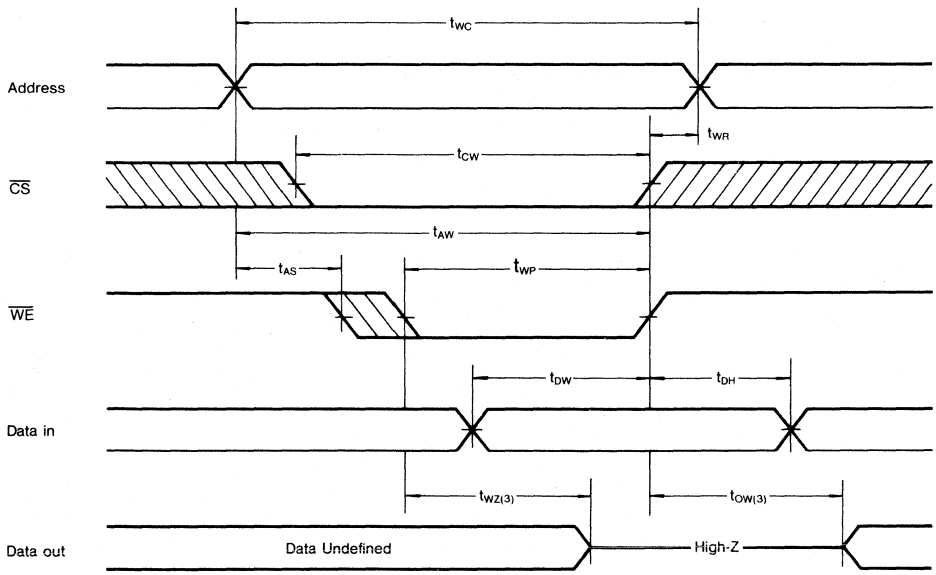
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



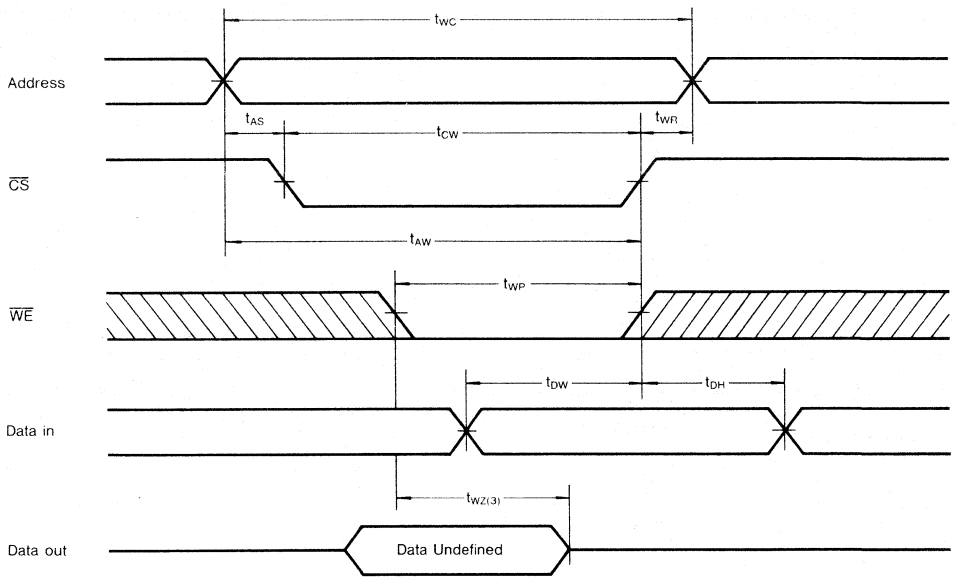
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Device is continuously selected with $\overline{CS}$=V_{IL}
6. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	Dout PIN	Supply Current	Mode
H	X*	High-Z	I_{sb}, I_{sb1}	Not Select
L	H	Dout	I_{CC}	Read
L	L	High-Z	I_{CC}	Write

*Note: X means Don't Care

32K x 9 Synchronous Burst Cache RAM with Self-Timed Write

FEATURES

- **Synchronous Operation**
- **On-Chip Address Counter.**
- **Self-Timed Write Cycle.**
- **On- Chip Address and Control Registers.**
- **High Capacitive Load (85pF) Drivers.**
- **Single 5V ± 10% Power Supply.**
- **Two Chip Selects.**
- **Asynchronous Output Enable Control.**
- **$\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.**
- **TTL-Level Three-State Outputs.**
- **TTL Compatible Inputs.**
- **44-Pin PLCC Package.**

FAST ACCESS TIMES

Parameter	Symbol	-14	-19	-24	Unit
Cycle Time	t_{CYC}	20	25	30	ns
Clock Access Time	t_{CD}	14	19	24	ns
Output Enable Access Time	t_{OE}	6	7	8	ns

GENERAL DESCRIPTION

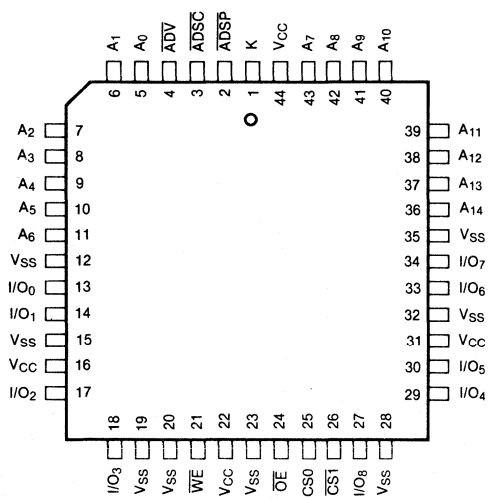
The KM79C86 is a 294,912 bit Synchronous Static Random Access Memory designed to support high speed i486 secondary caches. It is organized as 32,768 words of 9 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced component count implementations of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous. The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and furthre reducing the component count.

Bursts can be initiated with either the address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) inputs. Subsequent burst address are generated internally in the i486 burst sequence and are controlled by the burst address advance ($\overline{ADV}$) input.

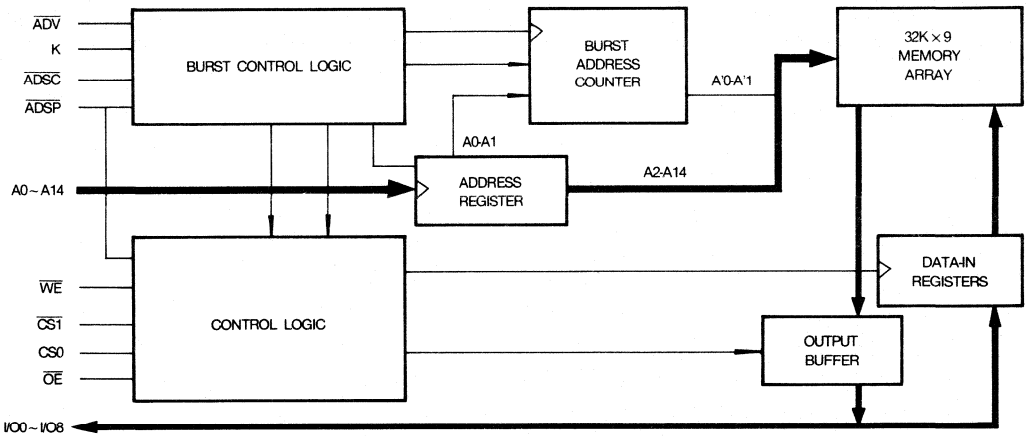
The KM79C86 is implemented in Samsung's high performance CMOS technology and is available in a 44 pin PLCC package. Multiple power and ground pins are utilized to minimize ground bounce.

PIN CONFIGURATION (Top View)



Pin Name	Pin Function
A0 ~ A14	Address Inputs
K	Clock
$\overline{WE}$	Write Enable
CS0, $\overline{CS1}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{ADV}$	Burst Address Advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status
I/O0 ~ I/O8	Data Inputs/Outputs
V_{CC}	+5V Power Supply
V_{SS}	Ground

LOGIC BLOCK DIAGRAM



FUNCTION DESCRIPTION

The KM79C86 is a synchronous SRAM designed to support the burst address accessing sequence of the i486 microprocessor. All inputs (with the exception of $\overline{OE}$) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$ and $\overline{ADSP}$. The sccesses are enabled with the chip select signals and output enable.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{WE}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the next and subsequent clock edges. The address is incremented internally for the next access of the burst when $\overline{ADV}$ is sampled low.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$. $\overline{WE}$ is ignored on the clock edge that samples $\overline{ADSP}$ low. but is sampled on the next and subsequent clock edges. The output buffers are disabled when $\overline{WE}$ is sampled low (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WE}$ is sampled low. The address is incremented internally before the write is performed if both $\overline{WE}$ and $\overline{ADV}$ are sampled low.

Read or write cycles (depending on $\overline{WE}$) may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSp}$ are as follows;

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{WE}$ is sampled on the clock edge that samples $\overline{ADSC}$ low (and $\overline{ADSP}$ high).

Address are generated for the burst accesses as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

i486 BURST SEQUENCE

	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	0	0	1	1	1	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

TRUTH TABLES

SYNCHRONOUS TRUST TABLE (See Notes 1 and 2)

$\overline{CS}$	$\overline{ADSO}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WE}$	K	Address Accessed	Operation
H	L	X	X	X	↑	N/A	Not Selected
H	X	L	X	X	↑	N/A	Not Selected
L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE 1: X means "Don't Care"
NOTE 2: The rising edge of clock is symbolized by ↑
NOTE 3: $\overline{CS}$ represents CS0 and $\overline{CS1}$. L implies CS0 = H and $\overline{CS1}$ = L; H implies CS0 = L or $\overline{CS1}$ = H.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{OE}$	Operation
L	Read I/O0 ~ I/O8
H	Outputs High-Z
X	Not Selected, Outputs High-Z

NOTE 1: X means "Don't Care"
NOTE 2: For write cycles that follow read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Voltage on Any Other Pin Relative to V_{SS}	V_{IN}	−0.5 to 7.0	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	−65 to +150	°C
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature Range Under Bias	T_{BIAS}	−10 to +85	°C

*NOTE: Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V

CAPACITANCE* ($T_A = 25°C$, f = 1Mhz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	5	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	8	pF

*NOTE: Sampled not 100% tested.

2

TEST CONDITIONS ($T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = 5V \pm 10\%$, $T_A = 0°C$ to $+70°C$)

Parameter	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{IL}	V_{CC} = Max; $V_{IN} = V_{SS}$ to V_{CC}		-2	$+2$	μA
Output Leakage Current	I_{OL}	Output Disabled		-2	$+2$	μA
Operating Current	I_{CC}	V_{CC} = Max, I_{OUT} = 0mA, Cycle Time $\geq t_{CYC}$ min	14ns	—	190	mA
			19ns	—	180	mA
			24ns	—	160	mA
Standby Current	I_{SB}	CS0 = V_{IL} or $\overline{CS1}$ = V_{IH}, Min Cycle		—	50	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA V_{CC} = Min		—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA V_{CC} = Min		2.4	—	V
Input Low Voltage	V_{IL}			2.2	$V_{CC} + 0.5$	V
Input High Voltage	V_{IH}			-0.5*	0.8	V

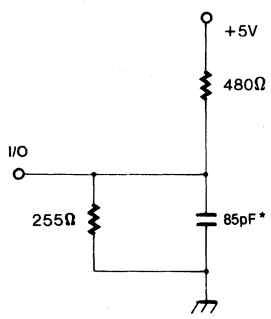
*V_{IL} (min) = -3.0 (Pulse Width $\leq$ 20ns)

AC TIMING CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	KM79C86-14		KM79C86-19		KM79C86-24		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	t_{CYC}	20		25		30		ns
Clock Access Time	t_{CD}		14		19		24	ns
Output Enable to Data Valid	t_{OE}		6		7		8	ns
Clock High to Output Low-Z	t_{LZC}	7		7		7		ns
Output Hold from Clock High	t_{OH}	4		4		4		ns
Output Enable Low to Output Low-Z	t_{LZOE}	0		0		0		ns
Output Enable High to Output High-Z	t_{HZOE}		7		8		9	ns
Clock High to Output High-Z	t_{HZC}		8		8		8	ns
Clock High Pulse Width	t_{CH}	8		9		11		ns
Clock Low Pulse Width	t_{CL}	8		9		11		ns
Address Setup to Clock High	t_{AS}	3		3		3		ns
Address Status Setup to Clock High	t_{SS}	3		3		3		ns
Data Setup to Clock High	t_{DS}	3		3		3		ns
Write Setup to Clock High	t_{WS}	3		3		3		ns
Address Advance Setup to Clock High	t_{ADVS}	3		3		3		ns
Chip Select Setup to Clock High	t_{CSS}	3		3		3		ns
Address Hold from Clock High	t_{AH}	2		2		2		ns
Address Status Hold from Clock High	t_{SH}	2		2		2		ns
Data Hold from Clock High	t_{DH}	2		2		2		ns
Write Hold from Clock High	t_{WH}	2		2		2		ns
Address Advance Hold from Clock High	t_{ADVH}	2		2		2		ns
Chip Select Hold from Clock High	t_{CSH}	2		2		2		ns

NOTE: All address inputs must meet the specified setup and hold times for all rising clock (K) edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

Output Load (A)



Output Load (B)
(for t_{HZOE})

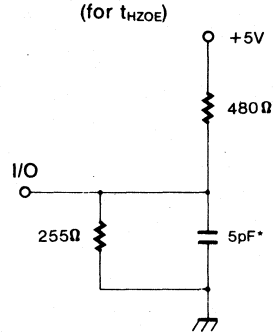
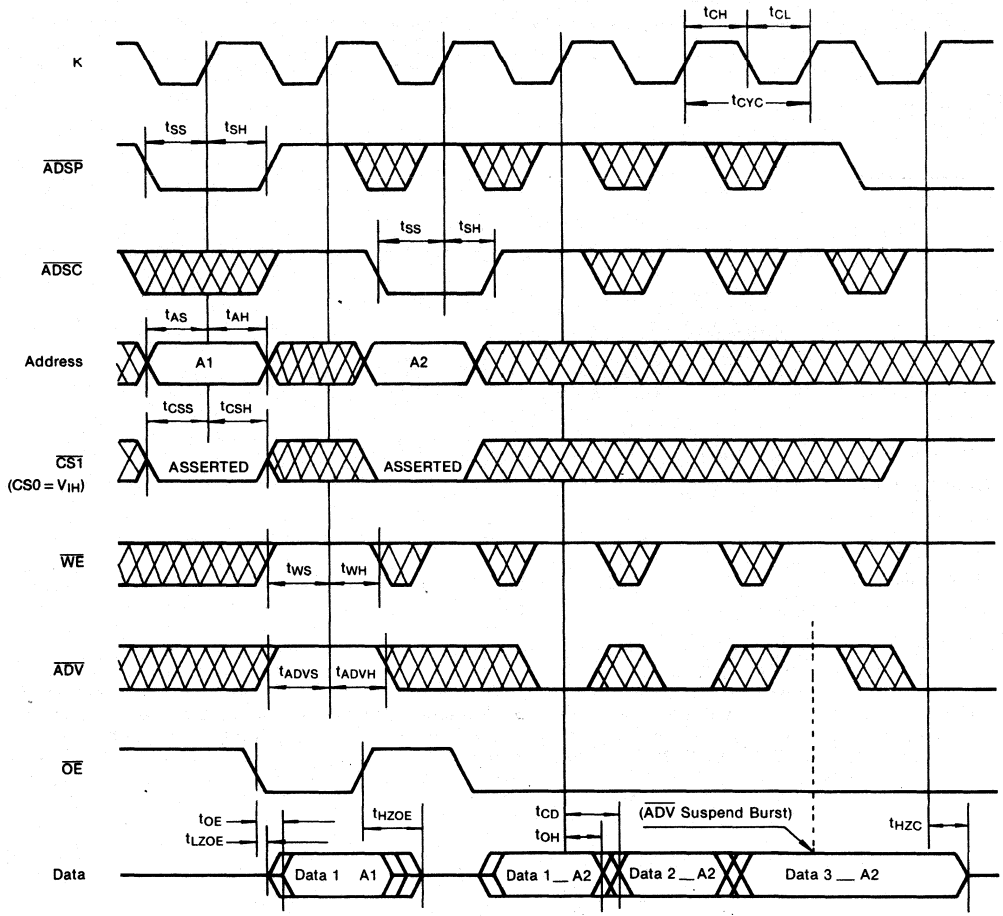


Fig. 1

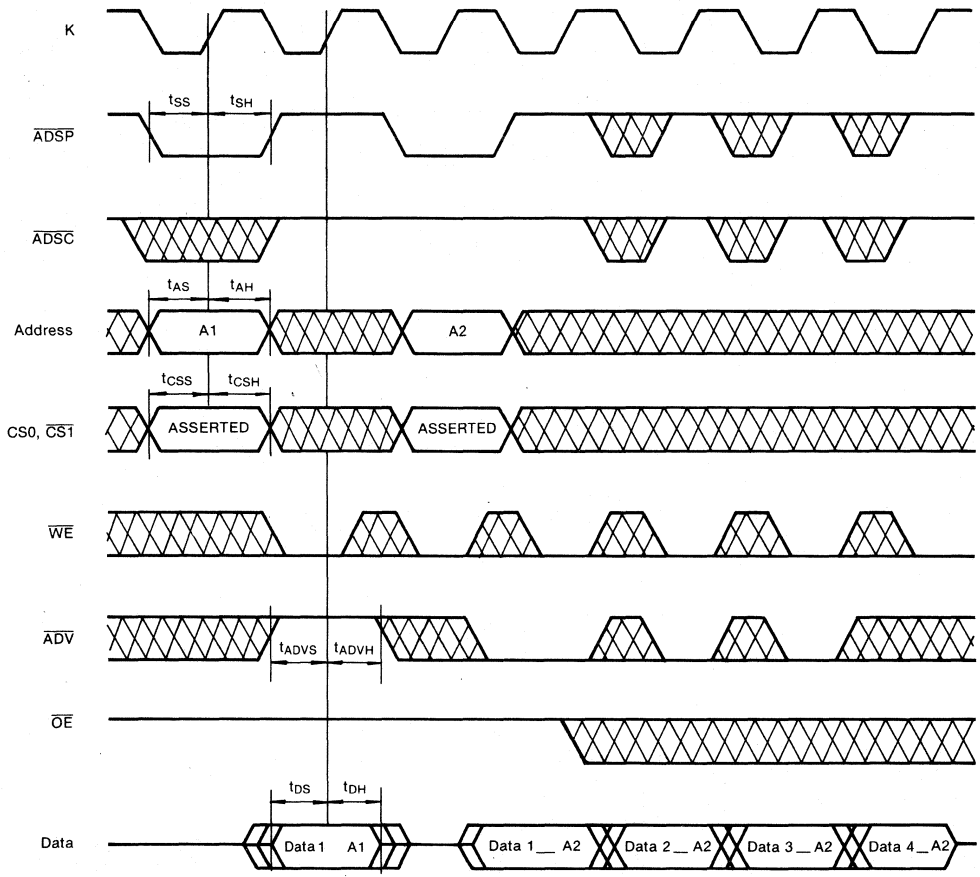
* Including Scope and Jig Capacitance

TIMING WAVEFORM OF READ CYCLES

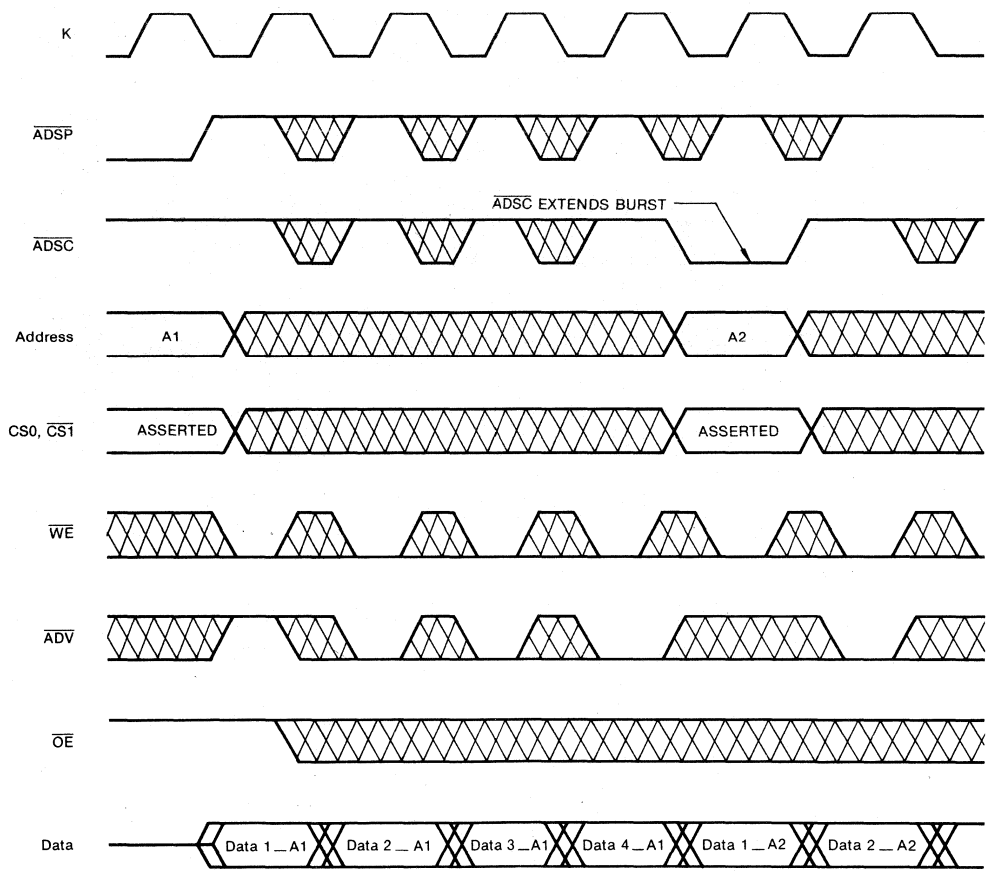


Note: In a burst mode, burst sequence is suspended with $\overline{ADV}$ sampled High on a positive going edge of clock (K).

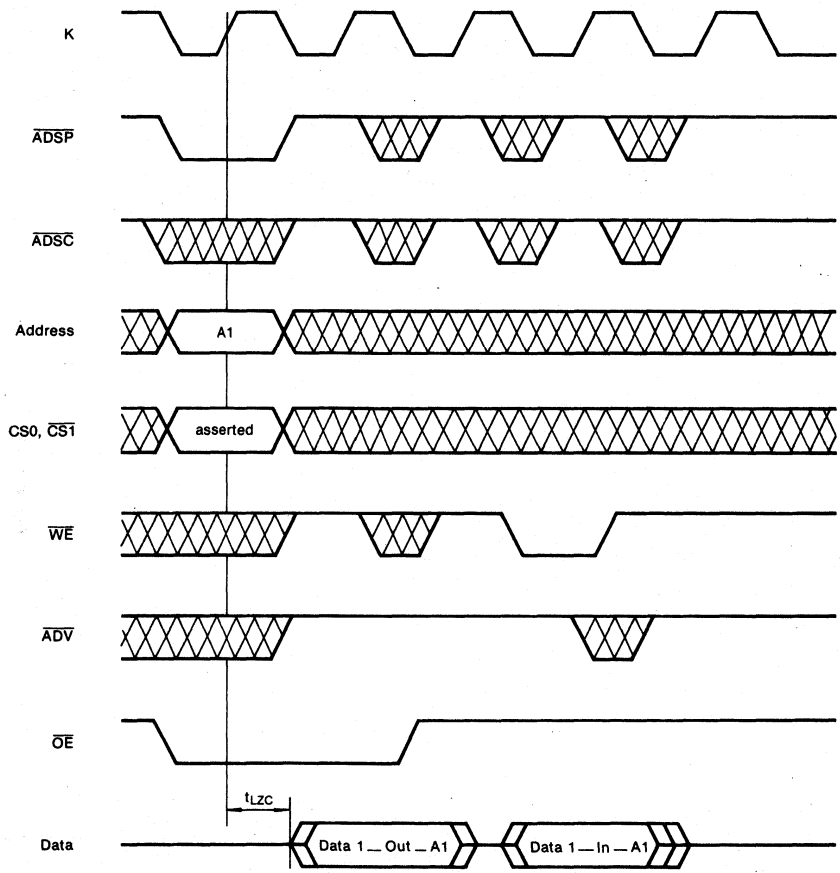
TIMING WAVEFORM OF SINGLE AND BURST WRITE CYCLES

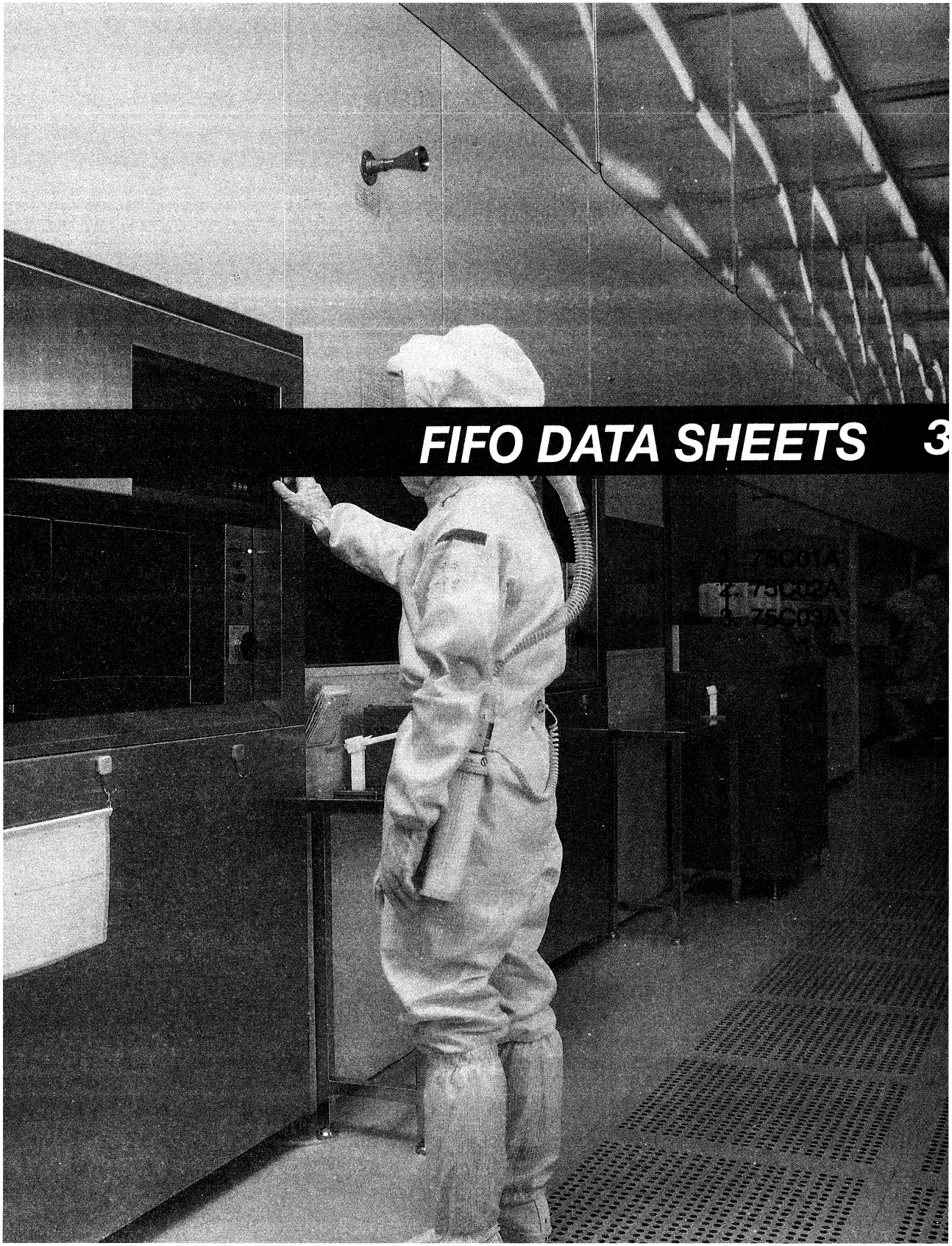


TIMING WAVEFORM OF EXTENDED WRITE CYCLE



TIMING WAVEFORM OF READ-MODIFY-WRITE CYCLE





FIFO DATA SHEETS 3

First-in First-out (FIFO) 512x9 CMOS Memory

FEATURES

- First-in, First-out dual port memory
  - 512 x 9 organization
- Very high speed independent of depth/width
  - 25ns cycle times
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or width
- Low power consumption
  - Active: 150mA (max)
  - Power Down: 15mA (max)
- KM75C01A pinout and functionality compatible with IDT IDT7201A and AMD Am 7201A
- Half-full flag capability in standalone mode
- Empty and full warning flags
- Auto retransmit capability in standalone mode
- High performance 1.2 micron CMOS technology
- Available in 300 mil and 600 mil Plastic DIP and 32 pin PLCC

DESCRIPTION

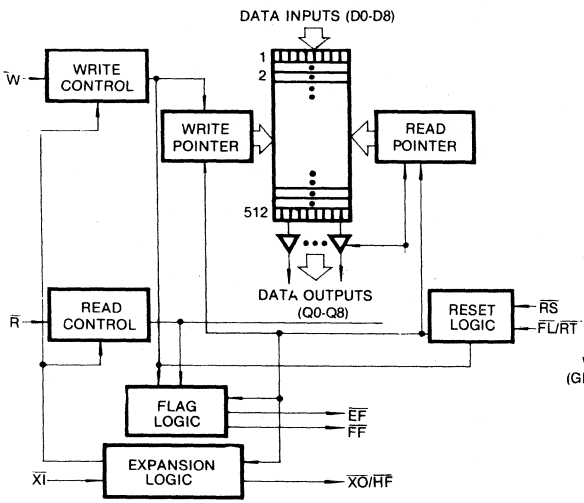
The KM75C01A is dual port memory that implements a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. Full and empty flags are provided to prevent data overflow. Expansion logic allows unlimited expansion capability in both word size and depth without any loss in speed.

No address information is required for KM75C01A. Ring counters automatically generate the addresses required for every read and write operations. Data is toggled in and out of the device through the use of WRITE($\overline{W}$) and READ($\overline{R}$) pins. The device has a read/write cycle time of 25nsec (40MHz).

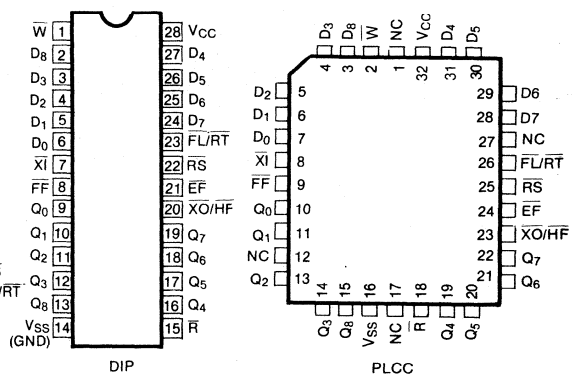
The device consists of a 9-bit wide array which is very useful in applications such as data communications where it is necessary to use parity bit. The RETRANSMIT ($\overline{RT}$) feature allows to re-read the previously read data. A half-full flag is available in the single device and width expansion modes.

The KM75C01A is fabricated using proprietary high speed CMOS 1.2 micron technology. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS (Top Views)



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage On Any Pin Relative to V_{SS}	V_{IN}	−0.5 to 7.0	V
Operating Temperature	T_A	0 to +70	°C
Temperature Under Bias	T_{bias}	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to 150	°C
Power Dissipation	P_D	1.0	W
DC Output Current	I_{OUT}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0			V
Input Low Voltage	V_{IL}			0.8	V

DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$)

Parameter	Symbol	T_A = 15/20ns			T_A = 25ns			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Active Current	I_{CC}			150			120	mA
V_{CC} Standby Current-TTL[1] ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$)	I_{SB1}			15			15	mA
V_{CC} Standby Current-CMOS[1] (all inputs = V_{CC}-0.2V)	I_{SB2}			5			5	mA
Input Leakage Current[2]	I_{LI}	−1		1	−1		1	μA
Output Leakage Current[3]	I_{LO}	−10		10	−10		10	μA
Output High Voltage Level (I_{OH} = −2mA)	V_{OH}	2.4			2.4			V
Output Low Voltage Level (I_{OL} = 8mA)	V_{OL}			0.4			0.4	V

DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$)

Parameter	Symbol	T_A = 35ns			T_A = 50ns			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Active Current	I_{CC}			100			60	mA
V_{CC} Standby Current-TTL[1] ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$)	I_{SB1}			15			15	mA
V_{CC} Standby Current-CMOS[1] (all inputs = V_{CC}-0.2V)	I_{SB2}			5			5	mA
Input Leakage Current[2]	I_{LI}	−1		1	−1		1	μA
Output Leakage Current[3]	I_{LO}	−10		10	−10		10	μA
Output High Voltage Level (I_{OH} = −2mA)	V_{OH}	2.4			2.4			V
Output Low Voltage Level (I_{OL} = 8mA)	V_{OL}			0.4			0.4	V

Notes: 1. I_{CC} and I_{SB} measurements are made with outputs open.
2. Measurements with $V_{SS} \leq V_{IN} \leq V_{CC}$.
3. $\overline{R} \geq V_{IH}$, $V_{SS} \leq V_{OUT} \leq V_{CC}$.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	KM75C01A-15		KM75C01A-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		30		ns
Access Time	t_A		15		20	ns
Read Recovery Time	t_{RR}	10		10		ns
Read Pulse Width[2]	t_{RPW}	15		20		ns
Data Valid from Read Pulse High	t_{DV}	5		5		ns
Read Pulse High to Data Bus at High-Z[3]	t_{RHZ}		15		15	ns
Write Cycle Time	t_{WC}	25		30		ns
Write Pulse Width[2]	t_{WPW}	15		20		ns
Write Recovery Time	t_{WR}	10		10		ns
Data Setup Time	t_{DS}	10		12		ns
Data Hold Time	t_{DH}	0		0		ns
Reset Cycle Time	t_{RSC}	25		30		ns
Reset Pulse Width[2]	t_{RS}	15		20		ns
Reset Recovery Time	t_{RSR}	10		10		ns
Retransmit Cycle Time	t_{RTC}	25		30		ns
Retransmit Pulse Width[2]	t_{RT}	15		20		ns
Retransmit Recovery Time	t_{RTR}	10		10		ns
Reset to Empty Flag Low	t_{EFL}		25		30	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		25		30	ns
Read Low to Empty Flag High	t_{REF}		20		20	ns
Read High to Full Flag High	t_{RFF}		20		20	ns
Write High to Empty Flag High	t_{WEF}		20		20	ns
Write Low to Full Flag Low	t_{WFF}		20		20	ns
Write Low to Half-Full Flag Low	t_{WHF}		25		30	ns
Read High to Half-Full Flag High	t_{RHF}		25		30	ns
Expansion Out Low Delay from Clock	t_{XOL}		20		20	ns
Expansion Out High Delay from Clock	t_{XOH}[4]		20		20	ns
$\overline{XI}$ Pulse Width	t_{PXI}	15		20		ns
$\overline{XI}$ Recovery Time	t_{XIR}	10		10		ns
$\overline{XI}$ Set-Up to Write or Clock	t_{XIS}	10		12		ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	KM75C01A-25		KM75C01A-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		ns
Access Time	t_A		25		35	ns
Read Recovery Time	t_{RR}	10		10		ns
Read Pulse Width[2]	t_{RPW}	25		35		ns
Data Valid from Read Pulse High	t_{DV}	5		5		ns
Read Pulse High to Data Bus at High-Z[1]	t_{RHZ}		20		20	ns
Write Cycle Time	t_{WC}	35		45		ns
Write Pulse Width[2]	t_{WPW}	25		35		ns
Write Recovery Time	t_{WR}	10		10		ns
Data Setup Time	t_{DS}	15		18		ns
Data Hold Time	t_{DH}	0		0		ns
Reset Cycle Time	t_{RSC}	35		45		ns
Reset Pulse Width[2]	t_{RS}	25		35		ns
Reset Recovery Time	t_{RSR}	10		10		ns
Retransmit Cycle Time	t_{RTC}	35		45		ns
Retransmit Pulse Width[2]	t_{RT}	25		35		ns
Retransmit Recovery Time	t_{RTR}	10		10		ns
Reset to Empty Flag Low	t_{EFL}		35		45	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		35		45	ns
Read Low to Empty Flag High	t_{REF}		25		30	ns
Read High to Full Flag High	t_{RFF}		25		30	ns
Write High to Empty Flag High	t_{WEF}		25		30	ns
Write Low to Full Flag Low	t_{WFF}		25		30	ns
Write Low to Half-Full Flag Low	t_{WHF}		35		45	ns
Read High to Half-Full Flag High	t_{RHF}		35		45	ns
Expansion Out Low Delay from Clock	t_{XOL}		25		35	ns
Expansion Out High Delay from Clock	t_{XOH}[4]		25		35	ns
$\overline{XI}$ Pulse Width	t_{PXI}	25		35		ns
$\overline{XI}$ Recovery Time	t_{XIR}	10		10		ns
$\overline{XI}$ Set-Up to Write or Clock	t_{XIS}	15		15		ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	KM75C01A-50		KM75C01A-80		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	65		100		ns
Access Time	t_A		50		80	ns
Read Recovery Time	t_{RR}	15		20		ns
Read Pulse Width[2]	t_{RPW}	50		80		ns
Data Valid from Read Pulse High	t_{DV}	5		5		ns
Read Pulse High to Data Bus at High-Z[3]	t_{RHZ}		30		30	ns
Write Cycle Time	t_{WC}	65		100		ns
Write Pulse Width[2]	t_{WPW}	50		80		ns
Write Recovery Time	t_{WR}	15		20		ns
Data Setup Time	t_{DS}	30		40		ns
Data Hold Time	t_{DH}	5		10		ns
Reset Cycle Time	t_{RSC}	65		100		ns
Reset Pulse Width[2]	t_{RS}	50		80		ns
Reset Recovery Time	t_{RSR}	15		20		ns
Retransmit Cycle Time	t_{RTC}	65		100		ns
Retransmit Pulse Width[2]	t_{RT}	50		80		ns
Retransmit Recovery Time	t_{RTR}	15		20		ns
Reset to Empty Flag Low	t_{EFL}		65		100	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		65		100	ns
Read Low to Empty Flag High	t_{REF}		45		60	ns
Read High to Full Flag High	t_{RFF}		45		60	ns
Write High to Empty Flag High	t_{WEF}		45		60	ns
Write Low to Full Flag Low	t_{WFF}		45		60	ns
Write Low to Half-Full Flag Low	t_{WHF}		65		100	ns
Read High to Half-Full Flag High	t_{RHF}		65		100	ns
Expansion Out Low Delay from Clock	t_{XOL}		50		80	ns
Expansion Out High Delay from Clock	t_{XOH}[4]		50		65	ns
XI Pulse Width	t_{EXI}	50		80		ns
XI Recovery Time	t_{XIR}	15		20		ns
XI Set-Up to Write or Clock	t_{XIS}	15		15		ns

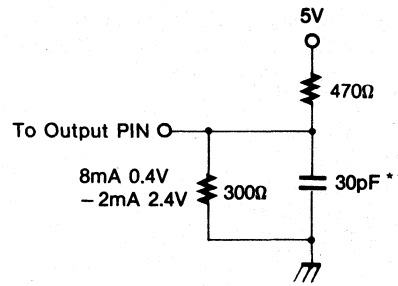
Notes: 1. Timings referenced as in AC Test Conditions
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested
4. t_{XOH} is guaranteed to be greater than or equal to t_{XOL} under all conditions.

SAMSUNG ELECTRONICS

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

Figure 1. Output Load



* INCLUDES JIG AND SCOPE CAPACITANCES

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

Note: This parameter is sampled and not 100% tested.

Note: Generation $\overline{R}/\overline{W}$ Signals-When using these high-speed FIFO devices, it is necessary to have clean inputs on the $\overline{R}$ and $\overline{W}$ signals. It is important not to have glitches, spikes or ringing on the $\overline{R}$, $\overline{W}$ (that violate the V_{IL}, V_{IH} requirements); although the minimum pulse width low for the $\overline{R}$ and $\overline{W}$ are specified in tens of nanosecond, a glitch of 3ns can affect the read or write pointer and cause it to increment.

Master Reset ($\overline{RS}$)

Reset is accomplished whenever the MASTER RESET ($\overline{RS}$) input is taken to a low state. During this operation, both the internal read and the internal write pointers are set to the first FIFO location. A Master Reset pulse is required to initialize the FIFO after power-up before any write operation is performed. Both $\overline{R}$ and $\overline{W}$ inputs must be inactive for t_{RPW} or t_{WPW} before the rising edge of $\overline{RS}$, and should not change for t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be set to inactive (high) level after master reset ($\overline{RS}$).

Read Enable ($\overline{R}$)

READ cycles are initiated on the falling edge of the READ ENABLE ($\overline{R}$) input provided that EMPTY-FLAG ($\overline{EF}$) is not low. Read Cycles may be initiated asynchronously to any write operation in progress. After READ ENABLE ($\overline{R}$) goes high, the data outputs will return to a high impedance condition until the next READ operation. If the FIFO is empty, the EMPTY-FLAG ($\overline{EF}$) will go low and prevent any further read cycles. The data outputs will enter the high-impedance state after completion of the last read cycle.

Write Enable ($\overline{W}$)

WRITE cycles may be initiated by a low signal at the $\overline{W}$ input provided the FULL-FLAG ($\overline{FF}$) is not set. Data is stored in the memory array sequentially independent of any read operation that may be in progress.

When more than half of the memory bytes have been filled, the HALF-FULL ($\overline{HF}$) Flag output will be set low and will remain low till the difference between the write pointer and read pointer is less than or equal to one half of the total memory bytes of the device. The HALF-FULL flag is then reset by the rising edge of the read operation.

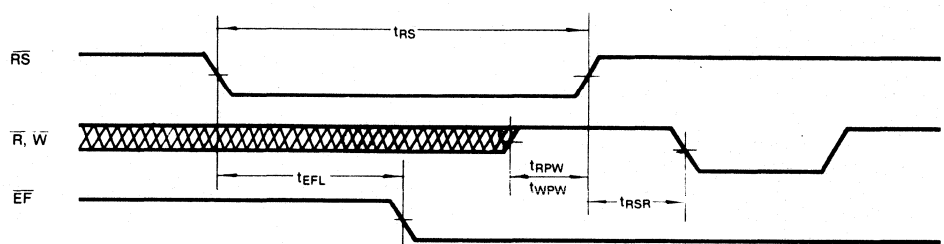
When the memory array is completely full, i.e., when the write pointer is one location from the read pointer, the FULL-FLAG ($\overline{FF}$) will go low preventing any further write operations. The FULL-FLAG will go high again t_{RFF} after completion of a valid read operation.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)

This input may be used in two different ways depending upon the configuration of EXPANSION-IN ($\overline{XI}$):

1. Single Device or Retransmit Mode: In this mode the $\overline{XI}$ pin must be grounded. Using this mode the device can be used to retransmit data when $\overline{RT}$ is pulsed low. A retransmit operation will set the internal read pointer

Figure 2. Reset



Notes

1. $t_{RSC} = t_{RS} + t_{RSR}$
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

to the first memory location in the array. The write pointer is unaffected. Both write enable and read enable must be inactive during the retransmit operation. This feature is particularly useful for FIFO applications in communications buffers where noise levels may be high and transmission errors are frequently detected. The retransmit feature may not be used along with depth expansion.

2. Depth Expansion Mode: In this mode the ($\overline{FL}/\overline{RT}$) pin is grounded it that device is the first of the "daisy chain." The $\overline{FL}$ pin is kept high if it is further down the chain. For details of Depth Expansion see Operating Modes.

Expansion-In ($\overline{XI}$)

This is a dual purpose input pin. As explained above, $\overline{XI}$ is grounded to indicate single device mode operation. EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device of the "daisy chain" in the Depth Expansion mode.

Full-Flag ($\overline{FF}$)

The FULL-FLAG output goes low inhibiting further write operations when the write pointer is one memory location from the read pointer i.e., the memory array is full. The total length of the memory array is 512 bytes write operations for the KM75C01A.

Expansion Out/Half-Full Flag ($\overline{XO}/\overline{HF}$)

This output may be used in two different ways:

Single Device Mode: In this mode this output acts as a HALF-FULL Flag. After half the memory locations are full, and at the falling edge of the next write operation, the $\overline{HF}$ output is set to low. It is reset to high if the difference between the write pointer and the read pointer is half the memory depth or less at the rising edge of the read operation.

Depth Expansion Mode: In this mode EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device of the "daisy chain." In this way a signal can be passed onto the next device when the current device reaches the last memory location.

FIFO's can also be expanded simultaneously in depth and width to provide word widths greater than 9 in increments of 9. Consequently, any depth or width FIFO can be created. When expanding in depth, a composite $\overline{FF}$ must be created by OR-ing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by OR-ing the $\overline{EF}$'s together. $\overline{HF}$ and $\overline{RT}$ functions are available in Depth Expansion Mode.

Single Device/Width Expansion Mode: Single Device and Width Expansion Modes are entered by grounding $\overline{XI}$ during a MR cycle. During these modes the $\overline{HF}$ and $\overline{RT}$ features are available. FIFO's can be expanded in width to provide word widths greater than 9 in increments of 9. During Width Expansion Mode all control line inputs are common to all devices and flag outputs from any device can be monitored.

Figure 3. Asynchronous Write and Read Operation

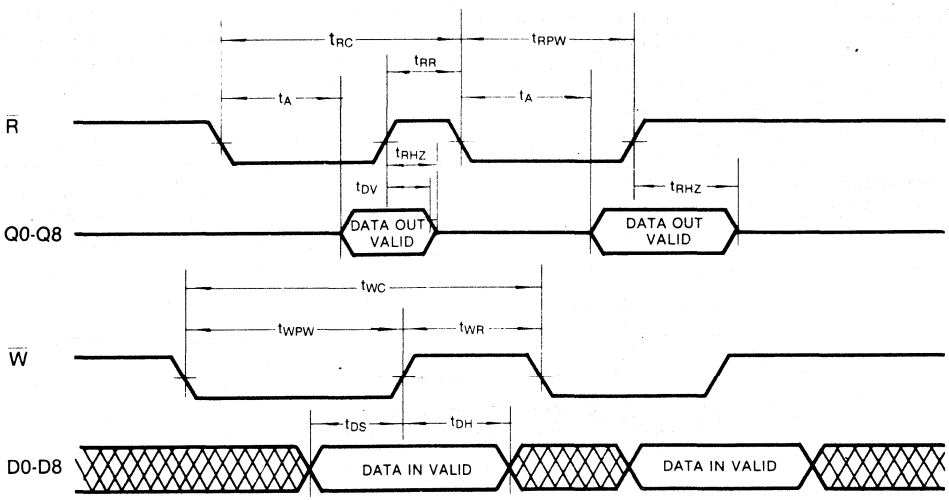


Figure 4. Full Flag From Last Write to First Read

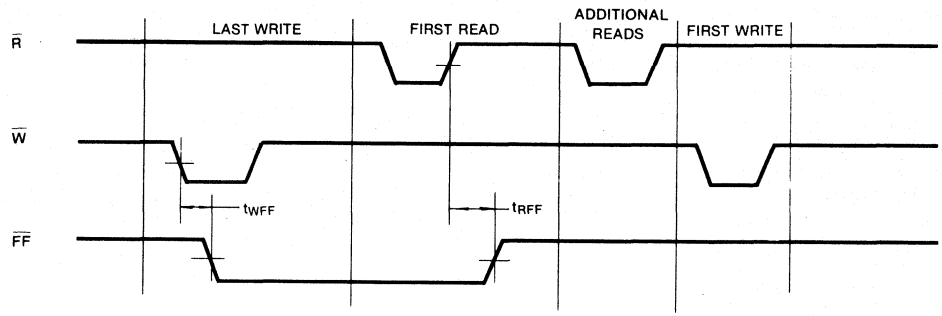


Figure 5. Empty Flag From Last Read to First Write

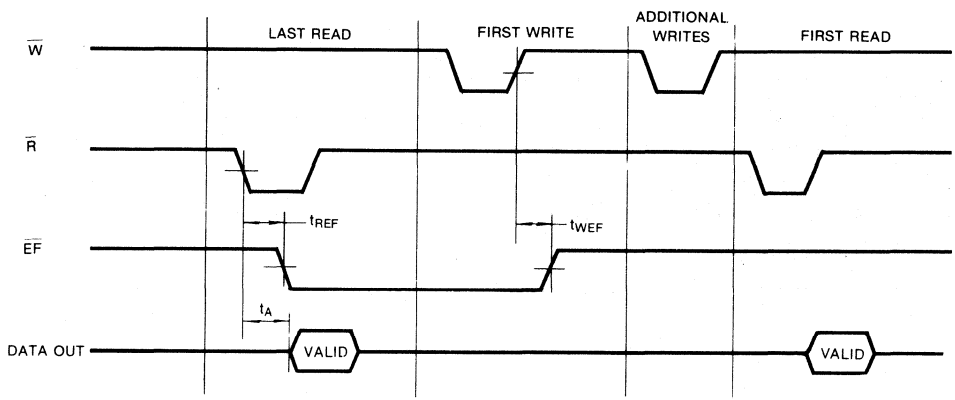
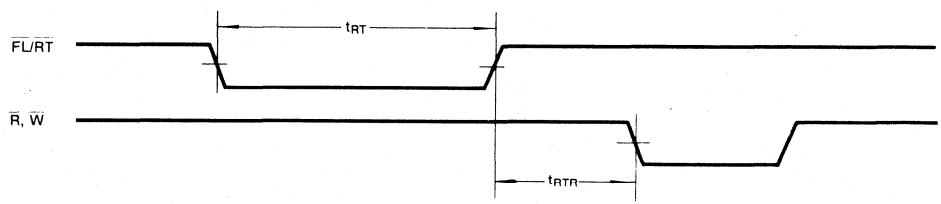


Figure 6. Retransmit



Notes:

1. $t_{RTC} = t_{RT} + t_{RTR}$
2. $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

Figure 7. Expansion-In Timing Diagram

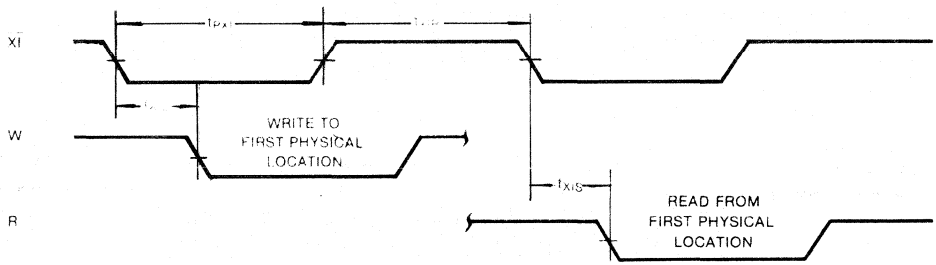


Figure 8. Expansion-Out Timing Diagram

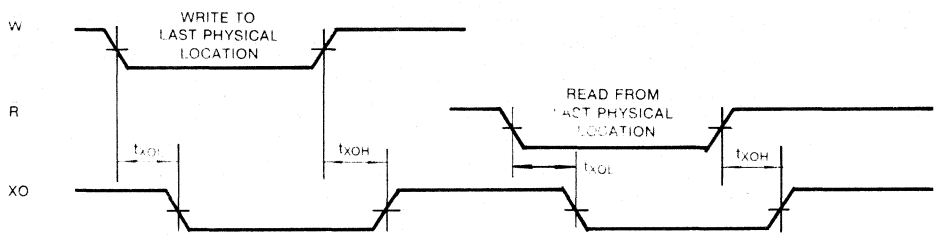
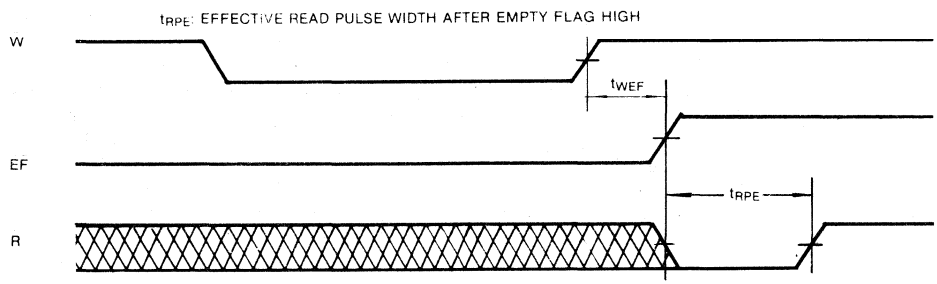


Figure 9. Empty Flag Timing



Note: 1. ($t_{RPE} = t_{RPW}$)

Figure 10. Full Flag Timing

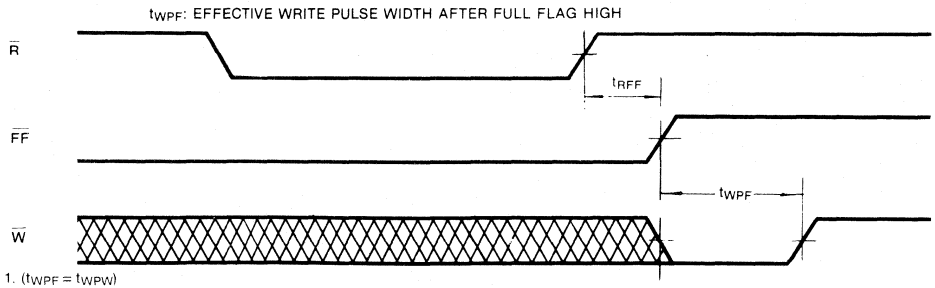
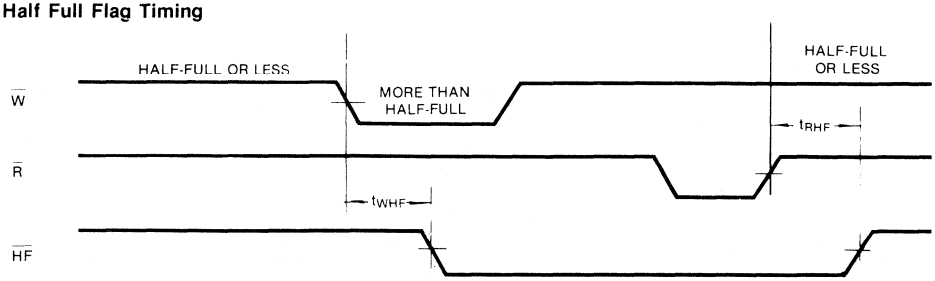


Figure 11. Half Full Flag Timing



OPERATING MODES

Single Device Mode

A single KM75C01A may be used when the application requirements are for 512 words or less, the device is placed in a Single Device Configuration when the EXPANSION IN (XI) control input is grounded (See Figure 12). In this mode the HALF-FULL FLAG (HF) and RETRANSMIT (RT) features are available.

Figure 12. Block Diagram of Single 512 x 9 FIFO

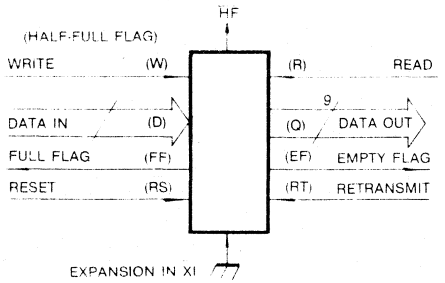
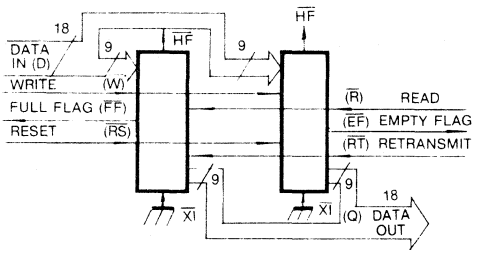


Figure 13. Block Diagram of 512 x 18 FIFO Memory Used in Width Expansion Mode



Notes: Flag detection is accomplished by monitoring the FF, EF, and HF signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Width Expansion Mode

Word width may be increased simply by connecting he corresponding input control signals of multiple devices. Status flags (EF, FF and HF) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two KM75C01A. Any word width can be attained by adding additional KM75C01A.

Depth Expansion (Daisy Chain) Mode

The KM75C01A can easily be adapted to applications when the requirements are for greater than 512 words. Figure 14 demonstrates Depth Expansion using three KM75C01A. Any depth can be attained by adding additional KM75C01A. The KM75C01A operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the FIRST LOAD (FL) control input. The RETRANSMIT feature is not available in this mode.
2. All other devices must have FL in the high state.
3. The EXPANSION OUT (XO) pin of each device must be tied to the EXPANSION IN (XI) pin of the next device. The half-full flag (HF) function is not available in this mode.
4. External logic is needed to generate a composite FULL FLAG (FF) and EMPTY FLAG (EF). This requires the OR-ing of all EFs and OR-ing of all FFs (i.e., all must be set to generate the correct composite FF or EF).

Compound Expansion Mode

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (See Figure 15).

Bidirectional Mode

Applications which required data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing KM75C01A as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system; (i.e., FF is monitored on the device where W is used; EF is monitored on the device where R is used). Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through Modes

This section describes two special conditions—when the FIFO is full or empty. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of W, called the first write edge, and it remains on the bus until the R line is raised from low-to-high, after which the bus would go into a tri-state mode after t_{RHZ} ns. The EF line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that R was low, more words can be written to the FIFO (the subsequent writes after the first write edge would deassert the emptly flag); however, the same word (written the first write edge), presented to the output bus as the read pointer, would not be incremented when R is low. On toggling R, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data (from a full FIFO. The R line causes the FF to be de-asserted but the W line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of W, the new word is loaded in the FIFO. The W line must be toggled when FF is not asserted to write new data in the FIFO and to increment the write pointer.

TRUTH TABLES

Table 1. Reset and Retransmit-Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment (1)	Increment (1)	X	X	X

Note: 1. Pointer will increment if flag is high

Table 2. Reset and First Load Truth Table-Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{HF}$
Reset	0	0	(1)	Location Zero	Location Zero	0	1
Retransmit	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

Note: 1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.
$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output.

Figure 14. Block Diagram of 1536 x 9 FIFO Memory (Depth Expansion)

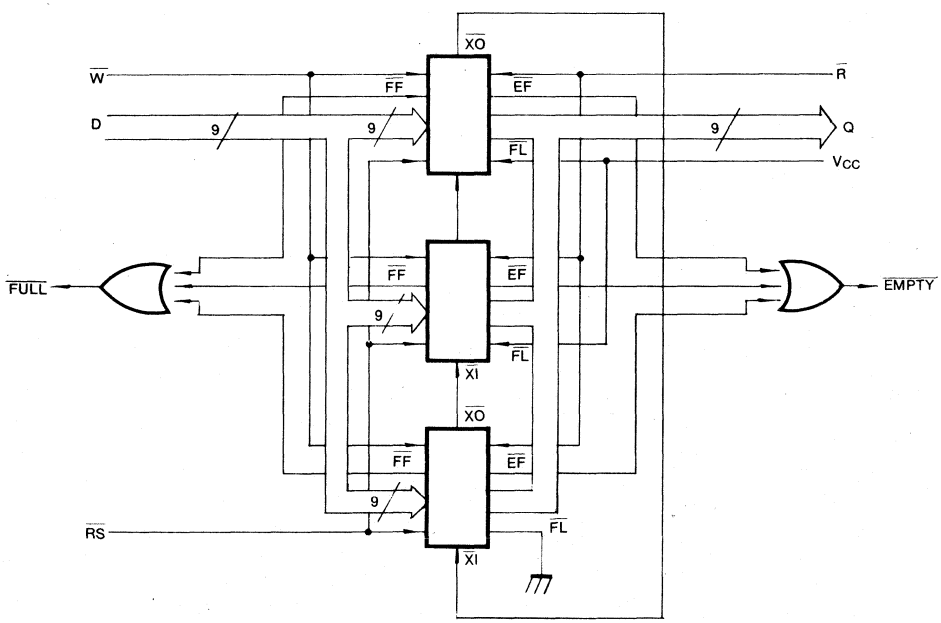


Figure 15. Compound FIFO Expansion

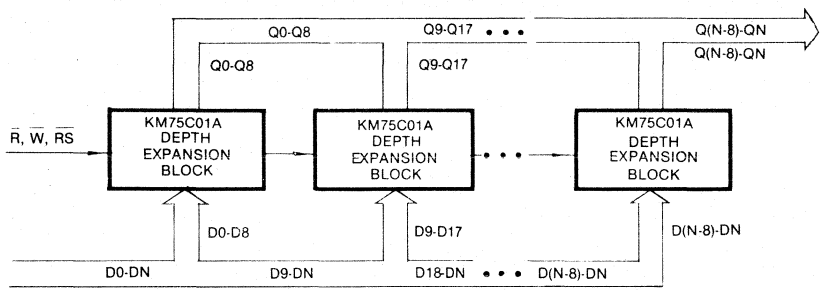
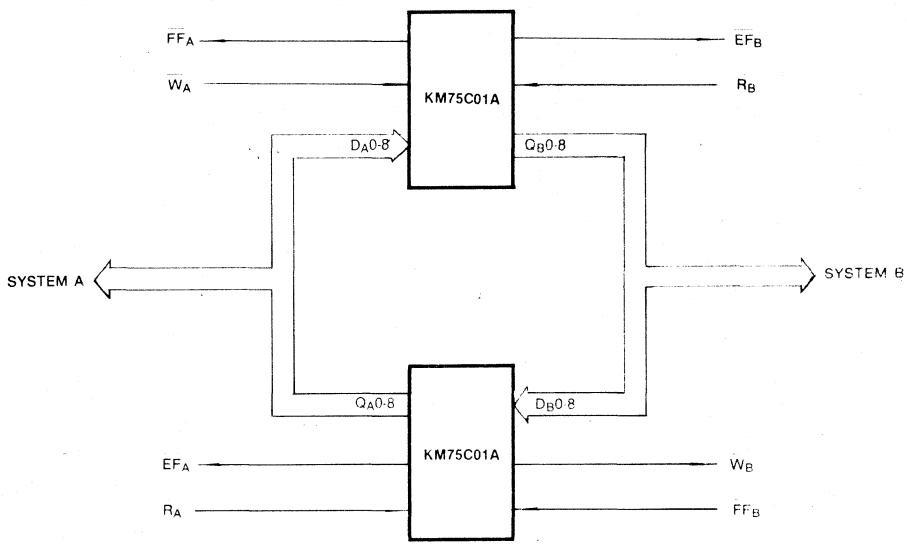
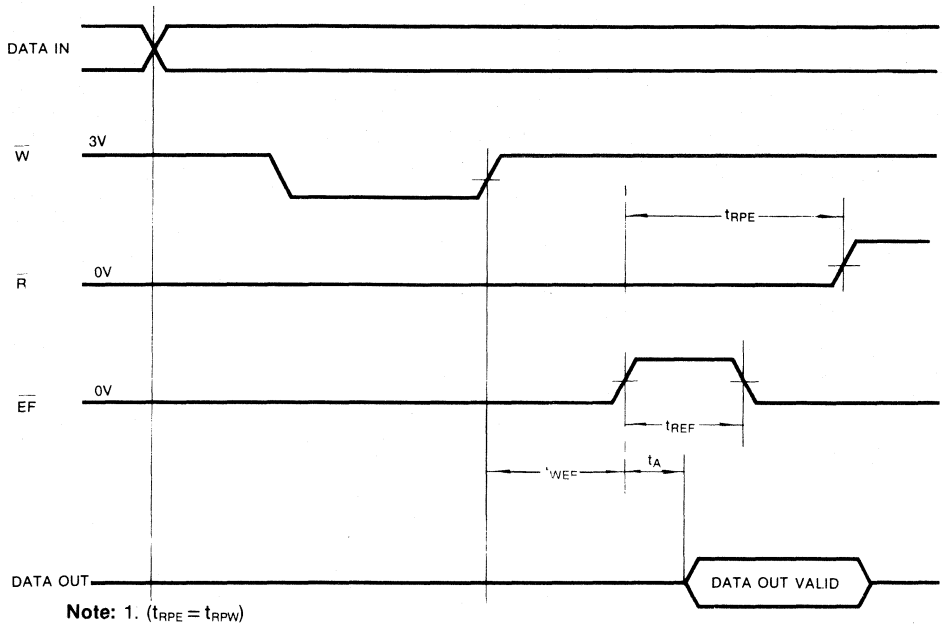


Figure 16. Bidirectional FIFO Mode



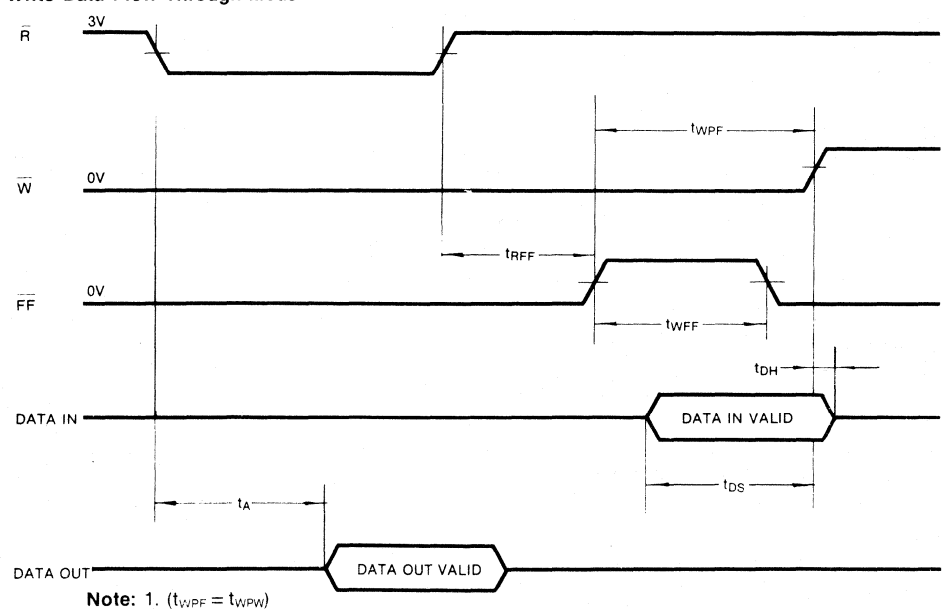
Notes:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 14.
2. For detection see WIDTH EXPANSION Section and Figure 13.

Figure 17. Read Data Flow Through Mode



Note: 1. ($t_{RPE} = t_{RPW}$)

Figure 18. Write Data Flow Through Mode



Note: 1. ($t_{WPF} = t_{WPW}$)

First-in First-out (FIFO) 1024 x 9 CMOS Memory

FEATURES

- First-in, First-out dual port memory
  - 1024 x 9 organization
- Very high speed independent of depth/width
  - 20ns cycle times
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or width
- Low power consumption
  - Active: 150mA (max)
  - Power Down: 15mA (max)
- KM75C02A allows for deep word structure (1024) without expansion-pin and functionally compatible with AMD Am7202 and IDT7202A
- Half-full flag capability in standalone mode
- Empty and full warning flags
- Auto retransmit capability in standalone mode
- High performance 1.2 micron CMOS technology
- Available in 300 mil and 600 mil Plastic DIP and 32 pin PLCC

DESCRIPTION

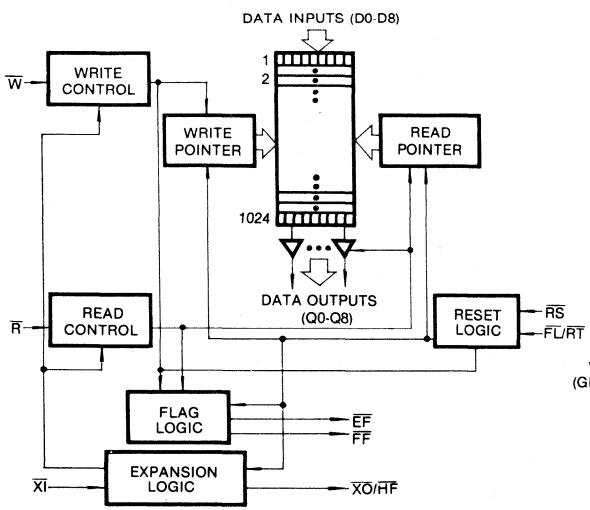
The KM75C02A is dual port memory that implements a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. Full and empty flags are provided to prevent data overflow. Expansion logic allows unlimited expansion capability in both word size and depth without any loss in speed.

No address information is required for KM75C02A. Ring counters automatically generate the addresses required for every read and write operations. Data is toggled in and out of the device through the use of WRITE($\overline{W}$) and READ($\overline{R}$) pins. The device has a read/write cycle time of 20nsec (50MHz).

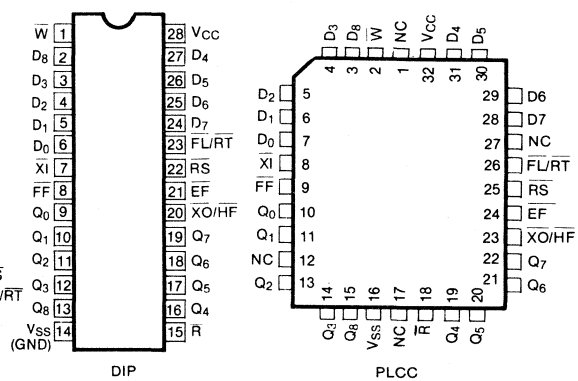
The device consists of a 9-bit wide array which is very useful in applications such as data communications where it is necessary to use parity bit. The RETRANSMIT ($\overline{RT}$) feature allows to re-read the previously read data. A half-full flag is available in the single device and width expansion modes.

The KM75C02A is fabricated using proprietary high speed CMOS 1.2 micron technology. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS (Top Views)



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage On Any Pin Relative to V_{SS}	V_{IN}	−0.5 to 7.0	V
Operating Temperature	T_A	0 to +70	°C
Temperature Under Bias	T_{bias}	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to 150	°C
Power Dissipation	P_D	1.0	W
DC Output Current	I_{OUT}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0			V
Input Low Voltage	V_{IL}			0.8	V

DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$)

Parameter	Symbol	T_A = 15/20ns			T_A = 25ns			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Active Current	I_{CC}			150			120	mA
V_{CC} Standby Current-TTL[1] ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$)	I_{SB1}			15			15	mA
V_{CC} Standby Current-CMOS[1] (all inputs = V_{CC}-0.2V)	I_{SB2}			5			5	mA
Input Leakage Current[2]	I_{LI}	−1		1	−1		1	μA
Output Leakage Current[3]	I_{LO}	−10		10	−10		10	μA
Output High Voltage Level (I_{OH} = −2mA)	V_{OH}	2.4			2.4			V
Output Low Voltage Level (I_{OL} = 8mA)	V_{OL}			0.4			0.4	V

DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$)

Parameter	Symbol	T_A = 35ns			T_A = 50ns			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Active Current	I_{CC}			100			60	mA
V_{CC} Standby Current-TTL[1] ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$)	I_{SB1}			15			15	mA
V_{CC} Standby Current-CMOS[1] (all inputs = V_{CC}-0.2V)	I_{SB2}			5			5	mA
Input Leakage Current[2]	I_{LI}	−1		1	−1		1	μA
Output Leakage Current[3]	I_{LO}	−10		10	−10		10	μA
Output High Voltage Level (I_{OH} = −2mA)	V_{OH}	2.4			2.4			V
Output Low Voltage Level (I_{OL} = 8mA)	V_{OL}			0.4			0.4	V

Notes: 1. I_{CC} and I_{SB} measurements are made with outputs open.
2. Measurements with $V_{SS} \leq V_{IN} \leq V_{CC}$.
3. $\overline{R} \geq V_{IH}$, $V_{SS} \leq V_{OUT} \leq V_{CC}$.

AC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, T_A=0°C to + 70°C)

Parameter	Symbol	KM75C02A-12		KM75C02A-15		KM75C02A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20		25		30		ns
Access Time	t_A		12		15		20	ns
Read Recovery Time	t_{RR}	8		10		10		ns
Read Pulse Width(2)	t_{RPW}	12		15		20		ns
Data Valid from Read Pulse High	t_{DV}	5		5		5		ns
Read Pulse High to Data Bus at High-Z(3)	t_{RHZ}		15		15		15	ns
Write Cycle Time	t_{WC}	20		25		30		ns
Write Pulse Width(2)	t_{WPW}	12		15		20		ns
Write Recovery Time	t_{WR}	8		10		10		ns
Data Setup Time	t_{DS}	8		10		12		ns
Data Hold Time	t_{DH}	0		0		0		ns
Reset Cycle Time	t_{RSC}	20		25		30		ns
Reset Pulse Width(2)	t_{RS}	12		15		20		ns
Reset Recovery Time	t_{RSR}	8		10		10		ns
Retransmit Cycle Time	t_{RTC}	25		25		30		ns
Retransmit Pulse Width(2)	t_{RT}	15		15		20		ns
Retransmit Recovery Time	t_{RTR}	10		10		10		ns
Reset to Empty Flag Low	t_{EFL}		20		25		30	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		20		25		30	ns
Read Low to Empty Flag High	t_{REF}		20		20		20	ns
Read High to Full Flag High	t_{RFF}		20		20		20	ns
Write High to Empty Flag High	t_{WEF}		20		20		20	ns
Write Low to Full Flag Low	t_{WFF}		20		20		20	ns
Write Low to Half-Full Flag Low	t_{WHF}				25		30	ns
Read High to Half-Full Flag High	t_{RHF}				25		30	ns
Expansion Out Low Delay from Clock	t_{XOL}		16		20		20	ns
Expansion Out High Delay from Clock	t_{XOH}(4)		16		20		20	ns
$\overline{XI}$ Pulse Width	t_{PXI}	12		15		20		ns
$\overline{XI}$ Recovery Time	t_{XIR}	8		10		10		ns
$\overline{XI}$ Set-Up to Write or Clock	t_{XIS}	8		10		12		ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	KM75C02A-25		KM75C02A-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		ns
Access Time	t_A		25		35	ns
Read Recovery Time	t_{RR}	10		10		ns
Read Pulse Width[2]	t_{RPW}	25		35		ns
Data Valid from Read Pulse High	t_{DV}	5		5		ns
Read Pulse High to Data Bus at High-Z[1]	t_{RHZ}		20		20	ns
Write Cycle Time	t_{WC}	35		45		ns
Write Pulse Width[2]	t_{WPW}	25		35		ns
Write Recovery Time	t_{WR}	10		10		ns
Data Setup Time	t_{DS}	15		18		ns
Data Hold Time	t_{DH}	0		0		ns
Reset Cycle Time	t_{RSC}	35		45		ns
Reset Pulse Width[2]	t_{RS}	25		35		ns
Reset Recovery Time	t_{RSR}	10		10		ns
Retransmit Cycle Time	t_{RTC}	35		45		ns
Retransmit Pulse Width[2]	t_{RT}	25		35		ns
Retransmit Recovery Time	t_{RTR}	10		10		ns
Reset to Empty Flag Low	t_{EFL}		35		45	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		35		45	ns
Read Low to Empty Flag High	t_{REF}		25		30	ns
Read High to Full Flag High	t_{RFF}		25		30	ns
Write High to Empty Flag High	t_{WEF}		25		30	ns
Write Low to Full Flag Low	t_{WFF}		25		30	ns
Write Low to Half-Full Flag Low	t_{WHF}		35		45	ns
Read High to Half-Full Flag High	t_{RHF}		35		45	ns
Expansion Out Low Delay from Clock	t_{XOL}		25		35	ns
Expansion Out High Delay from Clock	t_{XOH}[4]		25		35	ns
XI Pulse Width	t_{PXI}	25		35		ns
XI Recovery Time	t_{XIR}	10		10		ns
XI Set-Up to Write or Clock	t_{XIS}	15		15		ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

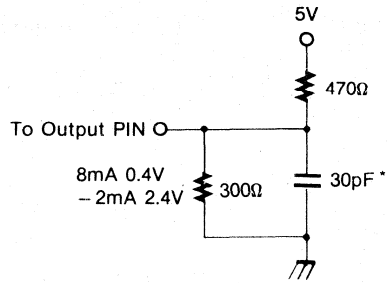
Parameter	Symbol	KM75C02A-50		KM75C02A-80		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	65		100		ns
Access Time	t_A		50		80	ns
Read Recovery Time	t_{RR}	15		20		ns
Read Pulse Width[2]	t_{RPW}	50		80		ns
Data Valid from Read Pulse High	t_{DV}	5		5		ns
Read Pulse High to Data Bus at High-Z[3]	t_{RHZ}		30		30	ns
Write Cycle Time	t_{WC}	65		100		ns
Write Pulse Width[2]	t_{WPW}	50		80		ns
Write Recovery Time	t_{WR}	15		20		ns
Data Setup Time	t_{DS}	30		40		ns
Data Hold Time	t_{DH}	5		10		ns
Reset Cycle Time	t_{RSC}	65		100		ns
Reset Pulse Width[2]	t_{RS}	50		80		ns
Reset Recovery Time	t_{RSR}	15		20		ns
Retransmit Cycle Time	t_{RTC}	65		100		ns
Retransmit Pulse Width[2]	t_{RT}	50		80		ns
Retransmit Recovery Time	t_{RTR}	15		20		ns
Reset to Empty Flag Low	t_{EFL}		65		100	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		65		100	ns
Read Low to Empty Flag High	t_{REF}		45		60	ns
Read High to Full Flag High	t_{RFF}		45		60	ns
Write High to Empty Flag High	t_{WEF}		45		60	ns
Write Low to Full Flag Low	t_{WFF}		45		60	ns
Write Low to Half-Full Flag Low	t_{WHF}		65		100	ns
Read High to Half-Full Flag High	t_{RHF}		65		100	ns
Expansion Out Low Delay from Clock	t_{XOL}		50		80	ns
Expansion Out High Delay from Clock	t_{XOH}[4]		50		65	ns
$\overline{XI}$ Pulse Width	t_{PXI}	50		80		ns
$\overline{XI}$ Recovery Time	t_{XIR}	15		20		ns
$\overline{XI}$ Set-Up to Write or Clock	t_{XIS}	15		15		ns

Notes: 1. Timings referenced as in AC Test Conditions
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested
4. t_{XOH} is guaranteed to be greater than or equal to t_{XOL} under all conditions.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

Figure 1. Output Load



* INCLUDES JIG AND SCOPE CAPACITANCES

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

Note: This parameter is sampled and not 100% tested.

Note: Generation $\overline{R}/\overline{W}$ Signals-When using these high-speed FIFO devices, it is necessary to have clean inputs on the $\overline{R}$ and $\overline{W}$ signals. It is important not to have glitches, spikes or ringing on the $\overline{R}$, $\overline{W}$ (that violate the V_{IL}, V_{IH} requirements); although the minimum pulse width low for the $\overline{R}$ and $\overline{W}$ are specified in tens of nanosecond, a glitch of 3ns can affect the read or write pointer and cause it to increment.

Master Reset ($\overline{RS}$)

Reset is accomplished whenever the MASTER RESET ($\overline{RS}$) input is taken to a low state. During this operation, both the internal read and the internal write pointers are set to the first FIFO location. A Master Reset pulse is required to initialize the FIFO after power-up before any write operation is performed. Both $\overline{R}$ and $\overline{W}$ inputs must be inactive for t_{RPW} or t_{WPW} before the rising edge of $\overline{RS}$, and should not change for t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be set to inactive (high) level after master reset ($\overline{RS}$).

Read Enable ($\overline{R}$)

READ cycles are initiated on the falling edge of the READ ENABLE ($\overline{R}$) input provided that EMPTY-FLAG ($\overline{EF}$) is not low. Read Cycles may be initiated asynchronously to any write operation in progress. After READ ENABLE ($\overline{R}$) goes high, the data outputs will return to a high impedance condition until the next READ operation. If the FIFO is empty, the EMPTY-FLAG ($\overline{EF}$) will go low and prevent any further read cycles. The data outputs will enter the high-impedance state after completion of the last read cycle.

Write Enable ($\overline{W}$)

WRITE cycles may be initiated by a low signal at the $\overline{W}$ input provided the FULL-FLAG ($\overline{FF}$) is not set. Data is stored in the memory array sequentially independent of any read operation that may be in progress.

When more than half of the memory bytes have been filled, the HALF-FULL ($\overline{HF}$) Flag output will be set low and will remain low till the difference between the write pointer and read pointer is less than or equal to one half of the total memory bytes of the device. The HALF-FULL flag is then reset by the rising edge of the read operation.

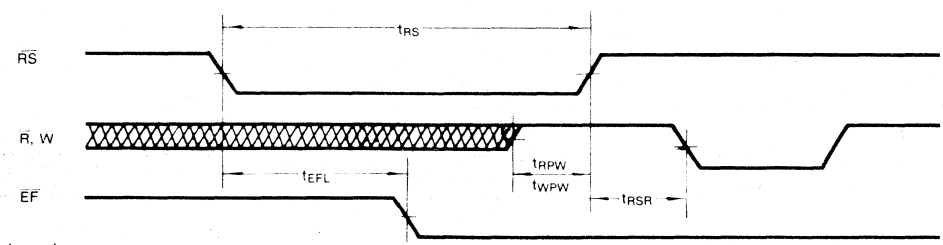
When the memory array is completely full, i.e., when the write pointer is one location from the read pointer, the FULL-FLAG ($\overline{FF}$) will go low preventing any further write operations. The FULL-FLAG will go high again t_{RFF} after completion of a valid read operation.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)

This input may be used in two different ways depending upon the configuration of EXPANSION-IN (XI):

1. Single Device or Retransmit Mode: In this mode the XI pin must be grounded. Using this mode the device can be used to retransmit data when $\overline{RT}$ is pulsed low. A retransmit operation will set the internal read pointer

Figure 2. Reset



Notes

1. $t_{RSC} = t_{RS} + t_{RSR}$
2. W and $\overline{R} = V_{IH}$ around the rising edge of RS.

to the first memory location in the array. The write pointer is unaffected. Both write enable and read enable must be inactive during the retransmit operation. This feature is particularly useful for FIFO applications in communications buffers where noise levels may be high and transmission errors are frequently detected. The retransmit feature may not be used along with depth expansion.

2. Depth Expansion Mode: In this mode the ($\overline{FL}/\overline{RT}$) pin is grounded it that device is the first of the "daisy chain." The $\overline{FL}$ pin is kept high if it is further down the chain. For details of Depth Expansion see Operating Modes.

Expansion-In ($\overline{XI}$)

This is a dual purpose input pin. As explained above, $\overline{XI}$ is grounded to indicate single device mode operation. EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device of the "daisy chain" in the Depth Expansion mode.

Full-Flag ($\overline{FF}$)

The FULL-FLAG output goes low inhibiting further write operations when the write pointer is one memory location from the read pointer i.e. the memory array is full. The total length of the memory array is 1024 bytes write operations for the KM75C02A.

Expansion Out/Half-Full Flag ($\overline{XO}/\overline{HF}$)

This output may be used in two different ways:

Single Device Mode: In this mode this output acts as a HALF-FULL Flag. After half the memory locations are full, and at the falling edge of the next write operation, the $\overline{HF}$ output is set to low. It is reset to high if the difference between the write pointer and the read pointer is half the memory depth or less at the rising edge of the read operation.

Depth Expansion Mode: In this mode EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device of the "daisy chain." In this way a signal can be passed onto the next device when the current device reaches the last memory location.

FIFO's can also be expanded simultaneously in depth and width to provide word widths greater than 9 in increments of 9. Consequently, any depth or width FIFO can be created. When expanding in depth, a composite $\overline{FF}$ must be created by OR-ing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by OR-ing the $\overline{EF}$'s together. $\overline{HF}$ and $\overline{RT}$ functions are available in Depth Expansion Mode.

Single Device/Width Expansion Mode: Single Device and Width Expansion Modes are entered by grounding $\overline{XI}$ during a MR cycle. During these modes the $\overline{HF}$ and $\overline{RT}$ features are available. FIFO's can be expanded in width to provide word widths greater than 9 in increments of 9. During Width Expansion Mode all control line inputs are common to all devices and flag outputs from any device can be monitored.

Figure 3. Asynchronous Write and Read Operation

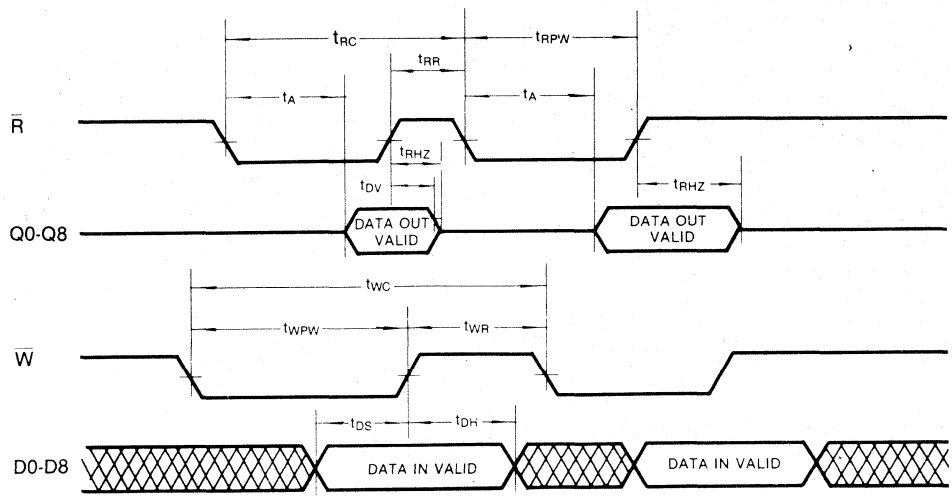


Figure 4. Full Flag From Last Write to First Read

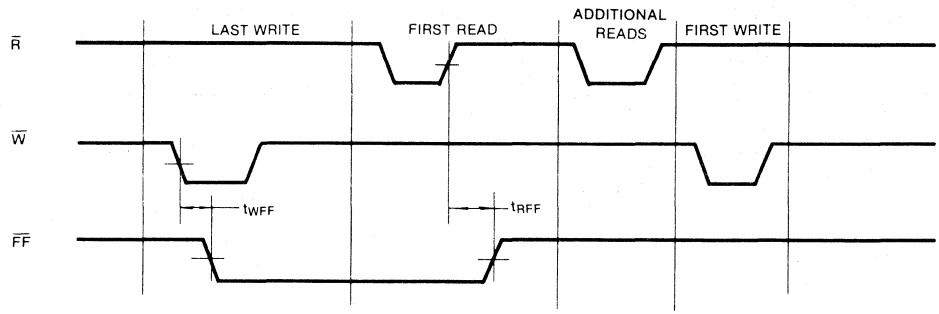


Figure 5. Empty Flag From Last Read to First Write

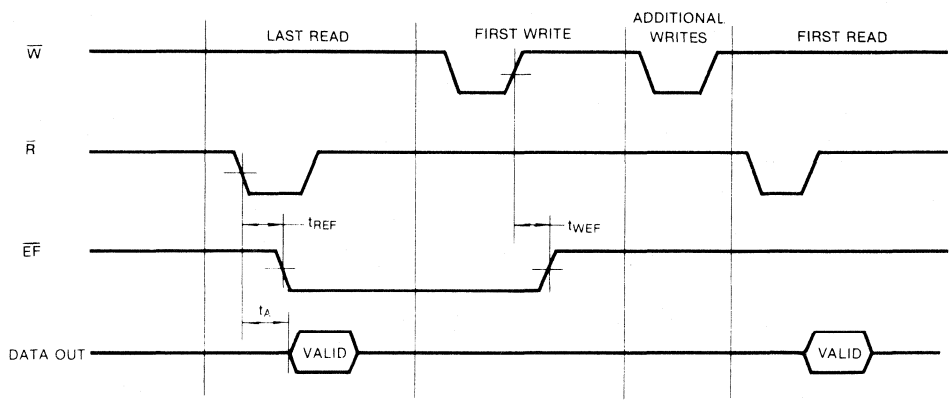
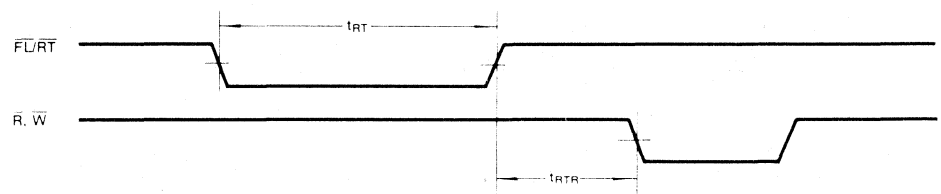


Figure 6. Retransmit



Notes:

1. $t_{RTC} = t_{RT} + t_{RTR}$
2. $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

Figure 7. Expansion-In Timing Diagram

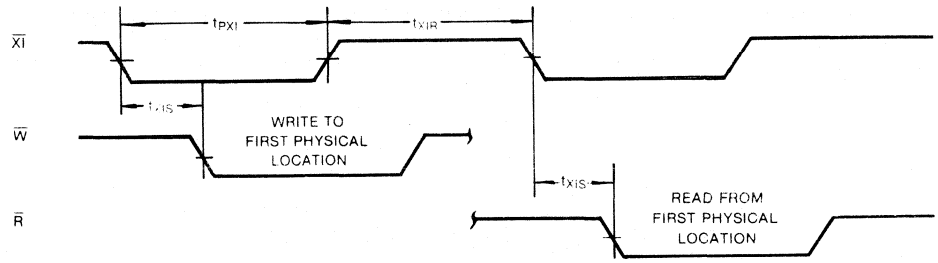


Figure 8. Expansion-Out Timing Diagram

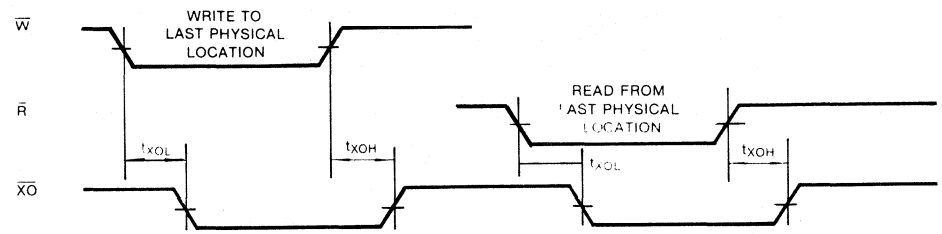
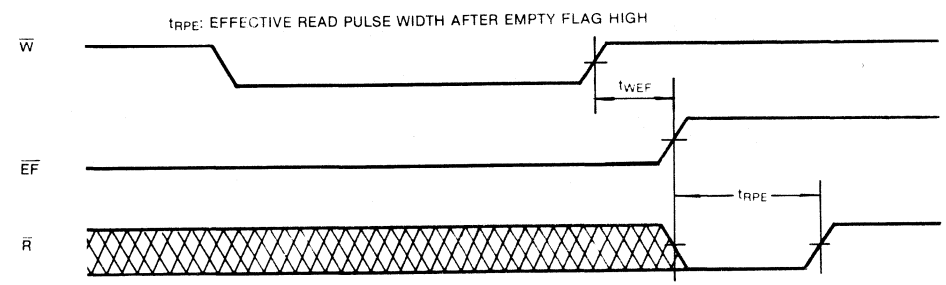


Figure 9. Empty Flag Timing



Note: 1. ($t_{RPE} = t_{RPW}$)

Figure 10. Full Flag Timing

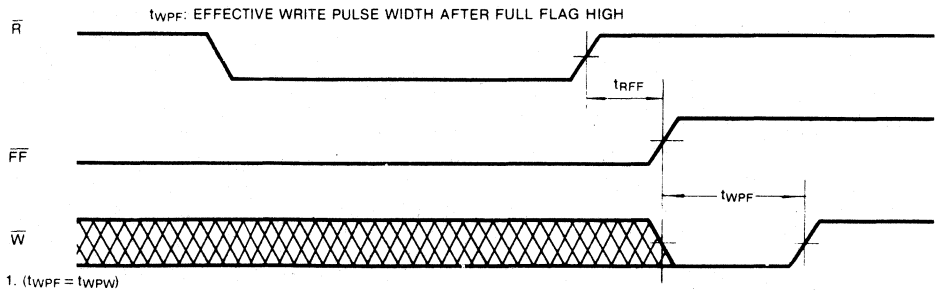
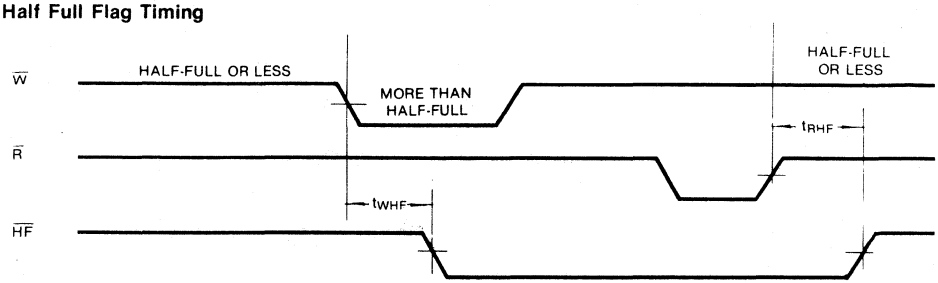


Figure 11. Half Full Flag Timing



OPERATING MODES

Single Device Mode

A single KM75C02A may be used when the application requirements are for 1024 words or less, the device is placed in a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is grounded (See Figure 12). In this mode the HALF-FULL FLAG ($\overline{HF}$) and RETRANSMIT ($\overline{RT}$) features are available.

Figure 12. Block Diagram of Single 1024 x 9 FIFO

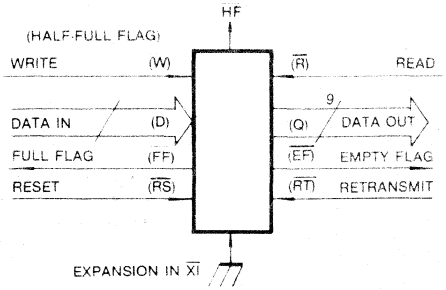
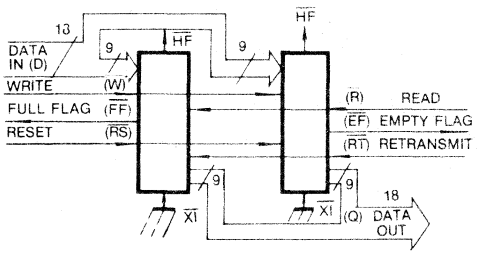


Figure 13. Block Diagram of 1024 x 18 FIFO Memory Used in Width Expansion Mode



Notes: Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Width Expansion Mode

Word width may be increased simply by connecting he corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two KM75C02A. Any word width can be attained by adding additional KM75C02A.

Depth Expansion (Daisy Chain) Mode

The KM75C02A can easily be adapted to applications when the requirements are for greater than 1024 words. Figure 14 demonstrates Depth Expansion using three KM75C02A. Any depth can be attained by adding additional KM75C02A. The KM75C02A operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the FIRST LOAD ($\overline{FL}$) control input. The RETRANSMIT feature is not available in this mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. The half-full flag ($\overline{HF}$) function is not available in this mode.
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

Compound Expansion Mode

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (See Figure 15).

Bidirectional Mode

Applications which required data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing KM75C02A as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system; (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through Modes

This sect taken to bes two special conditions—when the FIFO is full or empty. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a tri-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge would deassert the emptly flag); however, the same word (written the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data (from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

TRUTH TABLES

Table 1. Reset and Retransmit-Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment (1)	Increment (1)	X	X	X

Note: 1. Pointer will increment if flag is high

Table 2. Reset and First Load Truth Table-Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{HF}$
Reset	0	0	(1)	Location Zero	Location Zero	0	1
Retransmit	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

Note: 1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.
$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output,
$\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output.

Figure 14. Block Diagram of 1536 x 9 FIFO Memory (Depth Expansion)

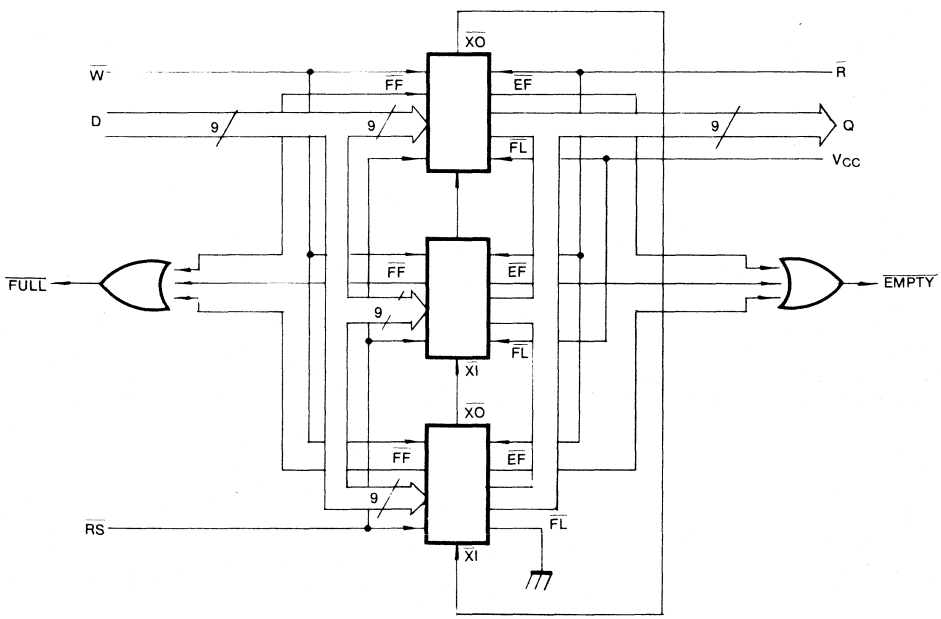


Figure 15. Compound FIFO Expansion

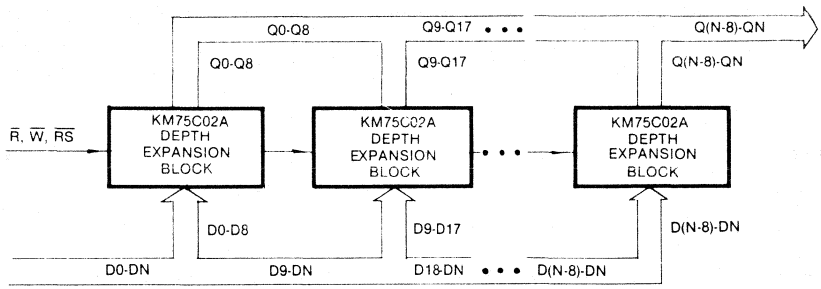
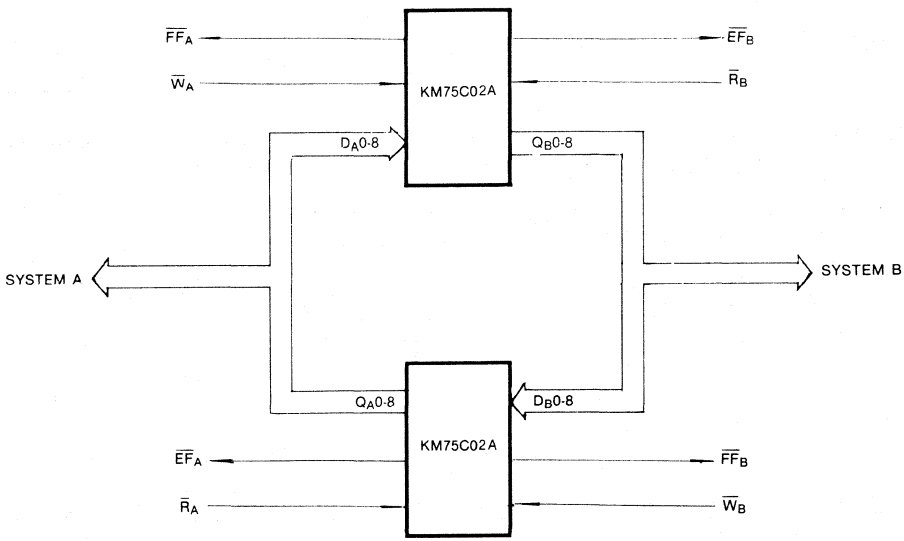
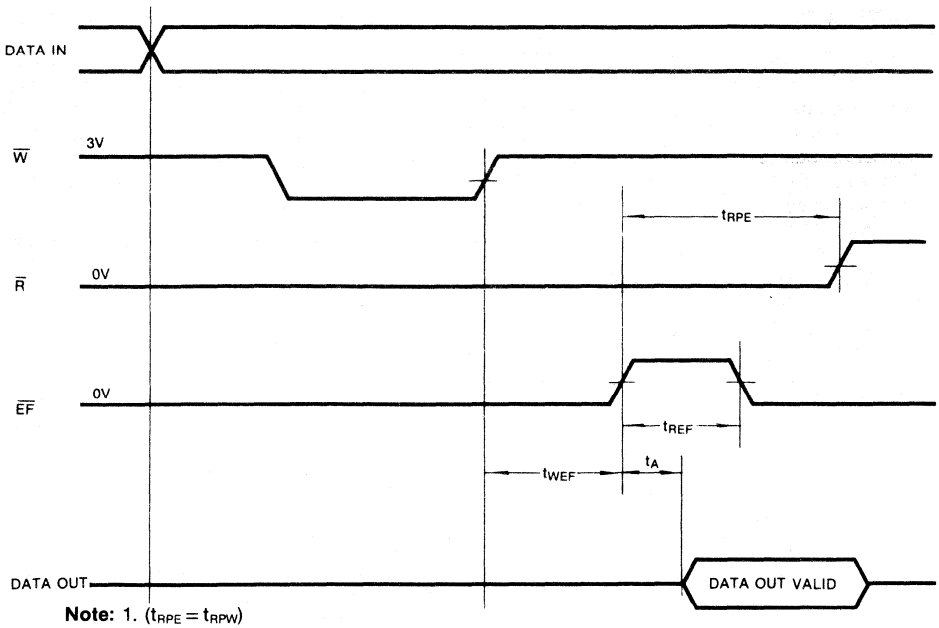


Figure 16. Bidirectional FIFO Mode



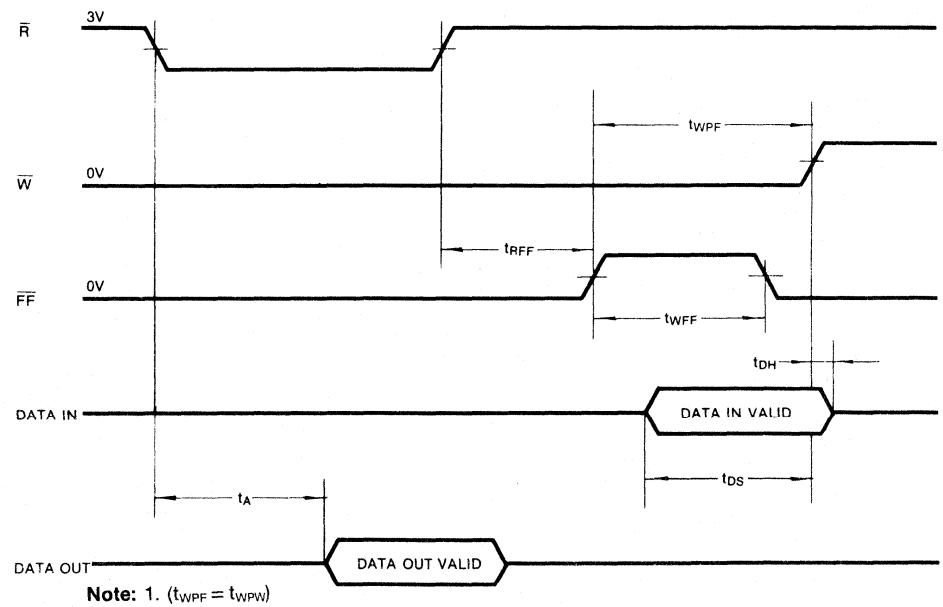
Notes:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 14.
2. For detection see WIDTH EXPANSION Section and Figure 13.

Figure 17. Read Data Flow Through Mode



Note: 1. ($t_{RPE} = t_{RPW}$)

Figure 18. Write Data Flow Through Mode



Note: 1. ($t_{WPF} = t_{WPW}$)

First-in First-out (FIFO) 2048 x 9 CMOS Memory

FEATURES

- **First-in, First-out dual port memory**
  - **2048 x 9 organization**
- **Very high speed independent of depth/width**
  - **20ns cycle times**
- **Asynchronous and simultaneous read and write**
- **Fully expandable by both word depth and/or width**
- **Low power consumption**
  - **Active: 150mA (max)**
  - **Power Down: 15mA (max)**
- **Half-full flag capability in standalone mode**
- **Empty and full warning flags**
- **Auto retransmit capability in standalone mode**
- **High performance 1.2 micron CMOS technology**
- **Available in 300 mil and 600 mil Plastic DIP and 32 pin PLCC**

DESCRIPTION

The KM75C03A is dual port memory that implements a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. Full and empty flags are provided to prevent data overflow. Expansion logic allows unlimited expansion capability in both word size and depth without any loss in speed.

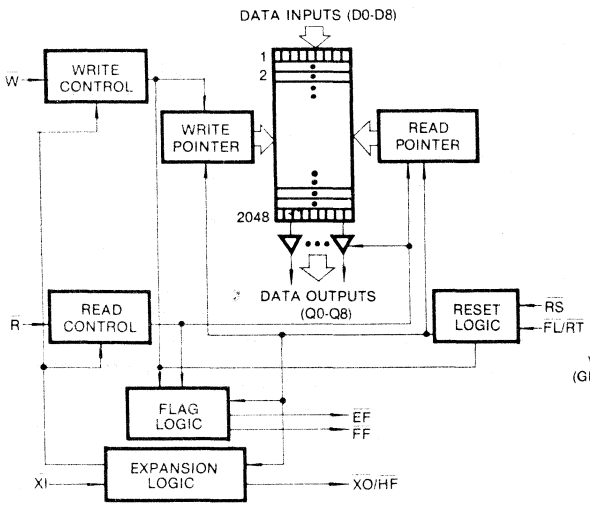
No address information is required for KM75C03A. Ring counters automatically generate the addresses required for every read and write operations. Data is toggled in and out of the device through the use of WRITE($\overline{W}$) and READ($\overline{R}$) pins. The device has a read/write cycle time of 20nsec (50MHz).

The device consists of a 9-bit wide array which is very useful in applications such as data communications where it is necessary to use parity bit. The RETRANSMIT ($\overline{RT}$) feature allows to re-read the previously read data. A half-full flag is available in the single device and width expansion modes.

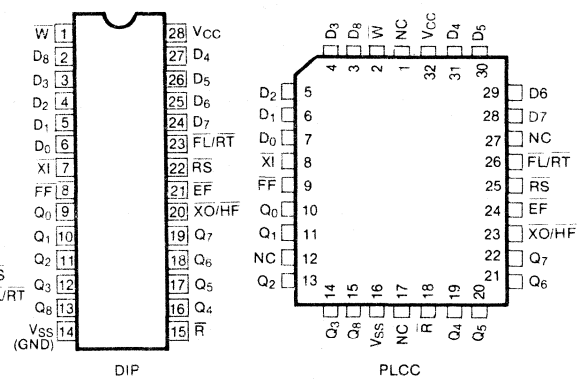
The KM75C03A is fabricated using proprietary high speed CMOS 1.2 micron technology. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS (Top Views)



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage On Any Pin Relative to V_{SS}	V_{IN}	−0.5 to 7.0	V
Operating Temperature	T_A	0 to +70	°C
Temperature Under Bias	T_{bias}	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to 150	°C
Power Dissipation	P_D	1.0	W
DC Output Current	I_{OUT}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0			V
Input Low Voltage	V_{IL}			0.8	V

DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$)

Parameter	Symbol	T_A = 15/20ns			T_A = 25ns			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Active Current	I_{CC}			150			120	mA
V_{CC} Standby Current-TTL[1] ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$)	I_{SB1}			15			15	mA
V_{CC} Standby Current-CMOS[1] (all inputs = V_{CC}-0.2V)	I_{SB2}			5			5	mA
Input Leakage Current[2]	I_{LI}	−1		1	−1		1	μA
Output Leakage Current[3]	I_{LO}	−10		10	−10		10	μA
Output High Voltage Level (I_{OH} = −2mA)	V_{OH}	2.4			2.4			V
Output Low Voltage Level (I_{OL} = 8mA)	V_{OL}			0.4			0.4	V

DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$)

Parameter	Symbol	T_A = 35ns			T_A = 50ns			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Active Current	I_{CC}			100			60	mA
V_{CC} Standby Current-TTL[1] ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$)	I_{SB1}			15			15	mA
V_{CC} Standby Current-CMOS[1] (all inputs = V_{CC}-0.2V)	I_{SB2}			5			5	mA
Input Leakage Current[2]	I_{LI}	−1		1	−1		1	μA
Output Leakage Current[3]	I_{LO}	−10		10	−10		10	μA
Output High Voltage Level (I_{OH} = −2mA)	V_{OH}	2.4			2.4			V
Output Low Voltage Level (I_{OL} = 8mA)	V_{OL}			0.4			0.4	V

Notes: 1. I_{CC} and I_{SB} measurements are made with outputs open.
2. Measurements with $V_{SS} \leq V_{IN} \leq V_{CC}$.
3. $\overline{R} \geq V_{IH}$, $V_{SS} \leq V_{OUT} \leq V_{CC}$.

AC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, T_A=0°C to + 70°C)

Parameter	Symbol	KM75C03A-12		KM75C03A-15		KM75C03A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20		25		30		ns
Access Time	t_A		12		15		20	ns
Read Recovery Time	t_{RR}	8		10		10		ns
Read Pulse Width(2)	t_{RPW}	12		15		20		ns
Data Valid from Read Pulse High	t_{DV}	5		5		5		ns
Read Pulse High to Data Bus at High-Z(3)	t_{RHZ}		15		15		15	ns
Write Cycle Time	t_{WC}	20		25		30		ns
Write Pulse Width(2)	t_{WPW}	12		15		20		ns
Write Recovery Time	t_{WR}	8		10		10		ns
Data Setup Time	t_{DS}	8		10		12		ns
Data Hold Time	t_{DH}	0		0		0		ns
Reset Cycle Time	t_{RSC}	20		25		30		ns
Reset Pulse Width(2)	t_{RS}	12		15		20		ns
Reset Recovery Time	t_{RSR}	8		10		10		ns
Retransmit Cycle Time	t_{RTC}	25		25		30		ns
Retransmit Pulse Width(2)	t_{RT}	15		15		20		ns
Retransmit Recovery Time	t_{RTR}	10		10		10		ns
Reset to Empty Flag Low	t_{EFL}		20		25		30	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		20		25		30	ns
Read Low to Empty Flag High	t_{REF}		20		20		20	ns
Read High to Full Flag High	t_{RFF}		20		20		20	ns
Write High to Empty Flag High	t_{WEF}		20		20		20	ns
Write Low to Full Flag Low	t_{WFF}		20		20		20	ns
Write Low to Half-Full Flag Low	t_{WHF}				25		30	ns
Read High to Half-Full Flag High	t_{RHF}				25		30	ns
Expansion Out Low Delay from Clock	t_{XOL}		16		20		20	ns
Expansion Out High Delay from Clock	t_{XOH}(4)		16		20		20	ns
$\overline{XI}$ Pulse Width	t_{PXI}	12		15		20		ns
$\overline{XI}$ Recovery Time	t_{XIR}	8		10		10		ns
$\overline{XI}$ Set-Up to Write or Clock	t_{XIS}	8		10		12		ns

3

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	KM75C03A-25		KM75C03A-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		ns
Access Time	t_A		25		35	ns
Read Recovery Time	t_{RR}	10		10		ns
Read Pulse Width[2]	t_{RPW}	25		35		ns
Data Valid from Read Pulse High	t_{DV}	5		5		ns
Read Pulse High to Data Bus at High-Z[1]	t_{RHZ}		20		20	ns
Write Cycle Time	t_{WC}	35		45		ns
Write Pulse Width[2]	t_{WPW}	25		35		ns
Write Recovery Time	t_{WR}	10		10		ns
Data Setup Time	t_{DS}	15		18		ns
Data Hold Time	t_{DH}	0		0		ns
Reset Cycle Time	t_{RSC}	35		45		ns
Reset Pulse Width[2]	t_{RS}	25		35		ns
Reset Recovery Time	t_{RSR}	10		10		ns
Retransmit Cycle Time	t_{RTC}	35		45		ns
Retransmit Pulse Width[2]	t_{RT}	25		35		ns
Retransmit Recovery Time	t_{RTR}	10		10		ns
Reset to Empty Flag Low	t_{EFL}		35		45	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		35		45	ns
Read Low to Empty Flag High	t_{REF}		25		30	ns
Read High to Full Flag High	t_{RFF}		25		30	ns
Write High to Empty Flag High	t_{WEF}		25		30	ns
Write Low to Full Flag Low	t_{WFF}		25		30	ns
Write Low to Half-Full Flag Low	t_{WHF}		35		45	ns
Read High to Half-Full Flag High	t_{RHF}		35		45	ns
Expansion Out Low Delay from Clock	t_{XOL}		25		35	ns
Expansion Out High Delay from Clock	t_{XOH}[4]		25		35	ns
$\overline{XI}$ Pulse Width	t_{PXI}	25		35		ns
$\overline{XI}$ Recovery Time	t_{XIR}	10		10		ns
$\overline{XI}$ Set-Up to Write or Clock	t_{XIS}	15		15		ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	KM75C03A-50		KM75C03A-80		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	65		100		ns
Access Time	t_A		50		80	ns
Read Recovery Time	t_{RR}	15		20		ns
Read Pulse Width[2]	t_{RPW}	50		80		ns
Data Valid from Read Pulse High	t_{DV}	5		5		ns
Read Pulse High to Data Bus at High-Z[3]	t_{RHZ}		30		30	ns
Write Cycle Time	t_{WC}	65		100		ns
Write Pulse Width[2]	t_{WPW}	50		80		ns
Write Recovery Time	t_{WR}	15		20		ns
Data Setup Time	t_{DS}	30		40		ns
Data Hold Time	t_{DH}	5		10		ns
Reset Cycle Time	t_{RSC}	65		100		ns
Reset Pulse Width[2]	t_{RS}	50		80		ns
Reset Recovery Time	t_{RSR}	15		20		ns
Retransmit Cycle Time	t_{RTC}	65		100		ns
Retransmit Pulse Width[2]	t_{RT}	50		80		ns
Retransmit Recovery Time	t_{RTR}	15		20		ns
Reset to Empty Flag Low	t_{EFL}		65		100	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		65		100	ns
Read Low to Empty Flag High	t_{REF}		45		60	ns
Read High to Full Flag High	t_{RFF}		45		60	ns
Write High to Empty Flag High	t_{WEF}		45		60	ns
Write Low to Full Flag Low	t_{WFF}		45		60	ns
Write Low to Half-Full Flag Low	t_{WHF}		65		100	ns
Read High to Half-Full Flag High	t_{RHF}		65		100	ns
Expansion Out Low Delay from Clock	t_{XOL}		50		80	ns
Expansion Out High Delay from Clock	t_{XOH}[4]		50		65	ns
$\overline{XI}$ Pulse Width	t_{PXI}	50		80		ns
$\overline{XI}$ Recovery Time	t_{XIR}	15		20		ns
$\overline{XI}$ Set-Up to Write or Clock	t_{XIS}	15		15		ns

Notes: 1. Timings referenced as in AC Test Conditions
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested
4. t_{XOH} is guaranteed to be greater than or equal to t_{XOL} under all conditions.

AC TEST CONDITIONS

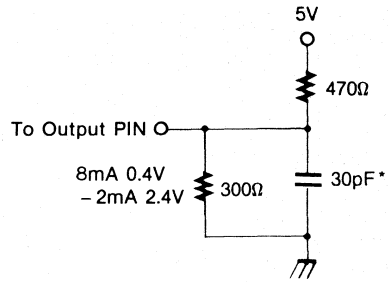
Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

Note: This parameter is sampled and not 100% tested.

Figure 1. Output Load



* INCLUDES JIG AND SCOPE CAPACITANCES

Note: Generation $\overline{R}/\overline{W}$ Signals-When using these high-speed FIFO devices, it is necessary to have clean inputs on the $\overline{R}$ and $\overline{W}$ signals. It is important not to have glitches, spikes or ringing on the $\overline{R}$, $\overline{W}$ (that violate the V_{IL}, V_{IH} requirements); although the minimum pulse width low for the $\overline{R}$ and $\overline{W}$ are specified in tens of nanosecond, a glitch of 3ns can affect the read or write pointer and cause it to increment.

Master Reset ($\overline{RS}$)

Reset is accomplished whenever the MASTER RESET ($\overline{RS}$) input is taken to a low state. During this operation, both the internal read and the internal write pointers are set to the first FIFO location. A Master Reset pulse is required to initialize the FIFO after power-up before any write operation is performed. Both $\overline{R}$ and $\overline{W}$ inputs must be inactive for t_{RPW} or t_{WPW} before the rising edge of $\overline{RS}$, and should not change for t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be set to inactive (high) level after master reset ($\overline{RS}$).

Read Enable ($\overline{R}$)

READ cycles are initiated on the falling edge of the READ ENABLE ($\overline{R}$) input provided that EMPTY-FLAG ($\overline{EF}$) is not low. Read Cycles may be initiated asynchronously to any write operation in progress. After READ ENABLE ($\overline{R}$) goes high, the data outputs will return to a high impedance condition until the next READ operation. If the FIFO is empty, the EMPTY-FLAG ($\overline{EF}$) will go low and prevent any further read cycles. The data outputs will enter the high-impedance state after completion of the last read cycle.

Write Enable ($\overline{W}$)

WRITE cycles may be initiated by a low signal at the $\overline{W}$ input provided the FULL-FLAG ($\overline{FF}$) is not set. Data is stored in the memory array sequentially independent of any read operation that may be in progress.

When more than half of the memory bytes have been filled, the HALF-FULL ($\overline{HF}$) Flag output will be set low and will remain low till the difference between the write pointer and read pointer is less than or equal to one half of the total memory bytes of the device. The HALF-FULL flag is then reset by the rising edge of the read operation.

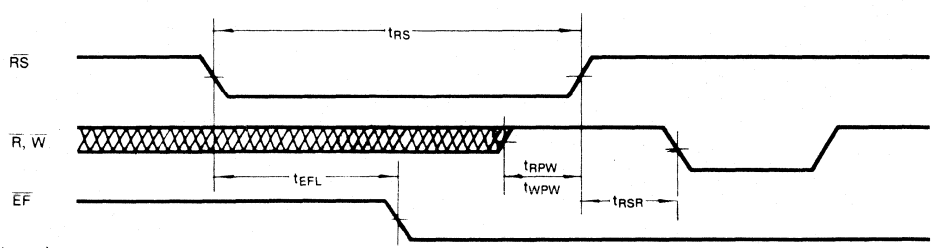
When the memory array is completely full, i.e., when the write pointer is one location from the read pointer, the FULL-FLAG ($\overline{FF}$) will go low preventing any further write operations. The FULL-FLAG will go high again t_{RFF} after completion of a valid read operation.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)

This input may be used in two different ways depending upon the configuration of EXPANSION-IN ($\overline{XI}$):

1. Single Device or Retransmit Mode: In this mode the $\overline{XI}$ pin must be grounded. Using this mode the device can be used to retransmit data when $\overline{RT}$ is pulsed low. A retransmit operation will set the internal read pointer

Figure 2. Reset



Notes

1. $t_{RSC} = t_{RS} + t_{RSR}$
2. $\overline{W}$ and $\overline{R} = V_{IH}$ around the rising edge of $\overline{RS}$.

to the first memory location in the array. The write pointer is unaffected. Both write enable and read enable must be inactive during the retransmit operation. This feature is particularly useful for FIFO applications in communications buffers where noise levels may be high and transmission errors are frequently detected. The retransmit feature may not be used along with depth expansion.

2. **Depth Expansion Mode:** In this mode the ($\overline{FL}/\overline{RT}$) pin is grounded it that device is the first of the "daisy chain." The $\overline{FL}$ pin is kept high if it is further down the chain. For details of Depth Expansion see Operating Modes.

Expansion-In ($\overline{XI}$)

This is a dual purpose input pin. As explained above, $\overline{XI}$ is grounded to indicate single device mode operation. EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device of the "daisy chain" in the Depth Expansion mode.

Full-Flag ($\overline{FF}$)

The FULL-FLAG output goes low inhibiting further write operations when the write pointer is one memory location from the read pointer i.e., the memory array is full. The total length of he memory array is 2048 bytes write operations for the KM75C03A.

Expansion Out/Half-Full Flag ($\overline{XO}/\overline{HF}$)

This output may be used in two different ways:

Single Device Mode: In this mode this output acts as a HALF-FULL Flag. After half the memory locations are full, and at the falling edge of the next write operation, the $\overline{HF}$ output is set to low. It is reset to high if the difference between the write pointer and the read pointer is half the memory depth or less at the rising edge of the read operation.

Depth Expansion Mode: In this mode EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device of the "daisy chain." In this way a signal can be passed onto the next device when the current device reaches the last memory location.

FIFO's can also be expanded simultaneously in depth and width to provide word widths greater than 9 in increments of 9. Consequently, any depth or width FIFO can be created. When expanding in depth, a composite $\overline{FF}$ must be created by OR-ing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by OR-ing the $\overline{EF}$'s together. $\overline{HF}$ and $\overline{RT}$ functions are available in Depth Expansion Mode.

Single Device/Width Expansion Mode: Single Device and Width Expansion Modes are entered by grounding $\overline{XI}$ during a MR cycle. During these modes the $\overline{HF}$ and $\overline{RT}$ features are available. FIFO's can be expanded in width to provide word widths greater than 9 in increments of 9. During Width Expansion Mode all control line inputs are common to all devices and flag outputs from any device can be monitored.

Figure 3. Asynchronous Write and Read Operation

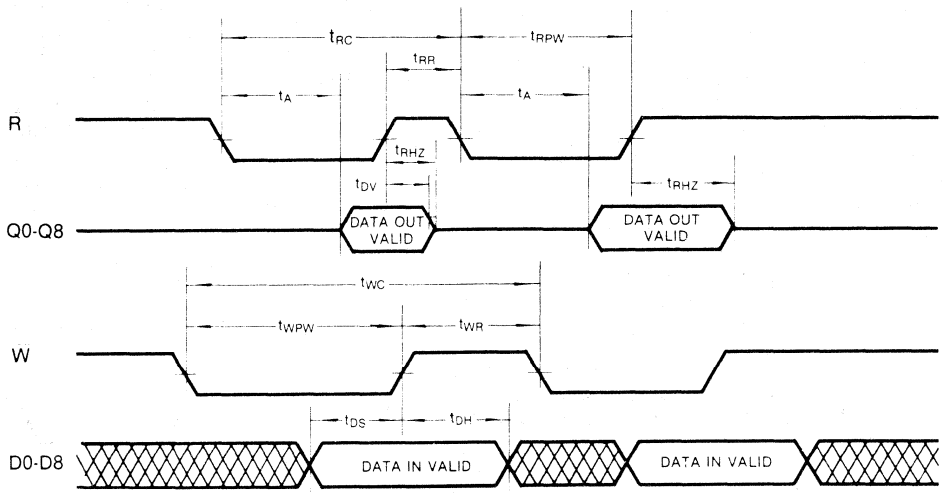


Figure 4. Full Flag From Last Write to First Read

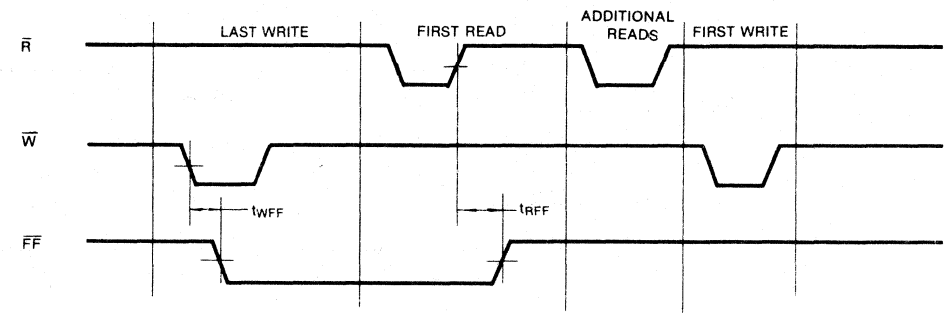


Figure 5. Empty Flag From Last Read to First Write

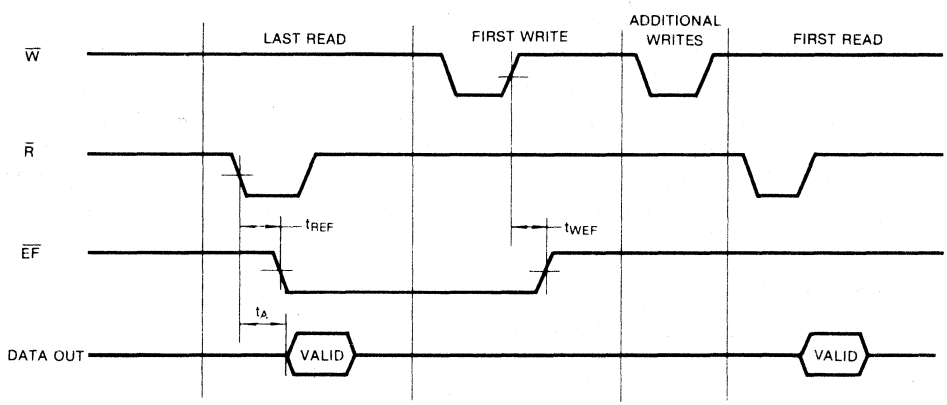
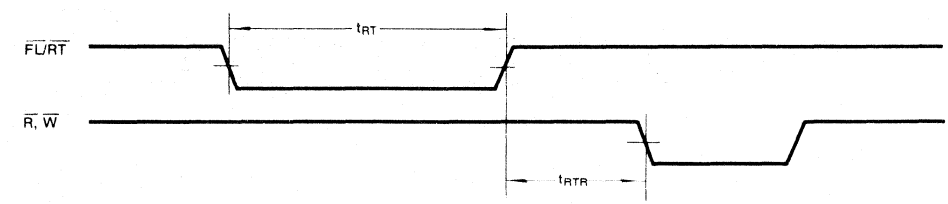


Figure 6. Retransmit



Notes:

1. $t_{RTC} = t_{RT} + t_{RTR}$
2. $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

Figure 7. Expansion-In Timing Diagram

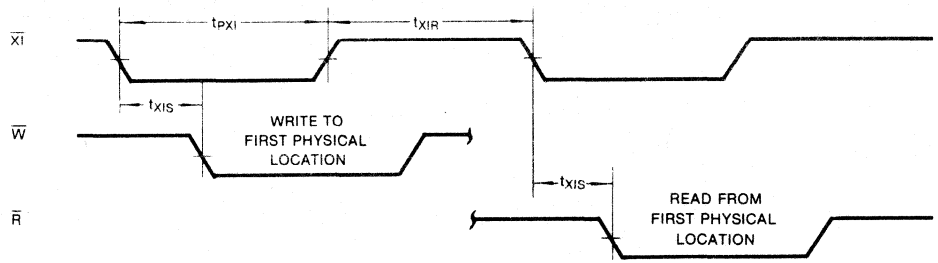


Figure 8. Expansion-Out Timing Diagram

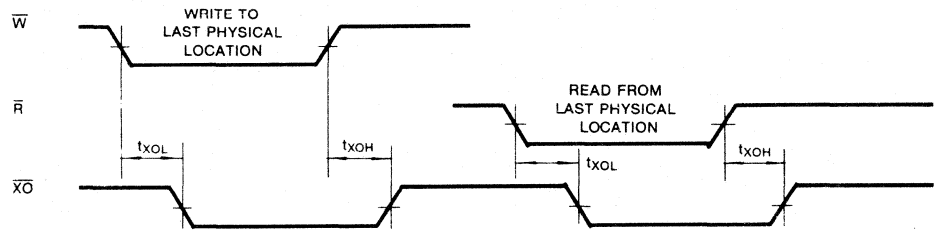
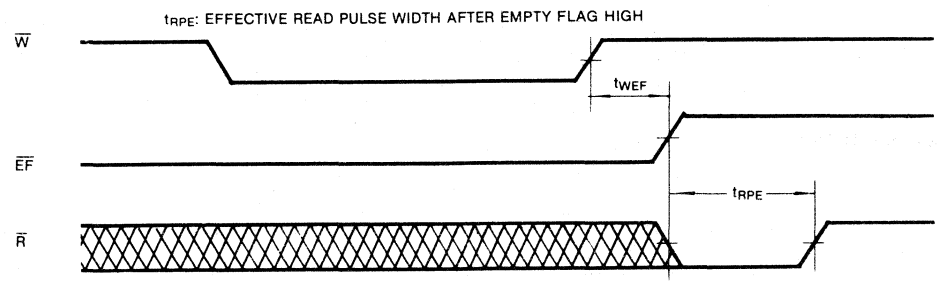


Figure 9. Empty Flag Timing



Note: 1. ($t_{RPE} = t_{RPW}$)

Figure 10. Full Flag Timing

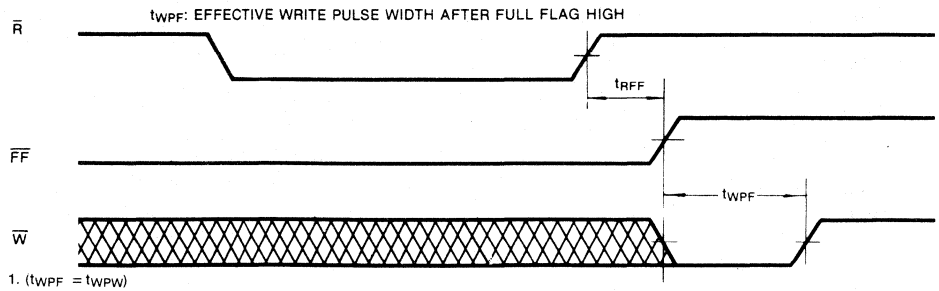
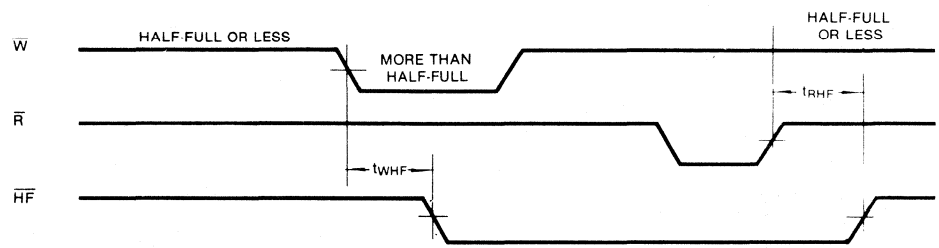


Figure 11. Half Full Flag Timing



OPERATING MODES

Single Device Mode

A single KM75C03A may be used when the application requirements are for 2048 words or less, the device is placed in a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is grounded (See Figure 12). In this mode the HALF-FULL FLAG (HF) and RETRANSMIT ($\overline{RT}$) features are available.

Figure 12. Block Diagram of Single 2048 x 9 FIFO

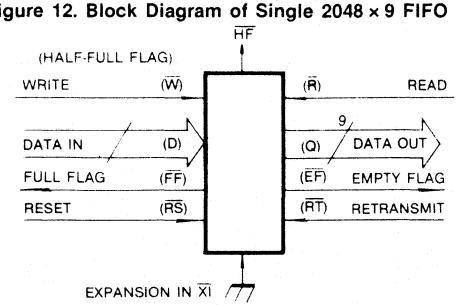
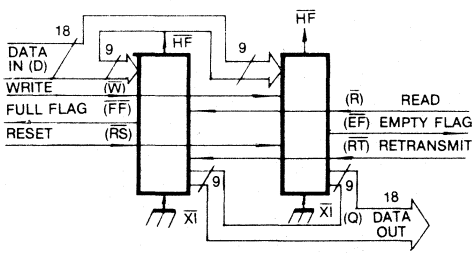


Figure 13. Block Diagram of 2048 x 18 FIFO Memory Used in Width Expansion Mode



Notes: Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Width Expansion Mode

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two KM75C03A.

Depth Expansion (Daisy Chain) Mode

The KM75C03A can easily be adapted to applications when the requirements are for greater than words. Figure 14 demonstrates Depth Expansion using three KM75C03A. Any depth can be attained by adding additional KM75C03A's. The KM75C03A operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the FIRST LOAD ($\overline{FL}$) control input. The RETRANSMIT feature is not available in this mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. The half-full flag ($\overline{HF}$) function is not available in this mode.
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

Compound Expansion Mode

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (See Figure 15).

Bidirection Mode

Applications which required data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing KM75C03A as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system; (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through Modes

This section describes two special conditions—when the FIFO is full or empty. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a tri-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge would deassert the emptly flag); however, the same word (written the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data (from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

TRUTH TABLES

Table 1. Reset and Retransmit-Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment (1)	Increment (1)	X	X	X

Note: 1. Pointer will increment if flag is high

Table 2. Reset and First Load Truth Table-Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{HF}$
Reset	0	0	(1)	Location Zero	Location Zero	0	1
Retransmit	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

Note: 1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.
$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output,
$\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output.

Figure 14. Block Diagram of 1536 x 9 FIFO Memory (Depth Expansion)

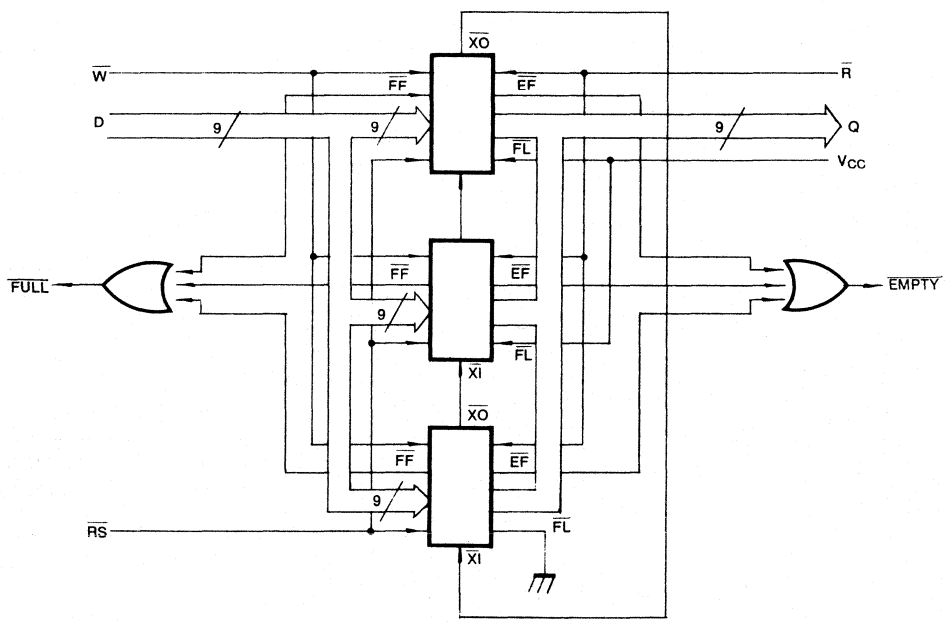


Figure 15. Compound FIFO Expansion

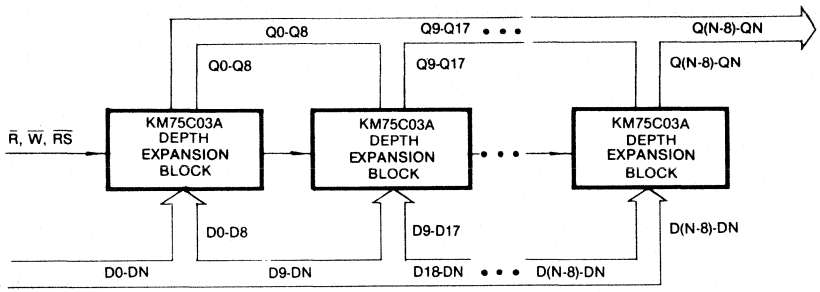
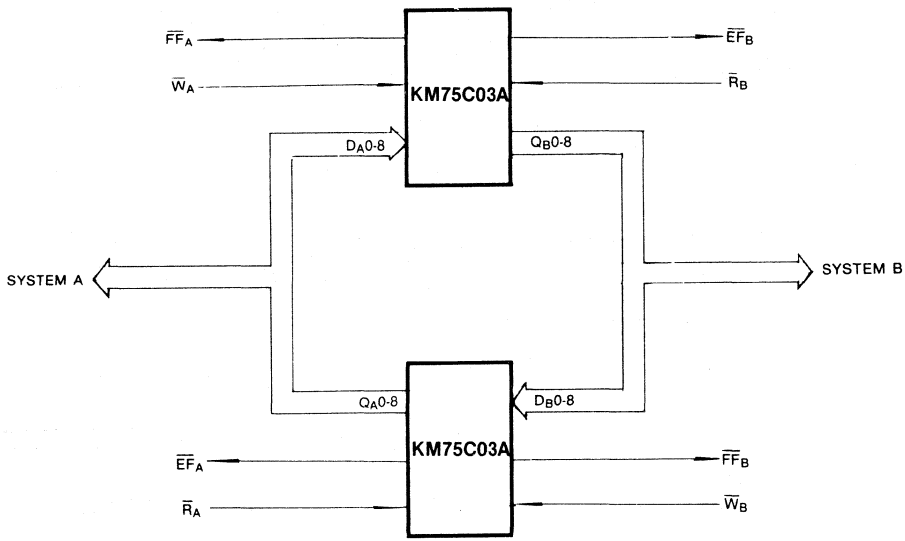
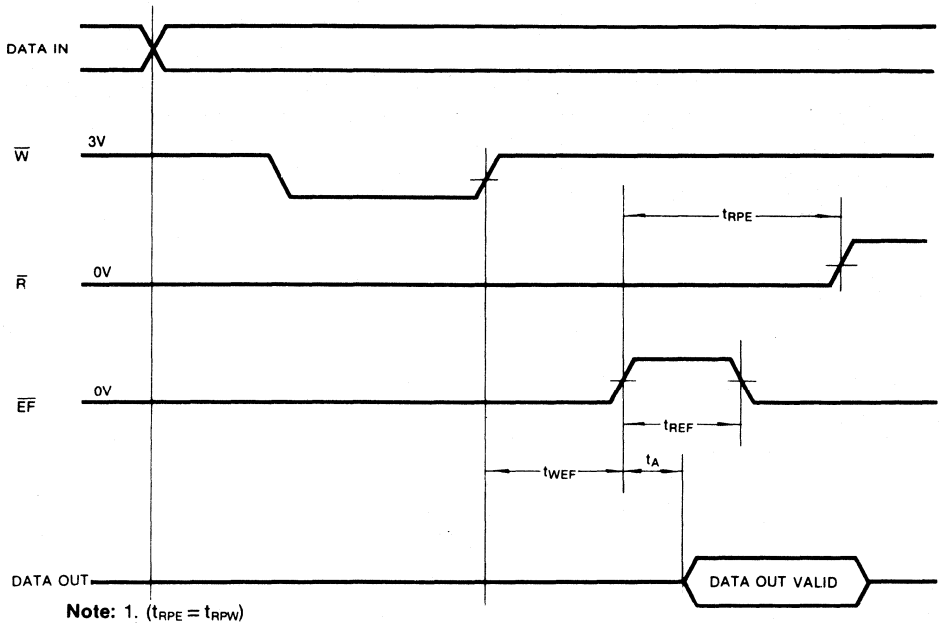


Figure 16. Bidirectional FIFO Mode



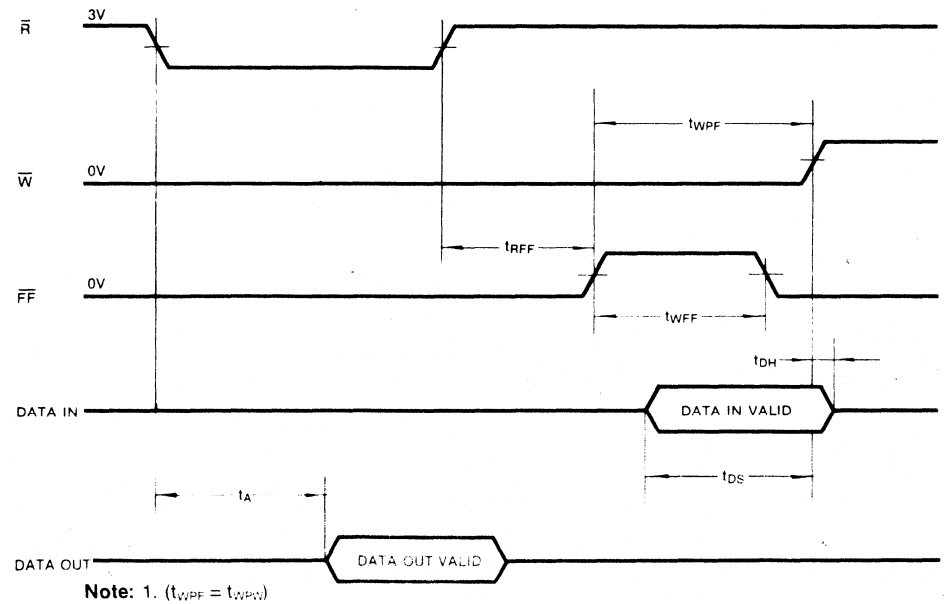
Notes:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 14.
2. For detection see WIDTH EXPANSION Section and Figure 13.

Figure 17. Read Data Flow Through Mode

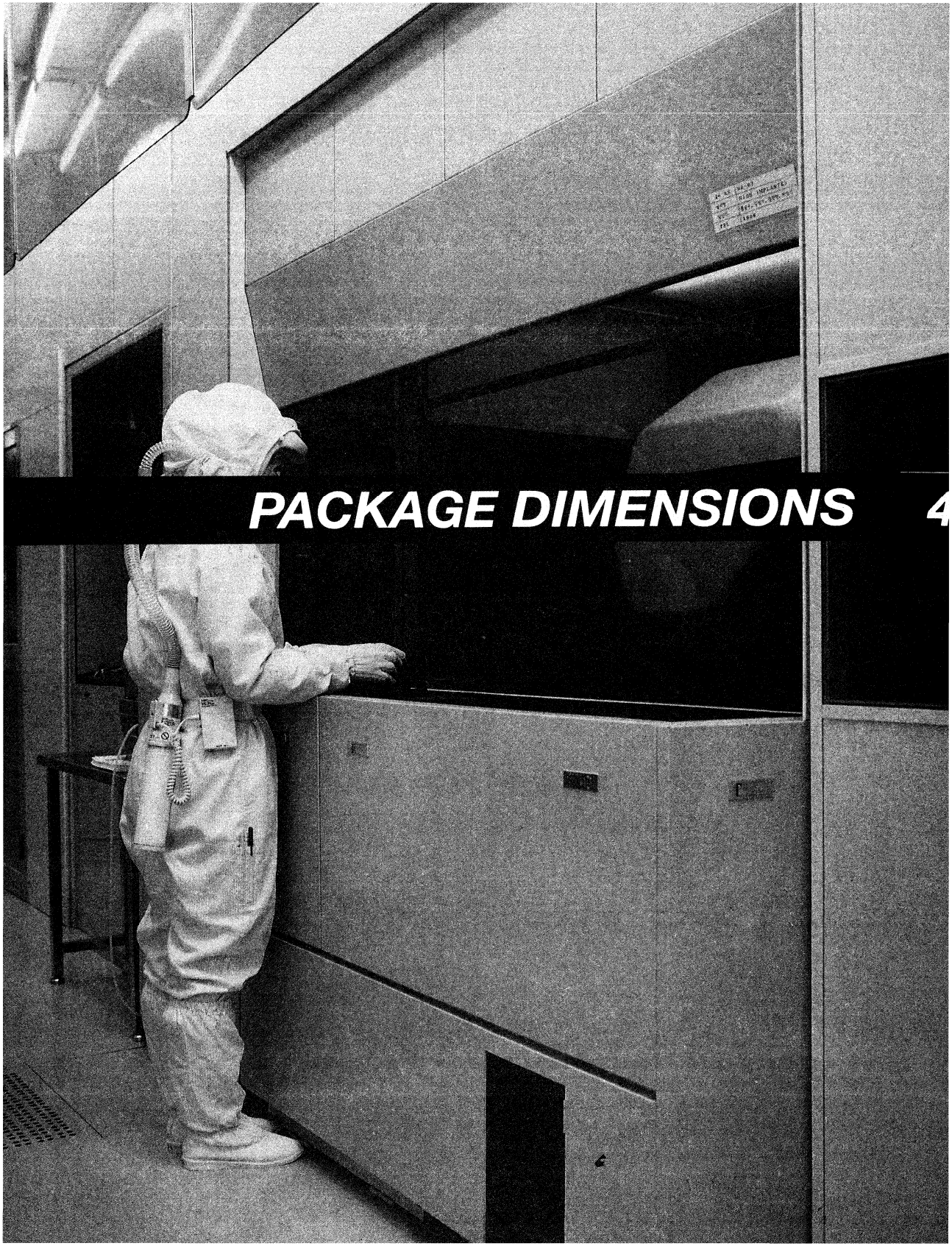


Note: 1. ($t_{RPE} = t_{RPW}$)

Figure 18. Write Data Flow Through Mode



Note: 1. ($t_{WPF} = t_{WPW}$)

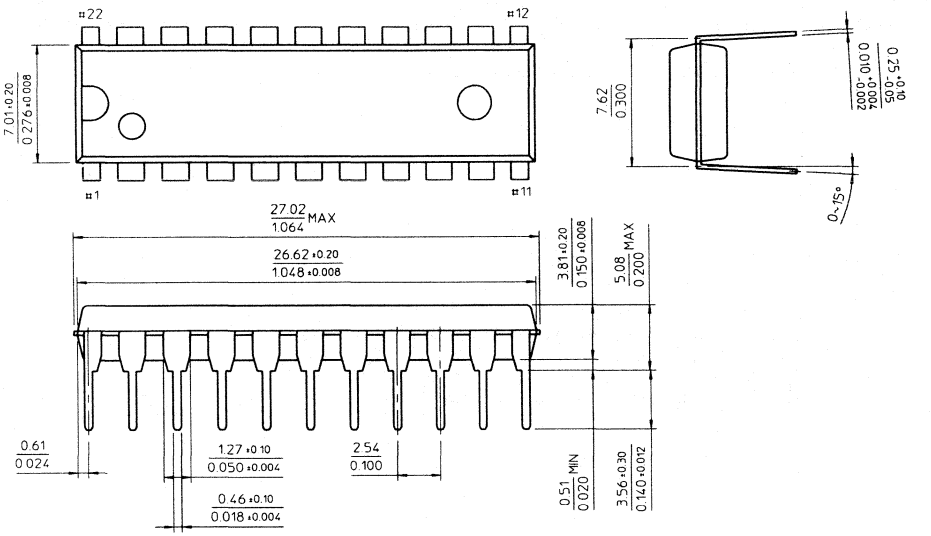


PACKAGE DIMENSIONS 4

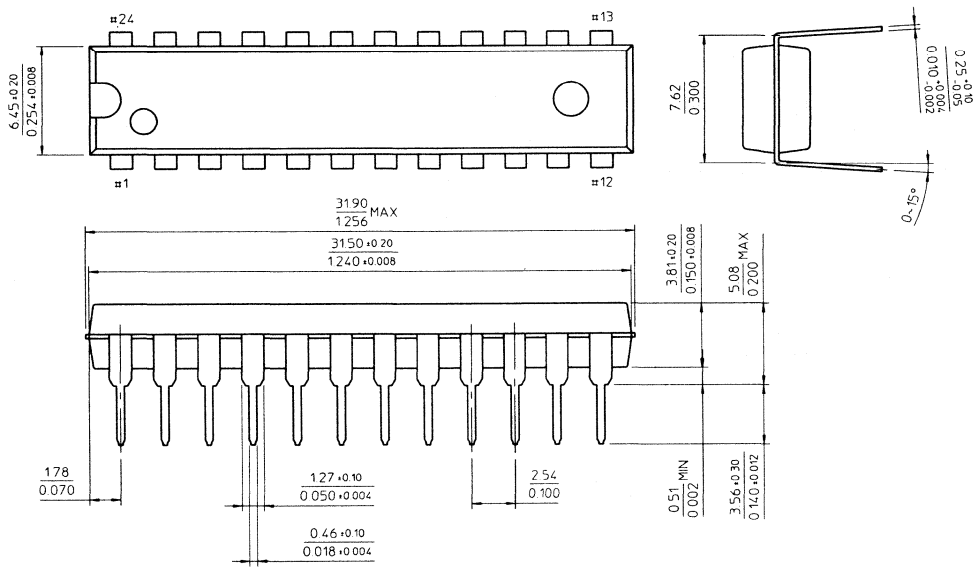
PACKAGE DIMENSIONS

Unit : mm/inch

22-DIP-300B



24-DIP-300

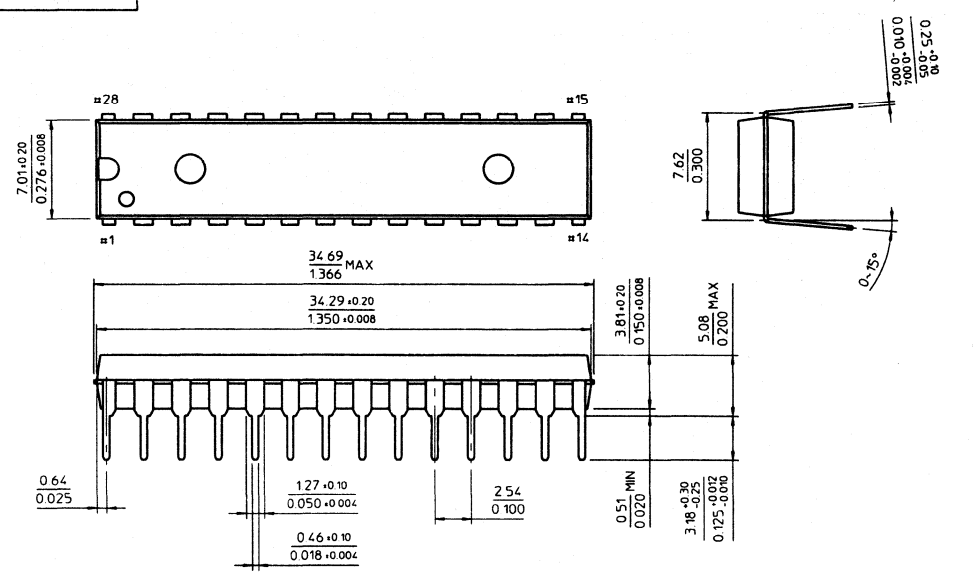


4

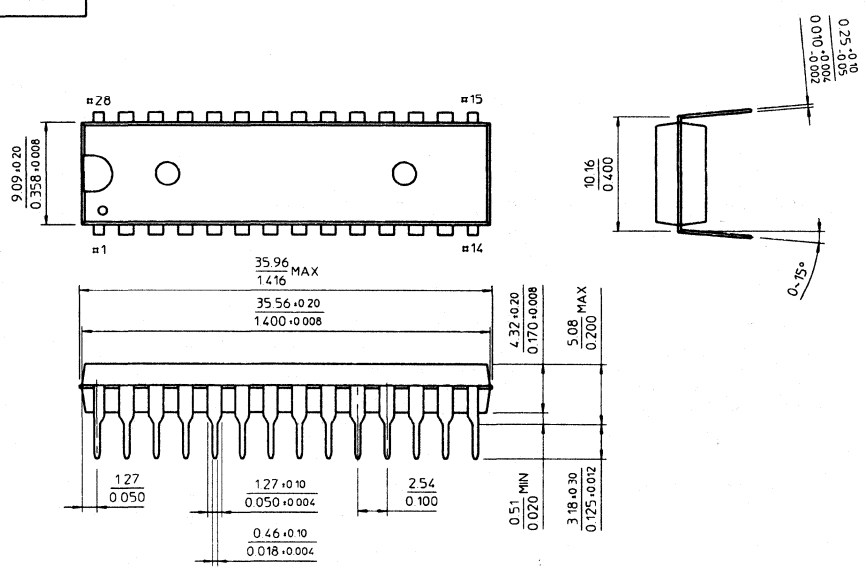
PACKAGE DIMENSIONS

Unit : mm/inch

28-DIP-300



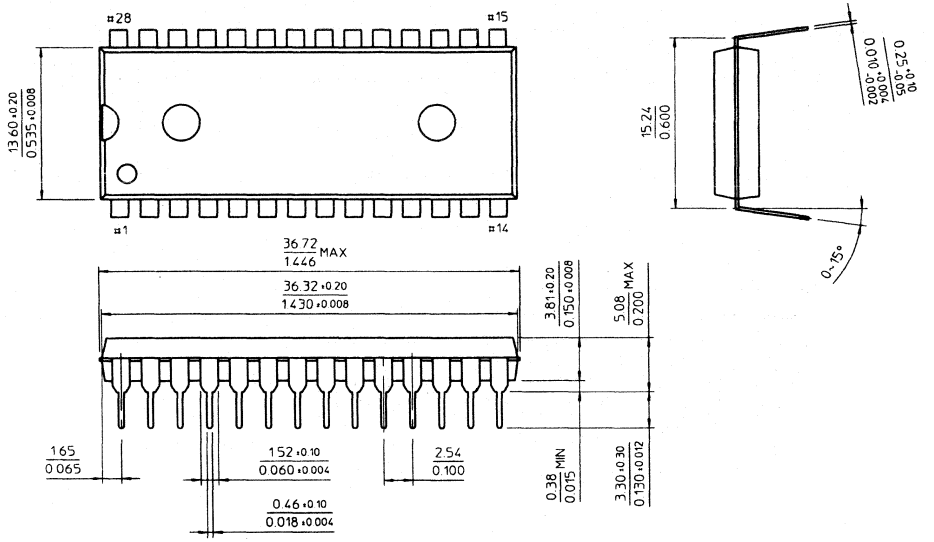
28-DIP-400



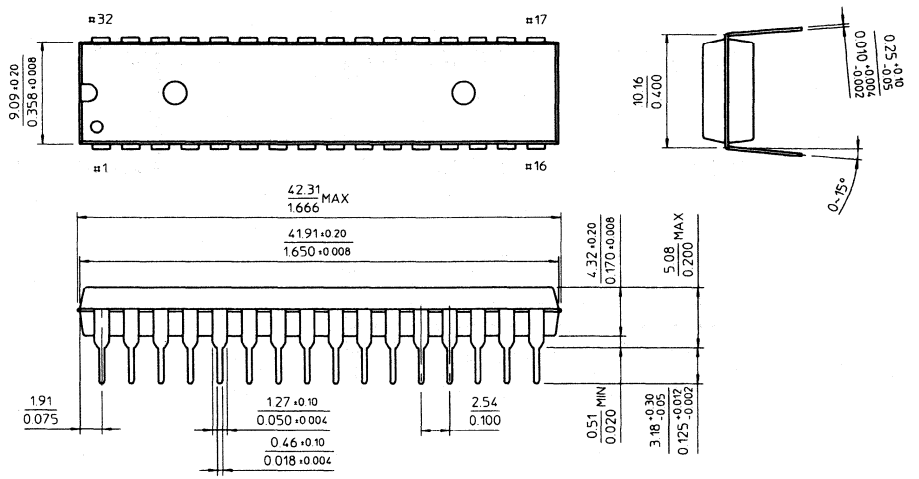
PACKAGE DIMENSIONS

Unit : mm/inch

28-DIP-600B



32-DIP-400



4

PACKAGE DIMENSIONS

Unit : mm/inch

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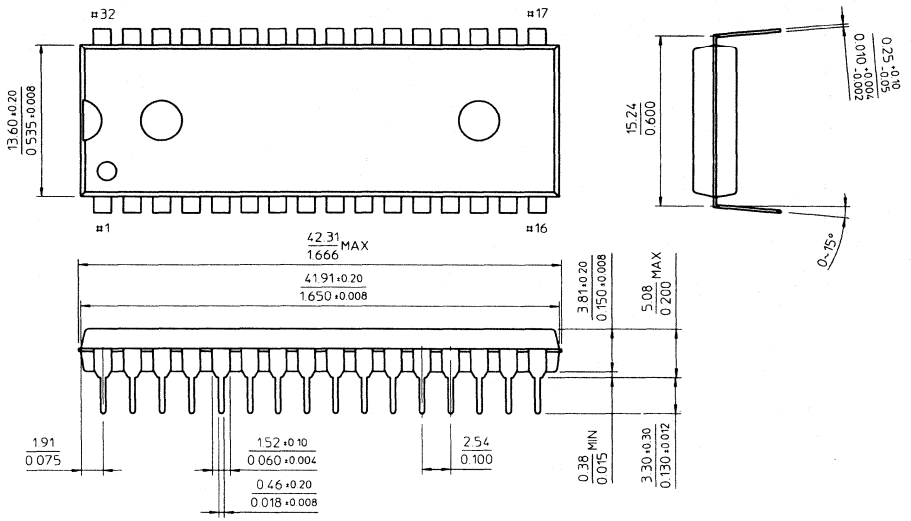
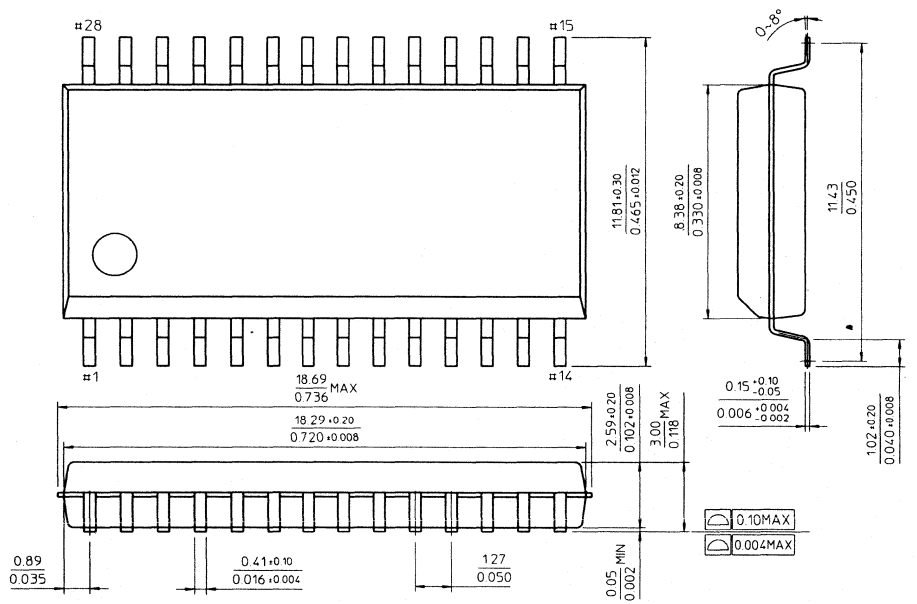


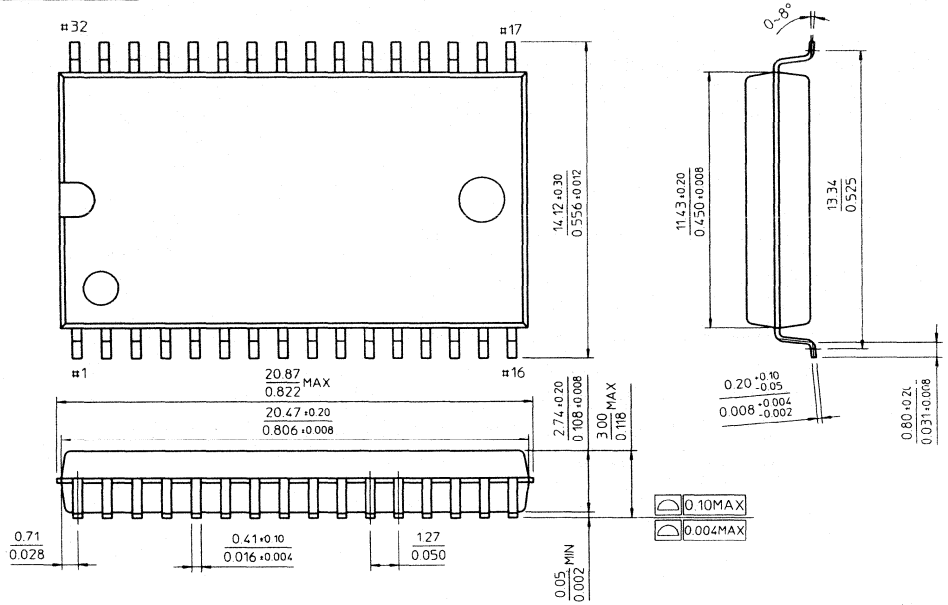
28-SOP-450



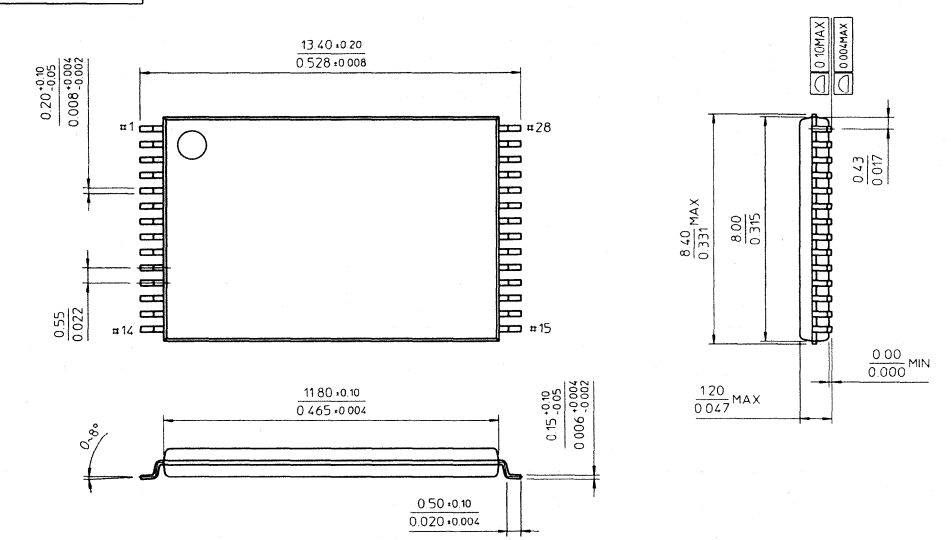
PACKAGE DIMENSIONS

Unit : mm/inch

32-SOP-525



28-TSOP1-0813.4F

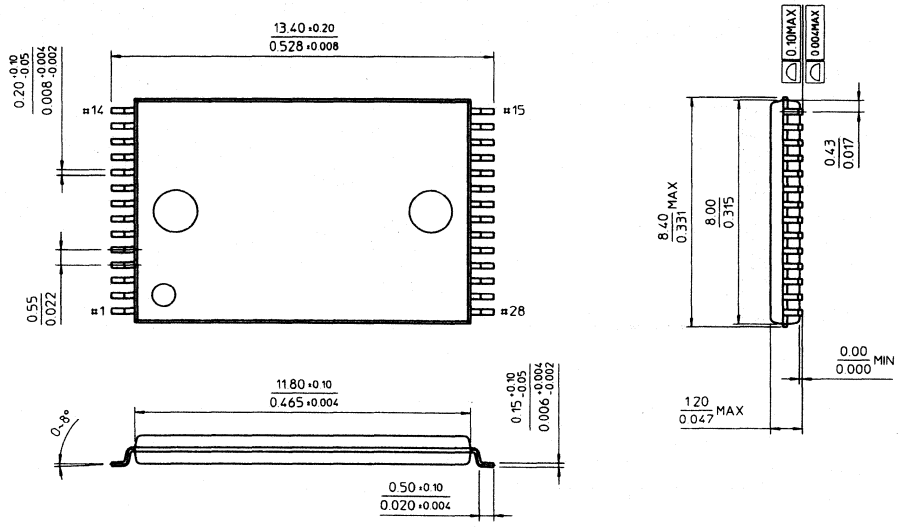


4

PACKAGE DIMENSIONS

Unit : mm/inch

28-TSOP1-0813.4R



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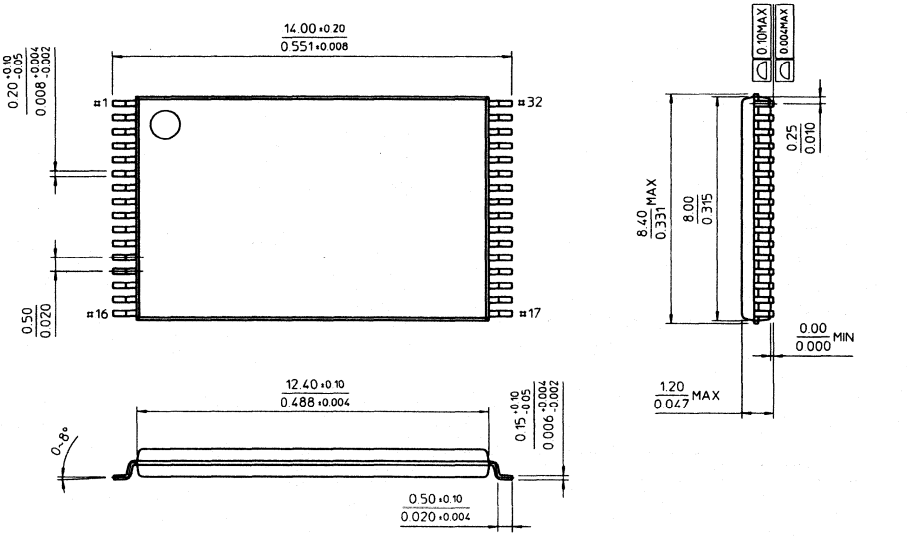
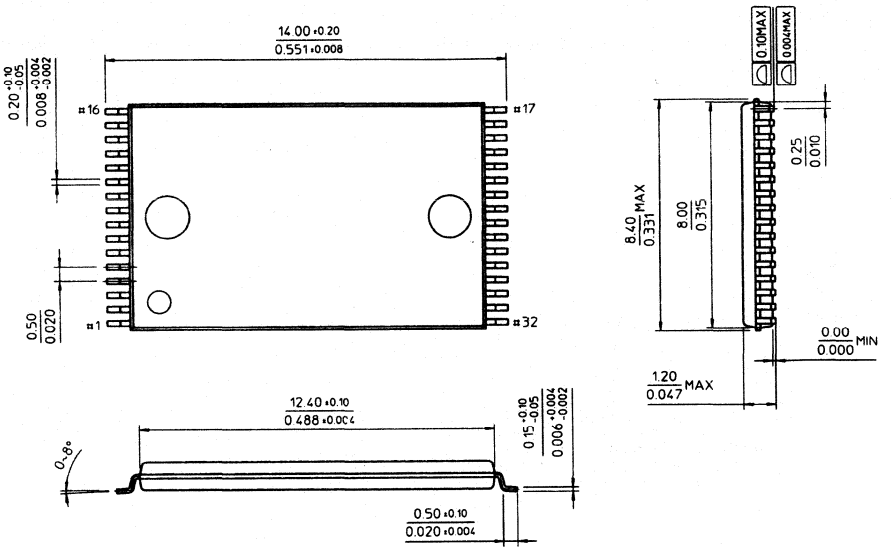


PACKAGE DIMENSIONS

Unit : mm/inch

32-TSOP1-0814R



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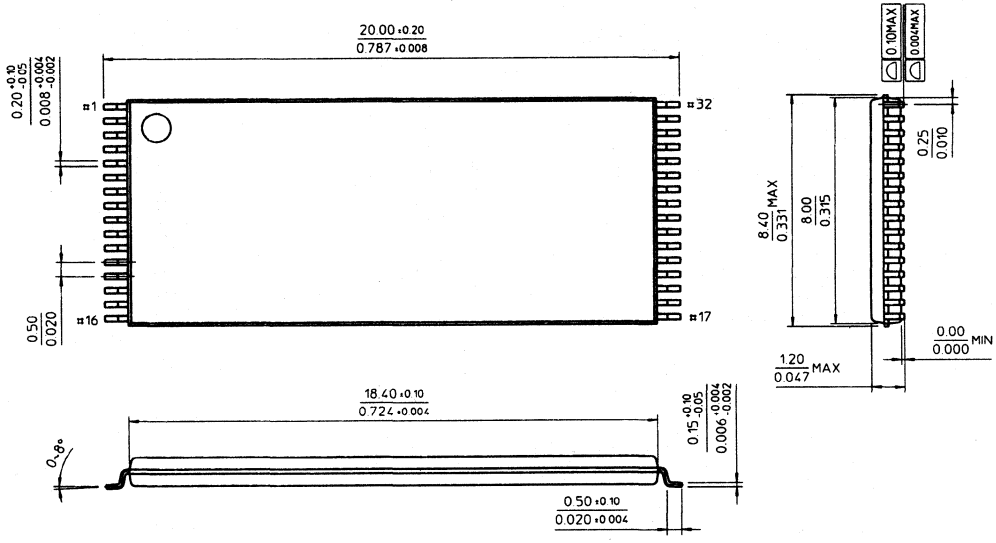
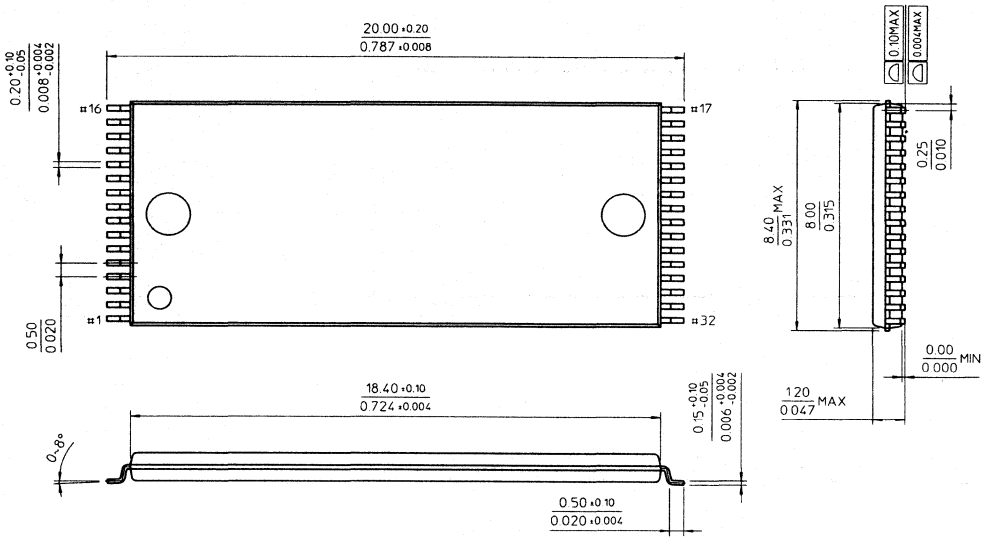


4

PACKAGE DIMENSIONS

Unit : mm/inch

32-TSOP1-0820R



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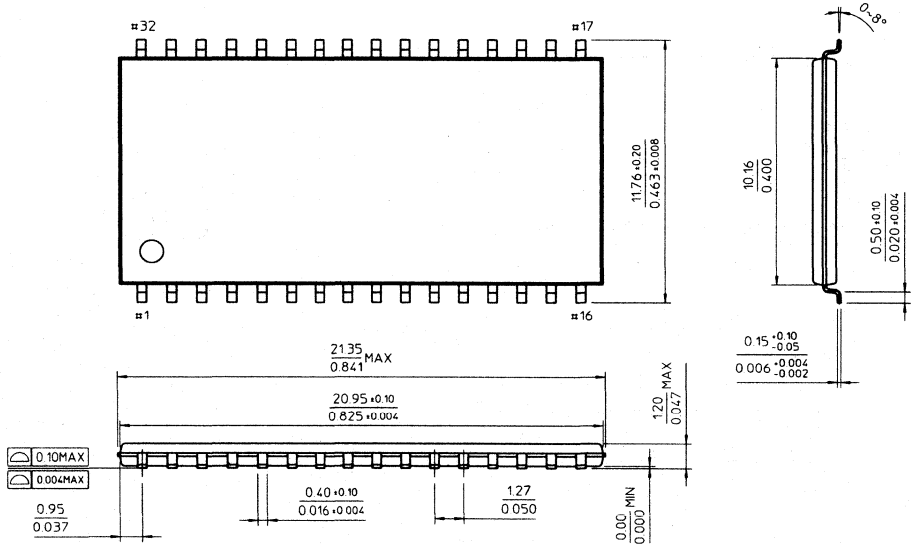
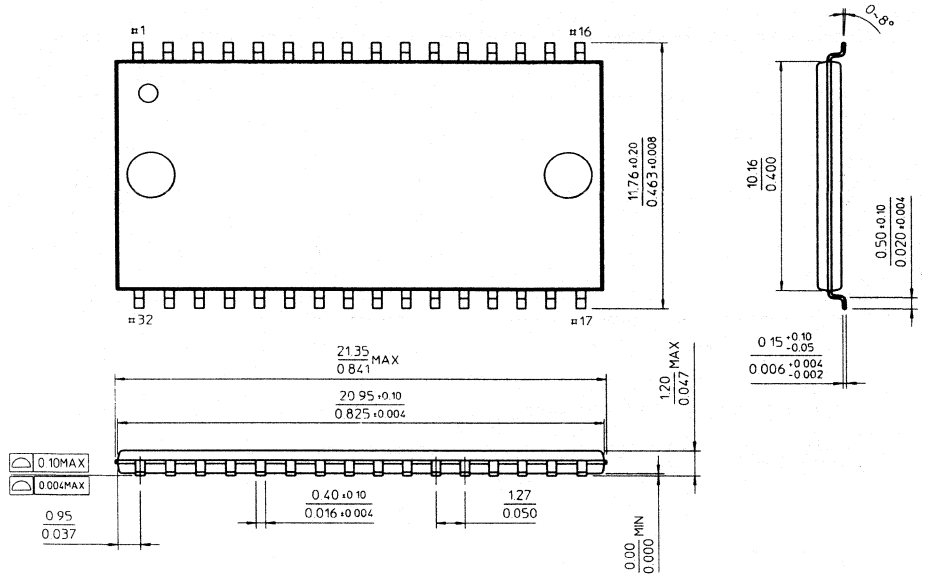


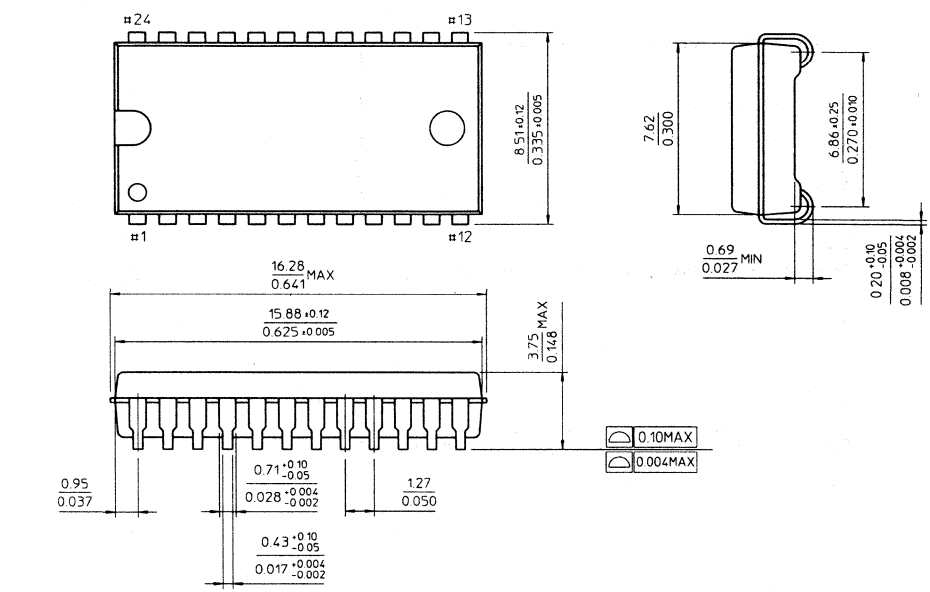
PACKAGE DIMENSIONS

Unit : mm/inch

32-TSOP2-400R



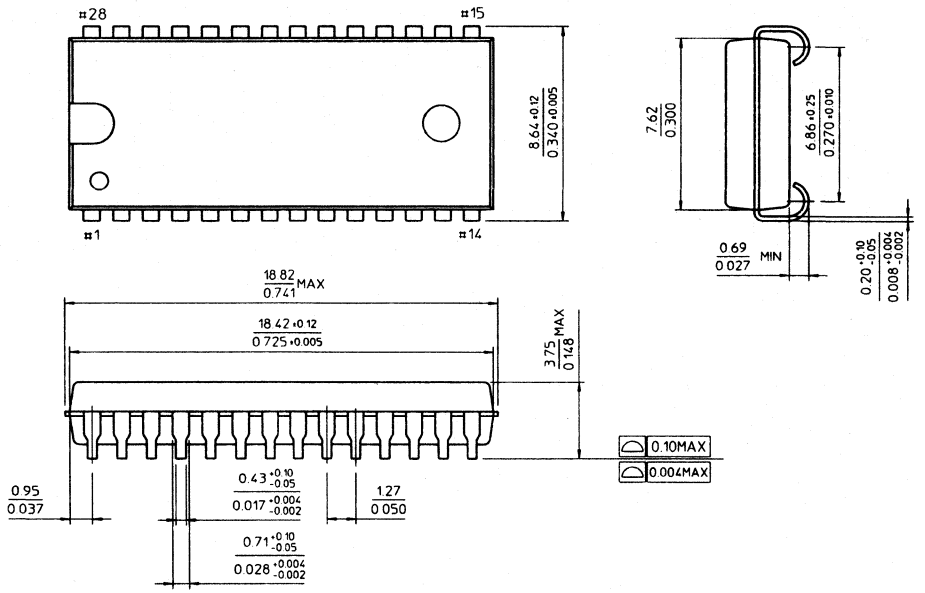
24-SOJ-300



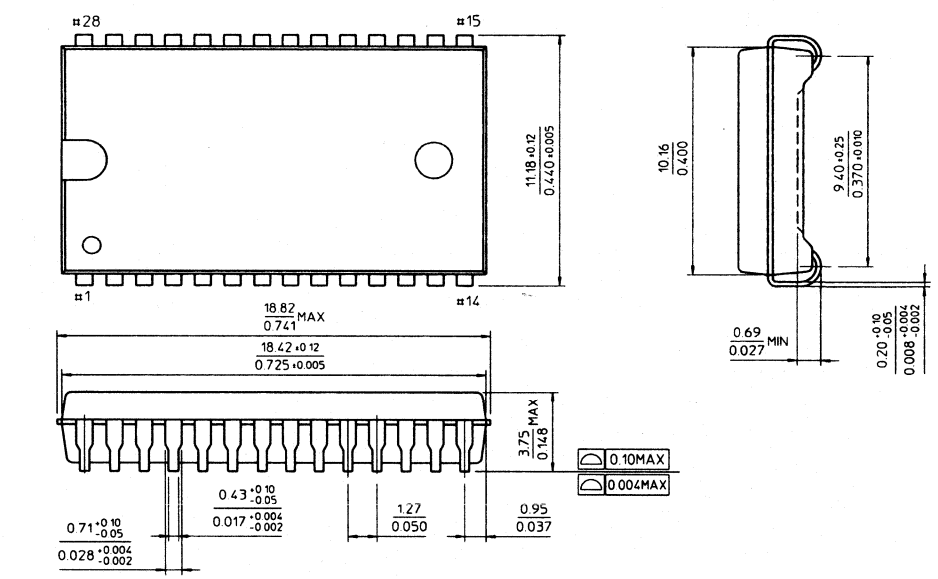
PACKAGE DIMENSIONS

Unit : mm/inch

28-SOJ-300



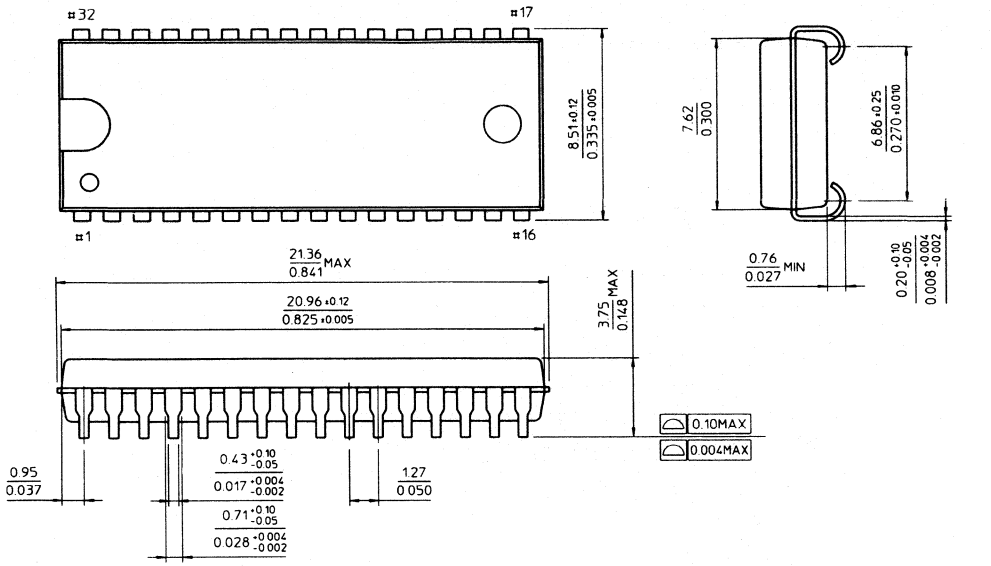
28-SOJ-400B



PACKAGE DIMENSIONS

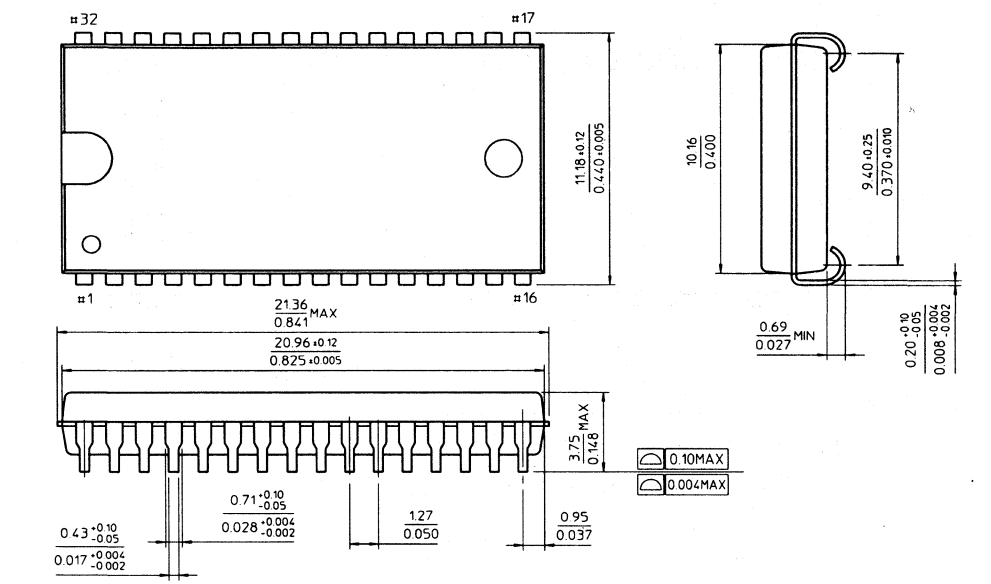
Unit : mm/inch

32-SOJ-300



Under Development

32-SOJ-400

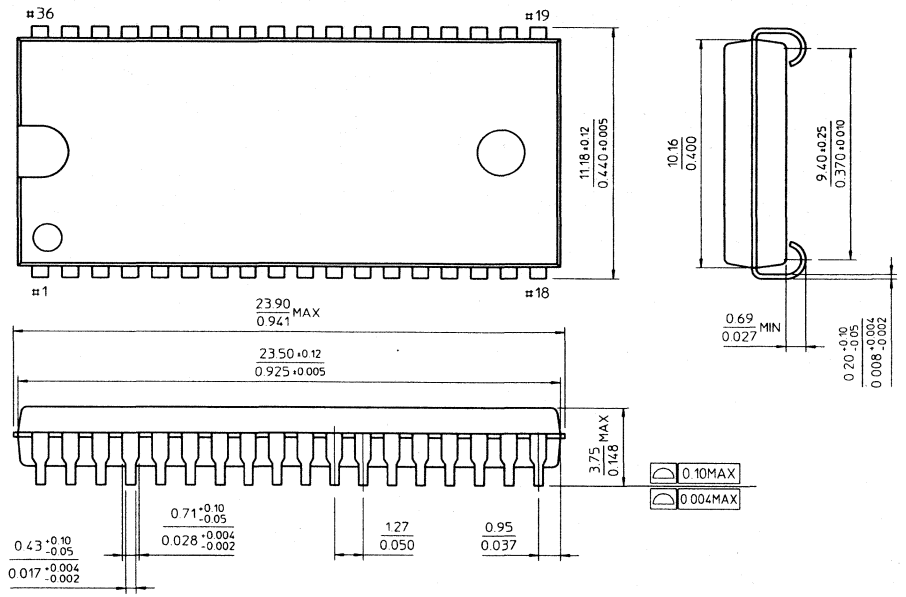


4

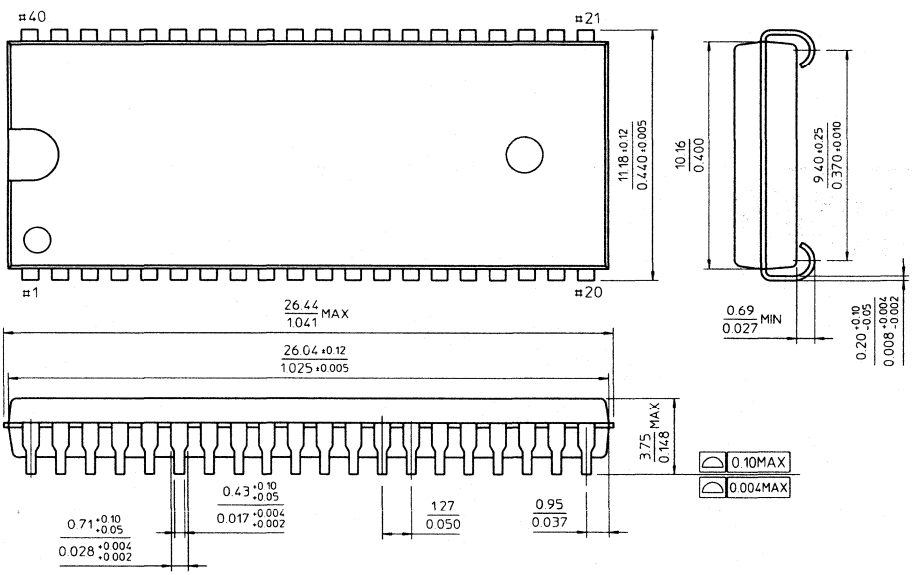
PACKAGE DIMENSIONS

Unit : mm/inch

36-SOJ-400



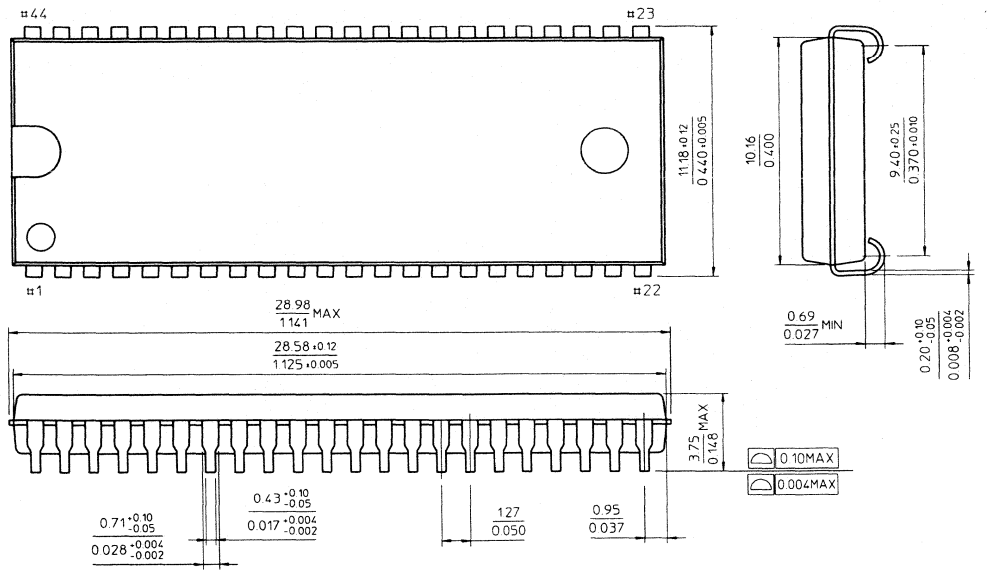
40-SOJ-400



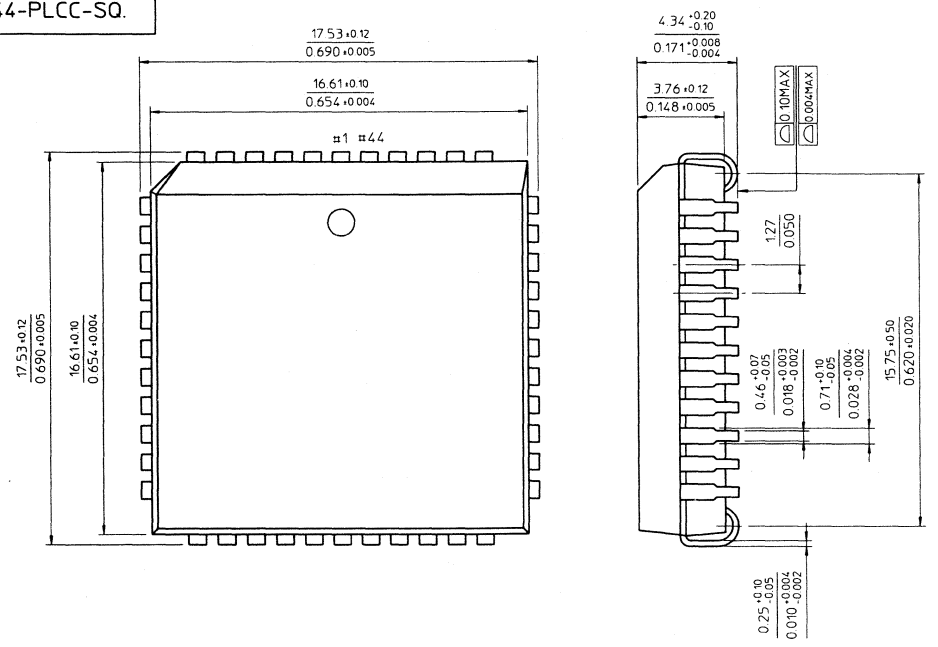
PACKAGE DIMENSIONS

Unit : mm/inch

44-SOJ-400



44-PLCC-SQ.

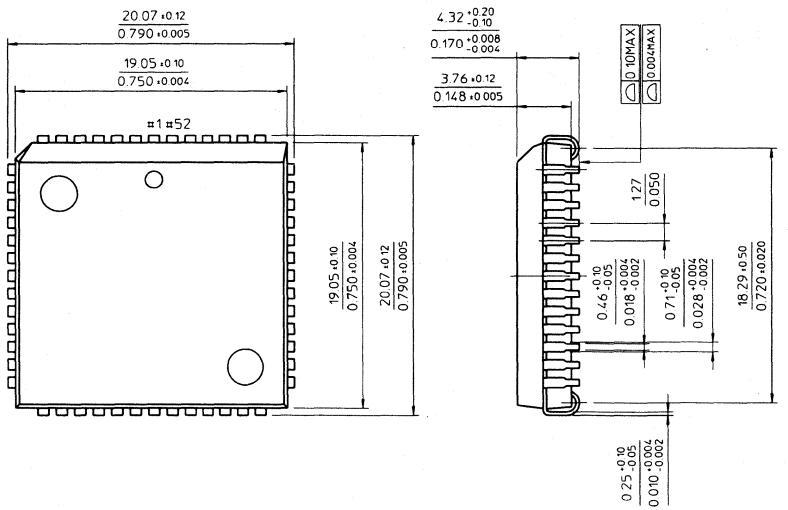


4

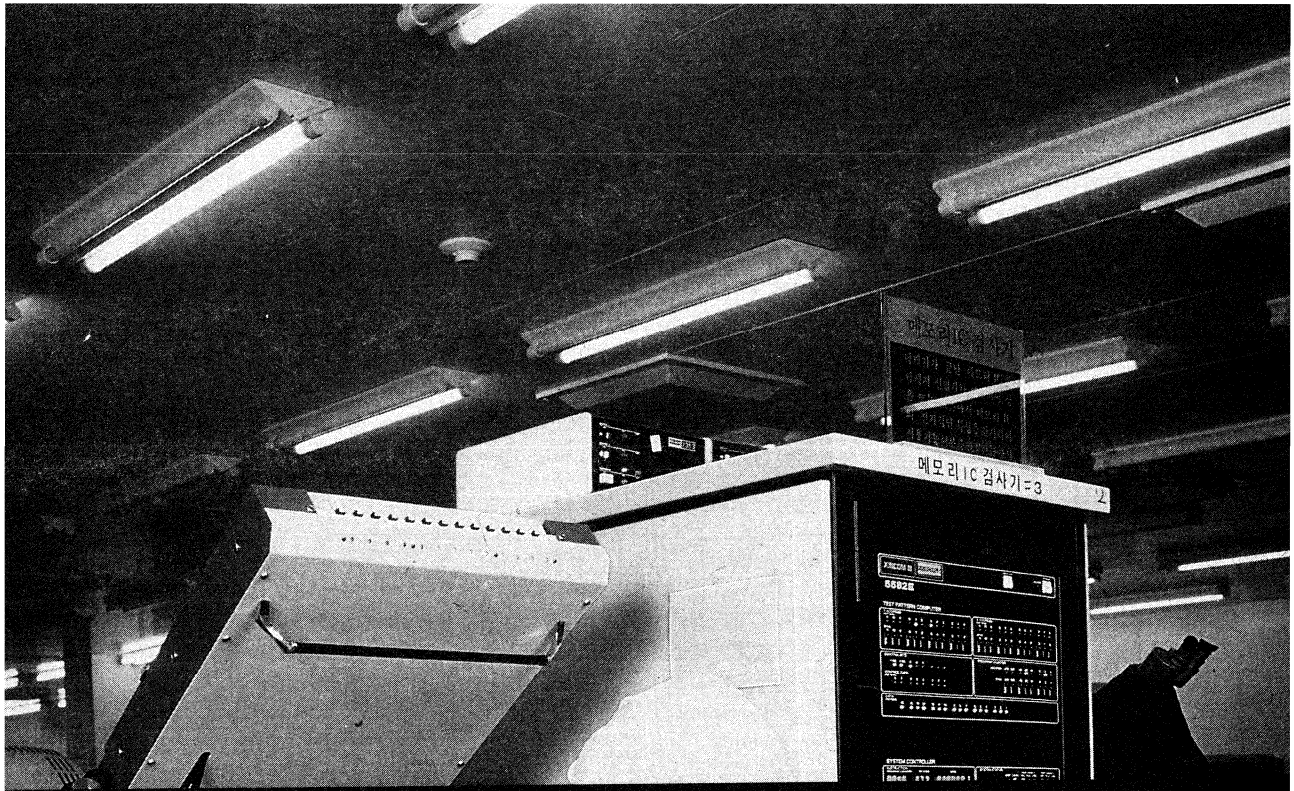
PACKAGE DIMENSIONS

Unit : mm/inch

52-PLCC-SQ.



Under Development



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Page	Wrong	Right
105	Isb 1 = 20uA at LL PWR	Isb 1 = 50uA at LL PWR
110	IDR = 10 uA at LL PWR	IDR = 25uA at LL PWR
125	NO 2 Pin is N.C.	No 2 Pin is A 16
149/151/152	Access Time: 70/85/100	Access Time: 70/100 .No 85 ns
342	Operating Current 12ns=175mA 15ns=160mA 20ns=155mA	Operating Current 12ns=240mA 15ns=230mA 20ns=220mA

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